OKI semiconductor

MSM5052

CMOS 4 BIT SINGLE CHIP VERY LOW POWER MICROCONTROLLER WITH TEMPERATURE DETECTION CIRCUIT AND LCD DRIVER

GENERAL DESCRIPTION

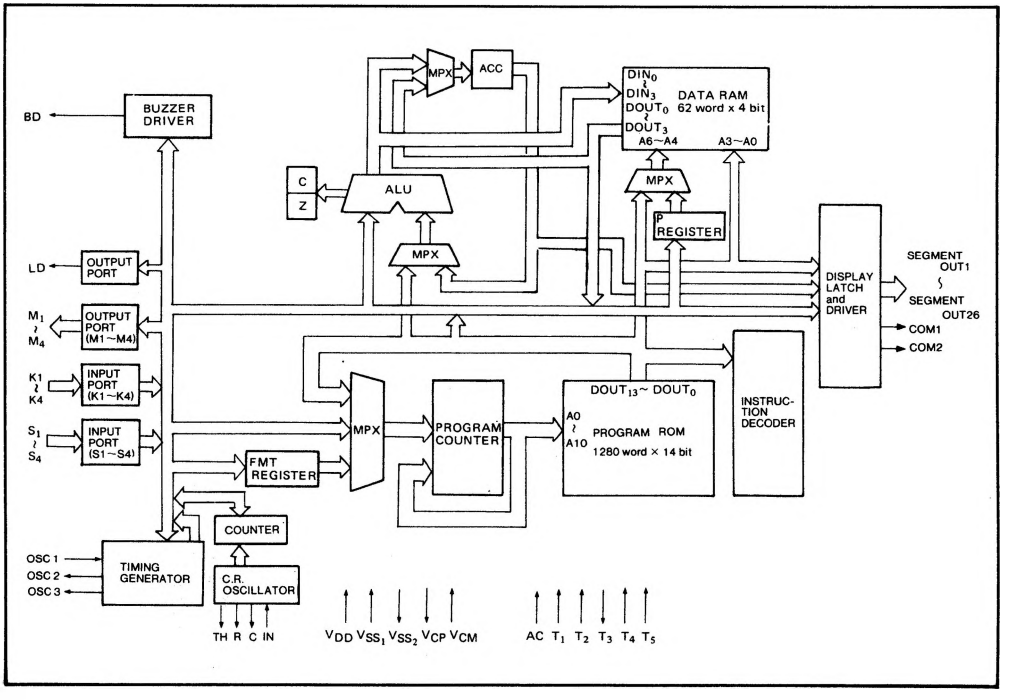
The OKI MSS5052 is a low-power and high-performance single-chip microcontroller employing complementary metal oxide semiconductor technology. Integrated onto a single chip are a 4 bit ALU, 18K bits of mask programmable ROM, 248 bits of data RAM, crystal oscillator, voltage doubler, timer, LCD driver, input port, output port and CR oscillator for temperature detection.

The MSM5052 is widely used in electronic products requiring low power operation, for example, thermometer and clinical thermometer with a time piece.

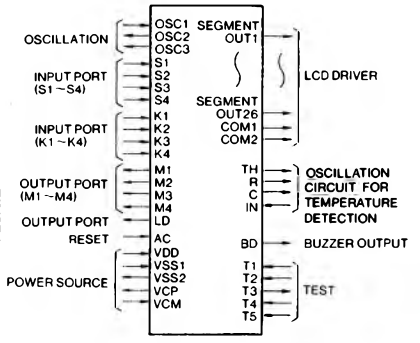
FEATURES

- Low Power Consumption 3 μA Typical
- 1280 × 14 Internal ROM
- 62 × 4 Internal RAM
- 4 × 2 Input Port
- 5 Output Port
- 4 × 4 Key Matrix Input (K1~K4, M1~M4)
- 26 LCD Driver
  (1/2 Duty, 1/2 Bias, 52 Segment)
- 42 Instructions
- 1.5 V Operating Voltage
- 32.768 kHz Crystal Oscillator
- 122.1 μs Instruction Cycle
- −20 to 75°C Operating Temperature
- 61 pad die

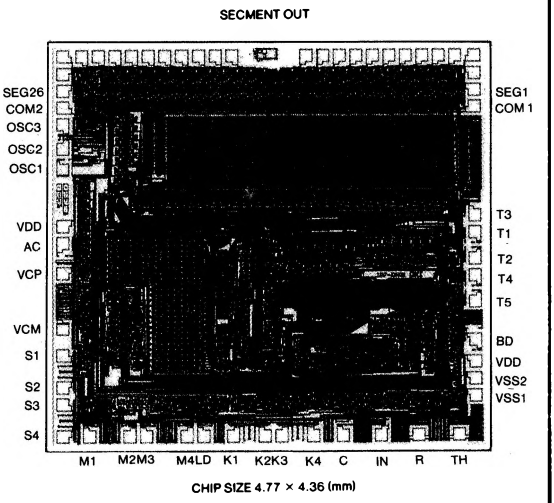
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



CHIP PAD LAYOUT



CHIP SIZE 4.77 × 4.36 (mm)

PIN DESCRIPTION

Designation	Function
V_{DD}	Circuit ground potential
V_{SS_1}	Power source (−1.5 V)
V_{SS_2}	Power source for LCD driver (−3.0 V) This terminal is connected to V_{DD} terminal through a 0.1 μF capacitor.
V_{CP}, V_{CM}	Booster capacitor connection terminals V_{CP} terminal is connected to V_{CM} terminal through a 0.1 μF capacitor.
OSC1, OSC3	Input and output terminals of oscillator inverter, 32.768 kHz crystal is connected to these terminals.
T1 ~ T5	Terminals to test internal logic, T1 ~ T3 and T5 are pulled down to V_{SS_1}. T4 is output. Test pins must be normally open.
AC	Terminal to clear internal logic pulled down to V_{SS_1}. After power is turned on, the MSM5052 must be reset by this terminal.
BD	Buzzer output
TH, R, C, IN	Terminal to CR oscillation circuit for temperature detection, fundamental resistor, thermistor, capacitor connection terminal.

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5052 is given on page 91. Each block of logic will be briefly discussed. For more information, please refer to the MSM5052 user's manual.

Program ROM

The MSM5052 addresses up to 1.25 K words of internal mask programmable ROM. Each word consists of 14 bits and all instructions are one word. The instructions are routed to a programmed logic array which generates the signals necessary for control of logic.

Data RAM

Data is organized in 4-bit nibbles. Internal data RAM consists of 62 nibbles.

The RAM is addressed by page address and column address. Normally page address is specified with page register, but direct addressing is available in Page 0.

Column address is directly addressed by operand of various instructions.

ALU

The ALU performs 4-bit parallel operation on RAM and ACC contents, or RAM contents and an immediate digit. It sets or resets the flags (Z, C) depending on the condition.

Program Counter (PC)

The program counter is 11 bits wide and specifies the address of the program ROM.

The PC is incremented by one every execution of the instruction, and then specifies the next instruction to be executed. However, the contents of the PC are rewritten by the execution of the Jump or Branch instruction.

There is no boundary in the ROM, so a Jump or Branch instruction can be put anywhere in the ROM.

Input/Output Port

Input Port (S1 ~ S4)

The input port (S1 ~ S4) is a 4 bit parallel input port. Each pin of the port is pulled down to V_{SS1} by an internal resistor, and the status of the port is fetched by an input instruction.

Input Port (K1 ~ K4)

The input port (K1 ~ K4) is a 4 bit parallel input port. Each pin of the port is pulled down to V_{SS1} by an internal resistor, and the status of the port is fetched by an input instruction.

Output Port (M1 ~ M4)

The output port (M1 ~ M4) is a 4 bit parallel output port. This port consists of data latches and buffers, and the contents of the data latches are rewritten by an output instruction.

Output Port (LD)

The output port (LD) is single output port. This terminal is used for loading of M1 to M4 data.

Display Function

The MSM5052 is provided with a segment output terminal which can directly drive a 1/2 bias, 1/2 duty LCD and the common drive output terminal COM1 and COM2.

The segment drive circuit consists of the display data latch, multiplexer and driver. If the data is sent to the display data latch with a display instruction, the LCD drive waveform is output to the segment drive output terminal.

Time Base

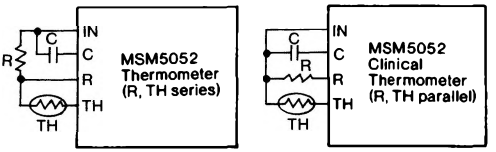
The time base for the CPU is provided by connecting a 32.768 kHz crystal to the OSC1 and OSC3 pins. One machine cycle is 122.1μs.

A hardware divider up to 1 Hz is provided enabling programs to implement a clock function by counting signals between 16 and 1 Hz.

Temperature Detection Circuit

The temperature detection circuit is composed of an external thermistor, a fundamental resistor, a capacitor and a built-in CR oscillation circuit.

Two types of temperature measurement circuit, as shown below, are available.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage 1	$V_{DD} - V_{SS_1}$	Ta = 25°C	−0.3 to +2.0	V
Supply Voltage 2	$V_{DD} - V_{SS_2}$	Ta = 25°C	−0.3 to +4.0	V
Input Voltage	V_{IN_1}	Ta = 25°C	V_{SS_1} −0.3 to +0.3	V
Storage Temperature	Tstg		−55 to 125	°C

OPERATING CONDITIONS

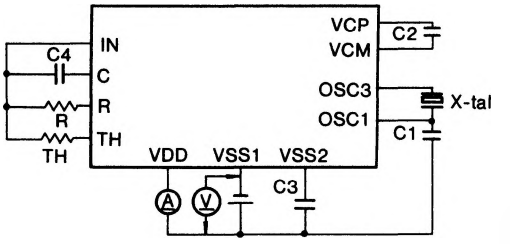
Parameter	Symbol	Limits	Unit
Operating Voltage	$V_{DD} - V_{SS_1}$	1.25 to 1.65	V
Operating Temperature	Topr	−20 to 75	°C

DC CHARACTERISTICS

(V_{DD} =0V, V_{SS_1} = −1.55V, V_{SS_2} = −3.0V, C_I = 30kΩ, Ta = 25°C)

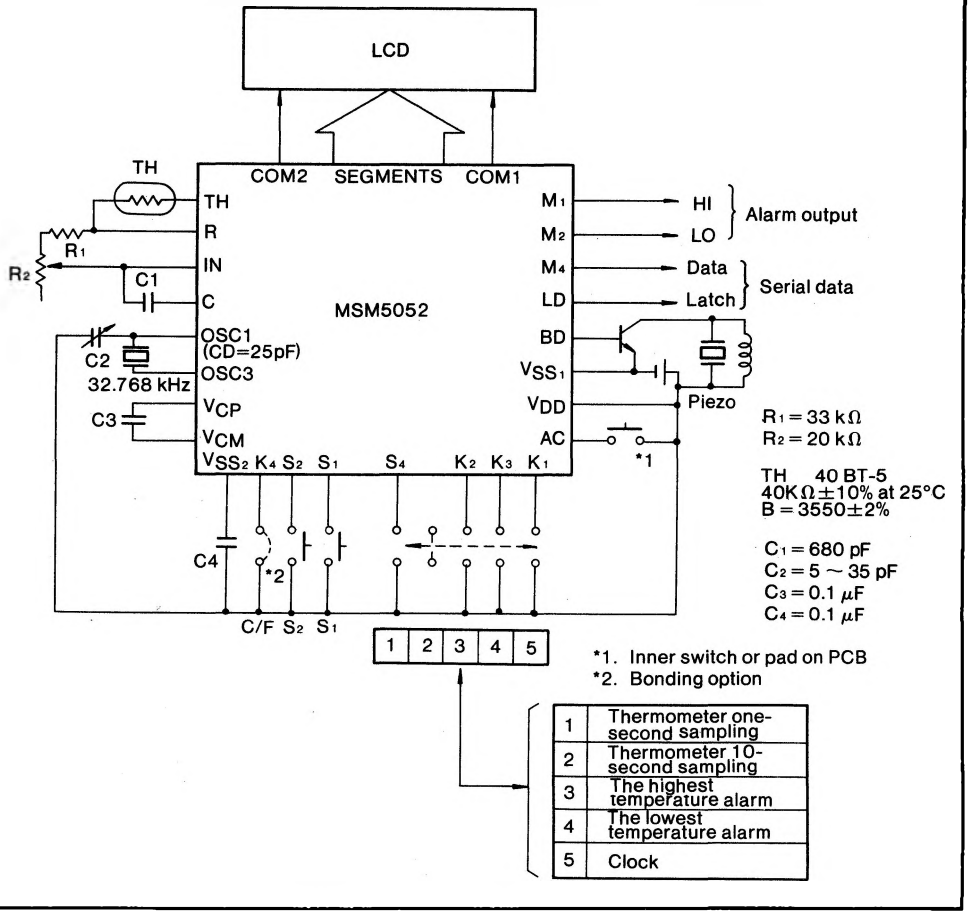
Parameter	Symbol	Condition	Limits			Unit
			Min.	Typ.	Max.	
Power supply current 1	I_{DD_1}	Temperature sampling off	–	3.0	–	μA
Power supply current 2	I_{DD_2}	Temperature sampling on	–	100	–	μA
Oscillation start voltage	$-V_{OSC}$	Within 10 seconds V_{SS_1} terminal	1.45	–	–	V
Output current 1 COM	I_{OH_1}	V_{OH_1} = −0.2V	−4	–	–	μA
	I_{OM_1}	$V_{OM_1} = V_{SS_1} \pm 0.2V$	4/−4	–	–	
	I_{OL_1}	V_{OL_1} = −2.8V	4	–	–	
Output current 2 SEGMENT	I_{OH_2}	V_{OH_2} = −0.2V	−0.4	–	–	μA
	I_{OL_2}	V_{OL_2} = −2.8V	0.4	–	–	
Output current 3 C. R. TH	I_{OH_3}	V_{OH_3} = −0.4 V	−400	–	–	μA
	I_{OL_3}	V_{OL_3} = −1.15V	400	–	–	
Output current 4 M1 ~ M4 LD	I_{OH_4}	V_{OH_4} = −0.4V	−100	–	–	μA
	I_{OL_4}	V_{OL_4} = −1.15V	10	–	–	
Output current 5 BD	I_{OH_5}	V_{OH_5} = −0.4V	−50	–	−500	μA
	I_{OL_5}	V_{OL_5} = −1.15V	4	–	–	
Input current S1 ~ S4 K1 ~ K4	I_{IH_1}	V_{IH_1} = 0V	1	10	100	μA
	I_{IL_1}	V_{IL_1} = −1.55V	–	–	−0.2	
Oscillator built-in capacitor	CD		–	25	–	pF

MEASURING CIRCUIT



C1 : 20 pF
C2, C3 : 0.1 μF
C4 : 3000 pF
X-tal : 32.768 kHz
R, TH : 10 KΩ

TYPICAL APPLICATION



DESCRIPTION OF INSTRUCTIONS

	Mnemonic	Instruction Code														Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Arithmetic operation	ADD ACC, AP	0	0	0	0	0	P	0	1	0	0		A			AP ← (AP) + (ACC)
	ADD #D, AP	0	1	1	0	0	P		D				A			AP ← (AP) − D
	ADC AP	0	0	0	0	0	P	0	1	0	1		A			AP ← Decimal adjust {(AP) + (ACC) + (C)}
	SUB ACC, AP	0	0	0	0	1	P	0	1	0	0		A			AP ← (AP) − (ACC)
	SUB #D, AP	0	1	1	0	1	P		D				A			AP ← (AP) − D
	SBC AP	0	0	0	0	1	P	0	1	0	1		A			AP ← Decimal adjust {(AP) − (ACC) − (C)}
	CMP ACC, AP	0	0	0	0	1	P	1	1	1	0		A			(AP) − (ACC)
	CMP #D, AP	0	1	0	1	1	P		D				A			(AP) − D
	INC AP	0	1	1	0	0	P	0	0	0	1		A			AP ← (AP) + 1
	DEC AP	0	1	1	0	1	P	0	0	0	1		A			A ← (AP) − 1
	XOR ACC, AP	0	0	0	0	0	P	0	1	1	1		A			AP ← (AP) ∀ (ACC)
	XOR #D, AP	0	1	1	1	1	P		D				A			AP ← (AP) ∀ D
Bit operation	BIT ACC, AP	0	0	0	0	0	P	1	1	1	0		A			(AP) V $\overline{(ACC)}$
	BIT #D, AP	0	1	0	1	0	P		D				A			(AP) V $\overline{D}$
	BIS ACC, AP	0	0	0	0	0	P	0	1	1	0		A			AP ← (AP) V (ACC)
	BIS #D, AP	0	1	0	0	0	P		D				A			AP ← (AP) V D
	BIC ACC, AP	0	0	0	0	1	P	0	1	1	0		A			AP ← (AP) Λ $\overline{(ACC)}$
	BIC #D, AP	0	1	0	0	1	P		D				A			AP ← (AP) Λ $\overline{D}$
Shift	ASR AP	0	0	0	0	0	P	0	0	1	1		A			⌊→(C) 0 → (AP)⌋
	ASL AP	0	0	0	0	1	P	0	0	1	1		A			(C) ← (AP) ← 0
Flag operation	CLZ	0	0	0	0	0	0	1	0	1	0	0	0	0	0	Z ← 0
	CLC	0	0	0	0	0	0	1	0	0	1	0	0	0	0	C ← 0
	CLA	0	0	0	0	0	0	1	0	1	1	0	0	0	0	Z ← 0, C ← 0
	SEZ	0	0	0	0	1	0	1	0	1	0	0	0	0	0	Z ← 1
	SEC	0	0	0	0	1	0	1	0	0	1	0	0	0	0	C ← 1
	SEA	0	0	0	0	1	0	1	0	1	1	0	0	0	0	Z ← 1, C ← 1
Data transfer	MOV ACC, AP	1	1	1	1	0	P	0	0	0	0		A			AP ← (ACC)
	MOV ACC, AX	1	1	1	1	0	0	0		X			A			AX ← (ACC)
	MOV #D, AP	0	1	1	1	0	P		D				A			AP ← D
	MOV AP, ACC	1	1	1	1	1	P	0	0	0	0		A			ACC ← (AP)
	MOV AX, ACC	1	1	1	1	1	0	0		X			A			ACC ← (AX)
	CHG AP	1	1	1	0	0	P	0	0	0	0		A			(ACC) ⟷ (AP)
	CHG AX	1	1	1	0	0	0	0		X			A			(ACC) ⟷ (AX)

DESCRIPTION OF INSTRUCTIONS (CONT.)

	Mnemonic	Instruction Code														Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Jump	JMP adrs	1	0	0	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	PC ← adrs
	JMP @AP	0	0	0	0	0	P	1	1	0	1	A				PC ← (PC) + (AP) + 1
	JMPIO @AP	0	0	0	0	1	P	1	1	0	1	A				PC ← (PC) + [(AP)A7H] + +1
	BEP +n BZE +n	0	0	0	1	1	0	0	1	0	n_4	n_3	n_2	n_1	n_0	PC ← (PC) + n + 1, if Z = 1
	BNE +n BNZ +n	0	0	0	1	1	0	1	1	0	n_4	n_3	n_2	n_1	n_0	PC ← (PC) + n + 1, if Z = 0
	BCS +n BLT +n	0	0	0	1	1	0	0	0	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) + n + 1, if C = 1
	BCC +n BGE +n	0	0	0	1	1	0	1	0	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) + n + 1, if C = 0
	BGT +n	0	0	0	1	1	0	1	1	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) + n + 1, if Z = 0 and C = 0
	BLE +n	0	0	0	1	1	0	0	1	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) + n + 1, if Z = 1 or C = 1
Input/ Output	INP Port, AP	1	1	0	1	0	P	Port				A				AP ← (Port)
	OUT AP, Port	1	1	0	1	1	P	Port				A				Port ← (AP)
	OUT #D, Port	0	0	0	1	0	0	Port				D				Port ← D
Display	DSP digit, AP	0	0	1	0	0	P	digit				A				digit ← (AP), (ACC)
	DSPF digit, AP	0	0	1	1	0	P	digit				A				digit ← (AP) via table
CPU control	HALT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	Halt CPU
	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	No Operation