Preliminary

OKI semiconductor

MSM38512RS

65536 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM38512RS is an N-channel silicon gate E/DMOS device ROM with a 65,536 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 10mA(max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

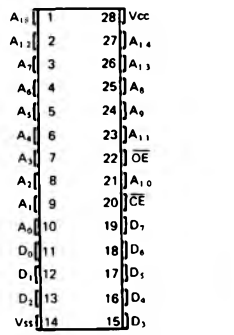
Since it provides $\overline{CE}$, $\overline{OE}$, signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

FEATURES

- 512k bits: 65,536 words x 8 bit
- high speed: access time 200 ns max
- low power: active current 60 mA max
  standby current 10 mA max
- wide tolerance operating: Vcc = 5 V ± 10 %
- fully static operating: using no clock
- fully TTL compatible
- pin compatible to 512k EPROM
- packaged to 28 pins plastic
- fabricated with 2um NMOS silicon gate technology

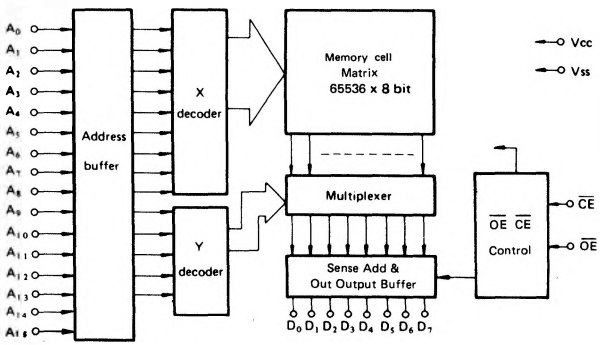
PIN CONFIGURATION

(Top View)



$\overline{OE}$: Output enable
Vcc, Vss : Power supply voltage
$A_0 - A_{15}$: Address input
$\overline{CE}$: Chip enable
$D_0 - D_7$: Data output

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Par package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2.2	–	6	V
	V_{IL}	–	−0.3	–	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
Input Leak Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leak Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	−10	–	10	μA
Power Supply Current	I_{CC}		–	–	60	mA
	I_{CCS}		–	–	10	mA

AC CHARACTERISTICS

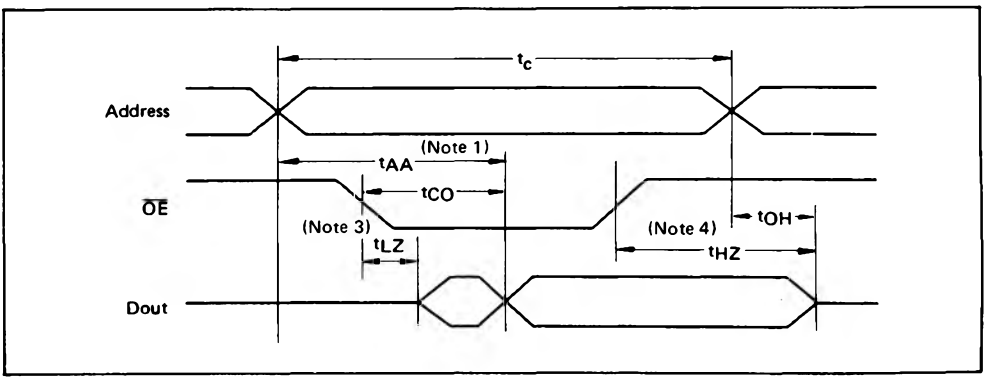
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} 2.4V, V_{IL} 0.6 V
Input Rising, Falling Time	tr = tf = 15 ns
Timing Measuring Point Voltage	Input Voltage = 1.5V
	Output Voltage = 0.8V & 2.0V
Loading Condition	C_L = 100 pF + 1 TTL

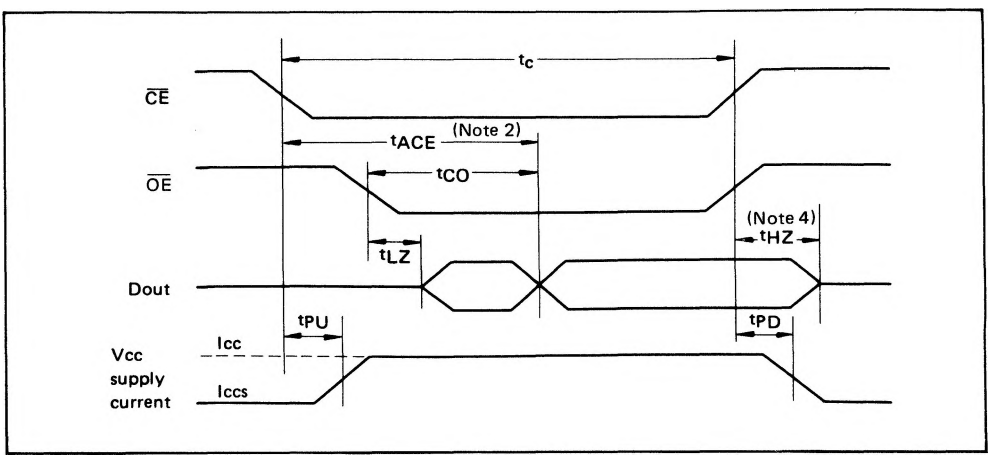
READ CYCLE

Parameter	Symbol	xxxxxx Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	200	–	–	ns	
Address Access Time	t_{AA}	–	–	200	ns	
Chip Enable Access Time	t_{ACE}	–	–	200	ns	
Output Delay Time	t_{CO}	–	–	50	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	50	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–	–	ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) t_{LZ} is determined by the later level, $\overline{CE}$ "L" or $\overline{OE}$ "L".
(4) t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

($Ta = 25^{\circ}C$, f = 1MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I = 0V
Output Capacitance	C_O		10	pF	V_O = 0V