OKI semiconductor

MSM37S64ARS/37S64RS

131,072-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM37S64 is a fully decoded dynamic NMOS random access memory organized as 131,072 one-bit words using 65,536 bit stacked. The design is optimized for high-speed, high performance applications such as main-frame memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

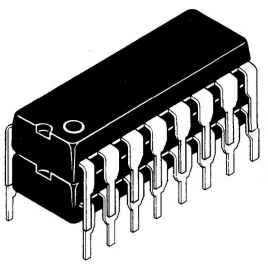
Multiplexed row and column address inputs permit the MSM37S64 to be housed in a standard 16 pin DIP.

The MSM37S64 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

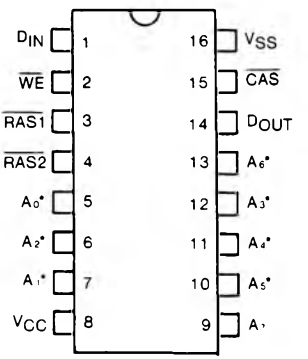
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 131,072 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 150 ns max (MSM37S64-15)
  - 200 ns max (MSM37S64-20)
- Cycle time:
  - 270 ns min (MSM37S64-15)
  - 330 ns min (MSM37S64-20)
- Low power:
  - 360 mW active, 55 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



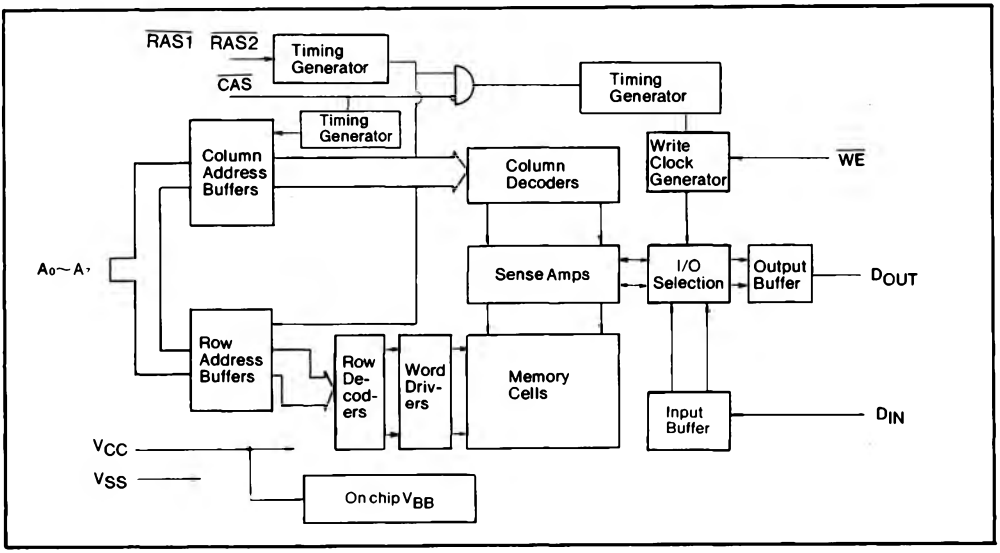
PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
A_0–A_7	Address Inputs
$\overline{RAS1}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address
1. Designates Bottom Module
2. Designates Top Module

FUNCTIONAL BLOCK DIAGRAM (ONE MODULE)



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

(TA = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	2	W
Short circuit output current	I_{os}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Current* – One Module Selected Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		65	mA	1
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		10	mA	
Refresh Current* – One Module Selected Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} =min.)	I_{CC3}		45	mA	
Page Mode Current* – One Module Selected Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC4}		65	mA	1
Refresh Current* – Two Module Selected Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC5}		80	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5mA) Output low voltage (I_{OL} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance ($A_0 \sim A_7$, D_{IN})	C_{IN1}	10	pF
Input Capacitance ($\overline{RAS1}$, $\overline{RAS2}$)	C_{IN2}	10	pF
Input Capacitance ($\overline{CAS}$)	C_{IN3}	15	pF
Input Capacitance ($\overline{WE}$)	C_{IN4}	12	pF
Output Capacitance (D_{OUT})	C_{OUT}	14	pF

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSM37S64-15		MSM37S64-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	30	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Units	MSM37S64-15		MSM37S64-20		Note
			Min.	Max.	Min.	Max.	
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	20		25		

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSM37S64A-15		MSM37S64A-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	260		330		
Read-write cycle time	t_{RWC}	ns	280		345		
Page mode cycle time	t_{PC}	ns	145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	75		100		
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	ns	60		80		
$\overline{CAS}$ precharge time	t_{CPN}	ns	35		45		
$\overline{CAS}$ pulse width	t_{CAS}	ns	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	20		25		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	95		125		
Read command set-up time	t_{RCS}	ns	0		0		

AC CHARACTERISTICS (Continued)

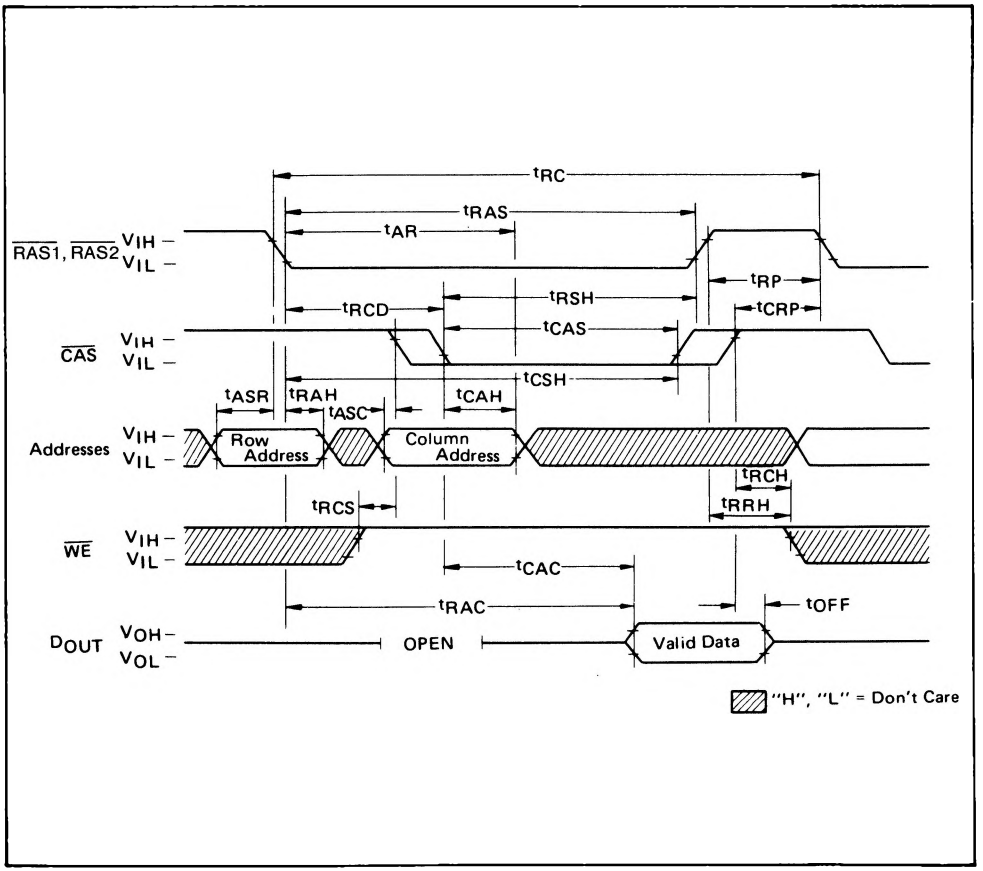
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Units	MSM37S64A-15		MSM37S64A-20		Note
			Min.	Max.	Min.	Max.	
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	120		155		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	45		55		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	120		155		8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	0		0		

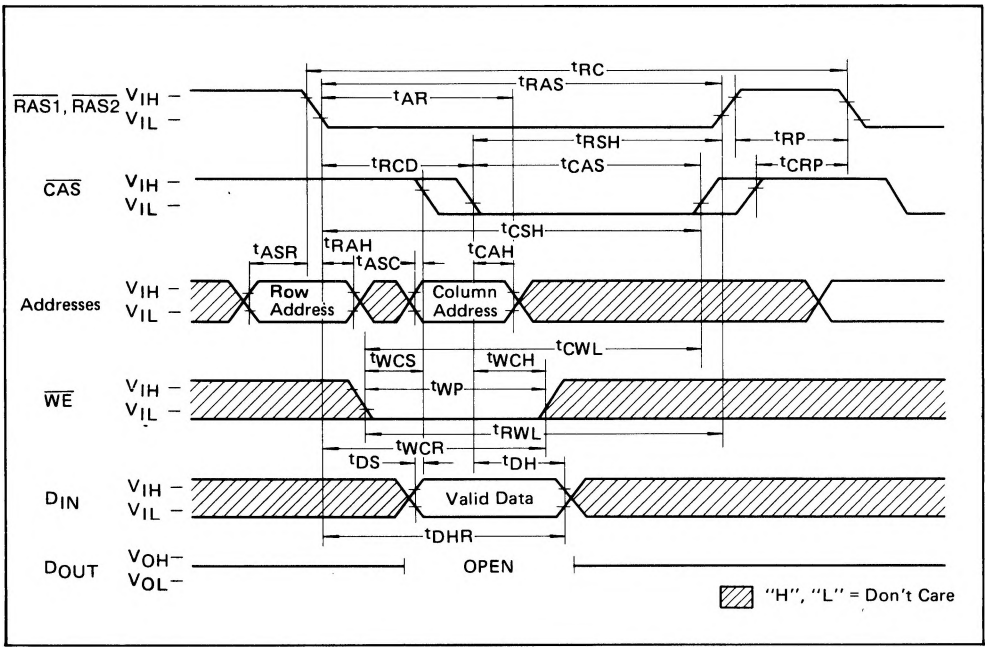
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. AC measurements assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$ (Max.)
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} < t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

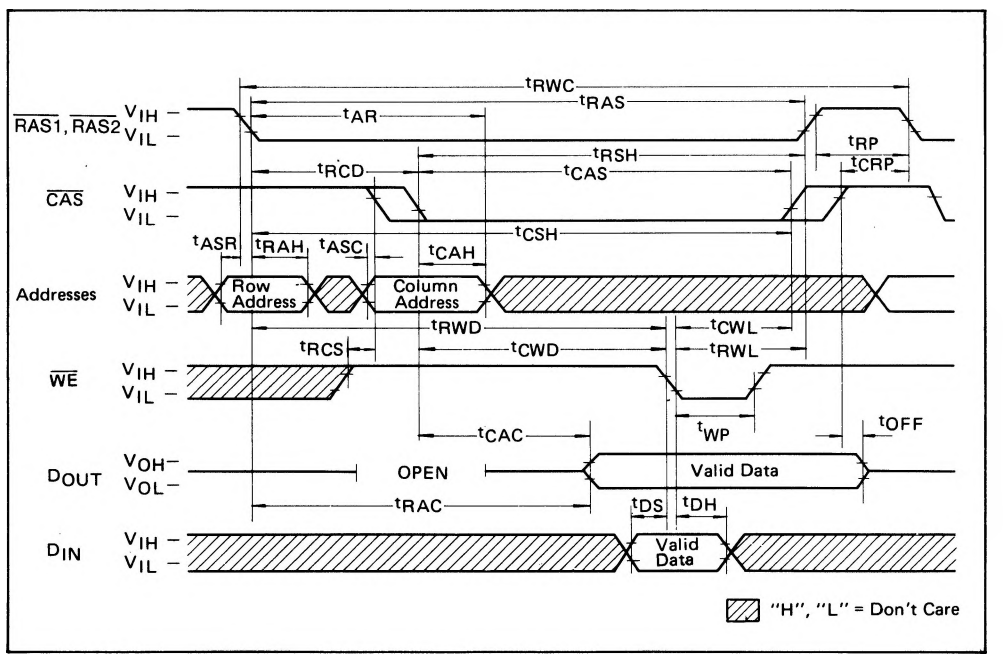
READ CYCLE TIMING



WRITE CYCLE TIMING
(EARLY WRITE)

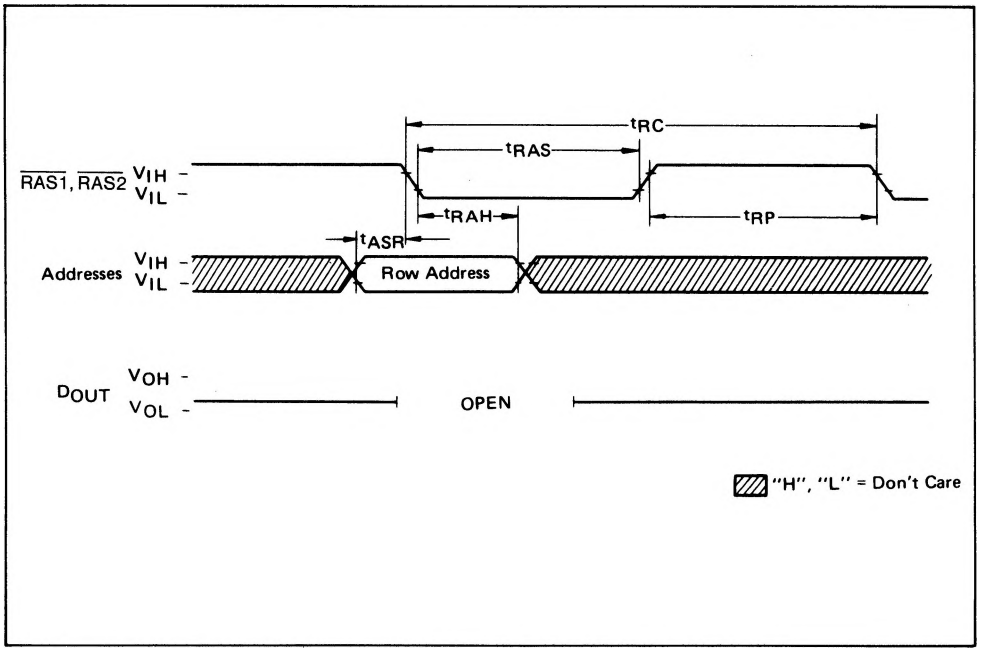


READ-WRITE/READ-MODIFY-WRITE CYCLE

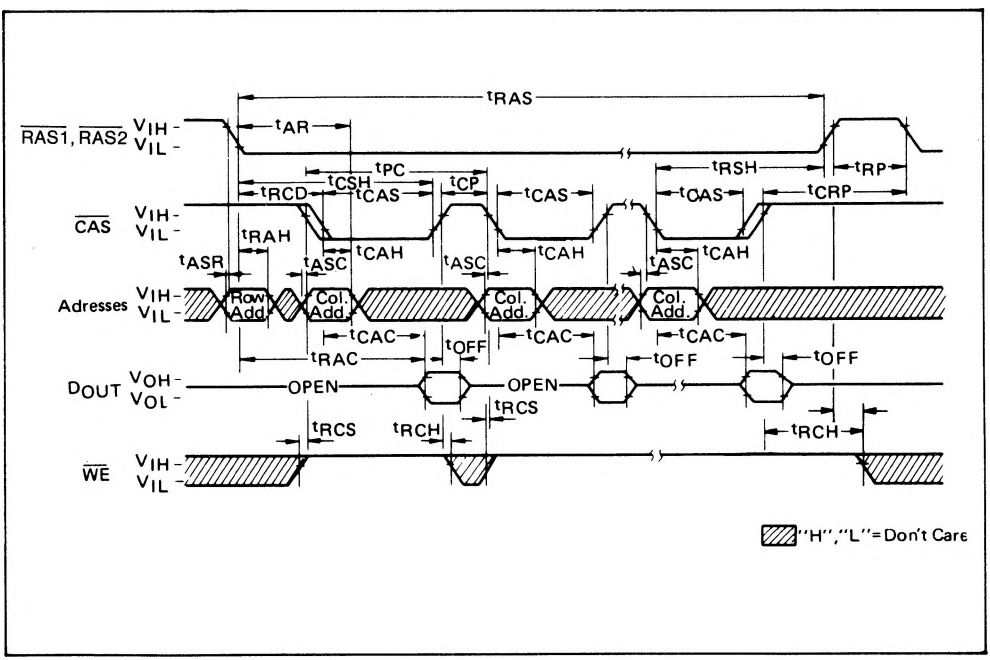


$\overline{RAS}$ ONLY REFRESH TIMING

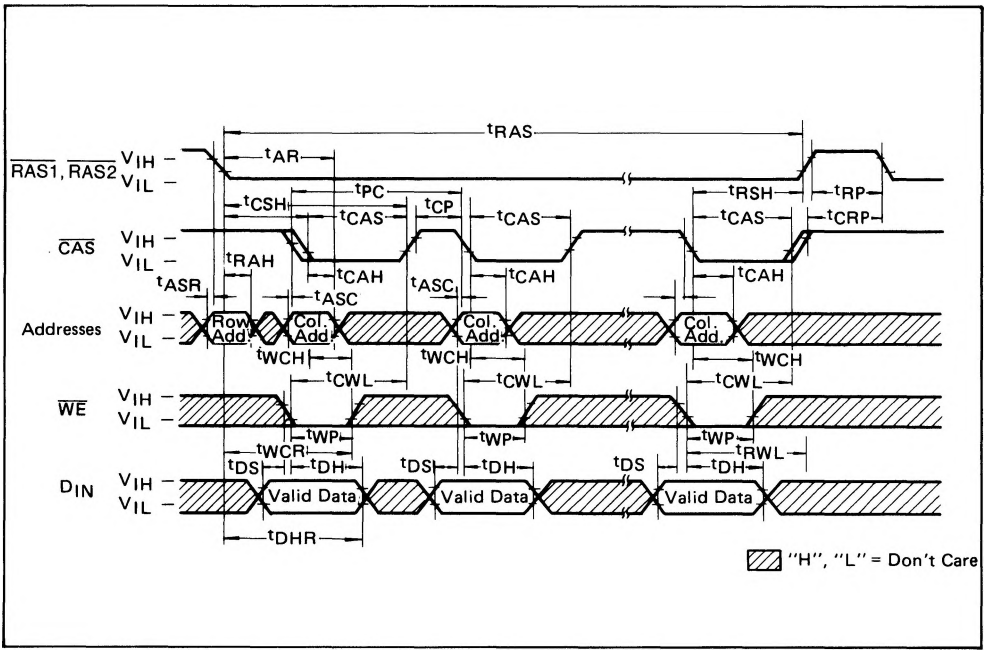
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



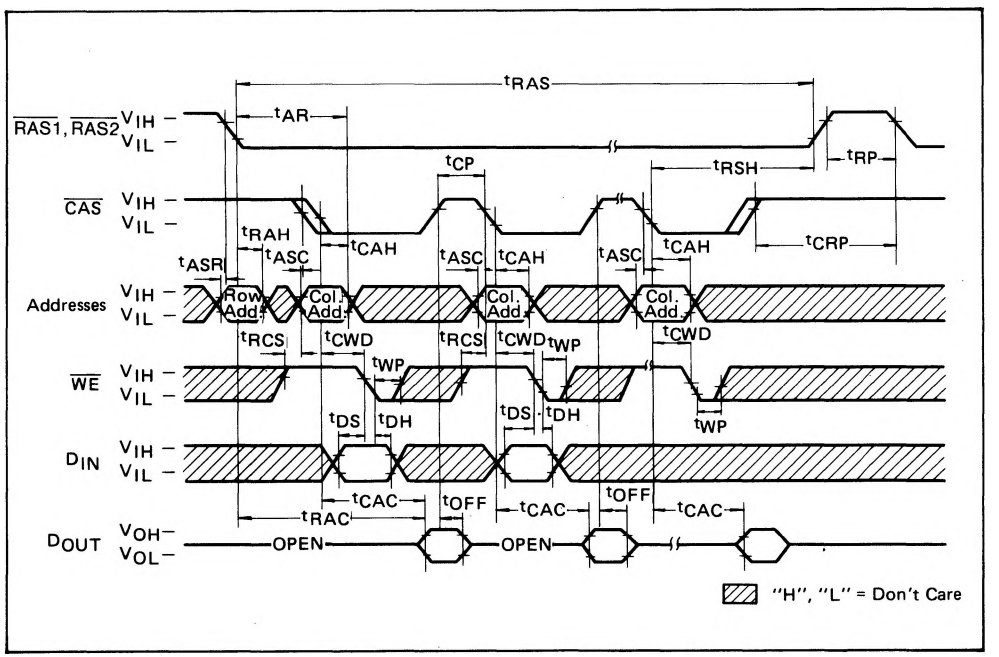
PAGE MODE READ CYCLE



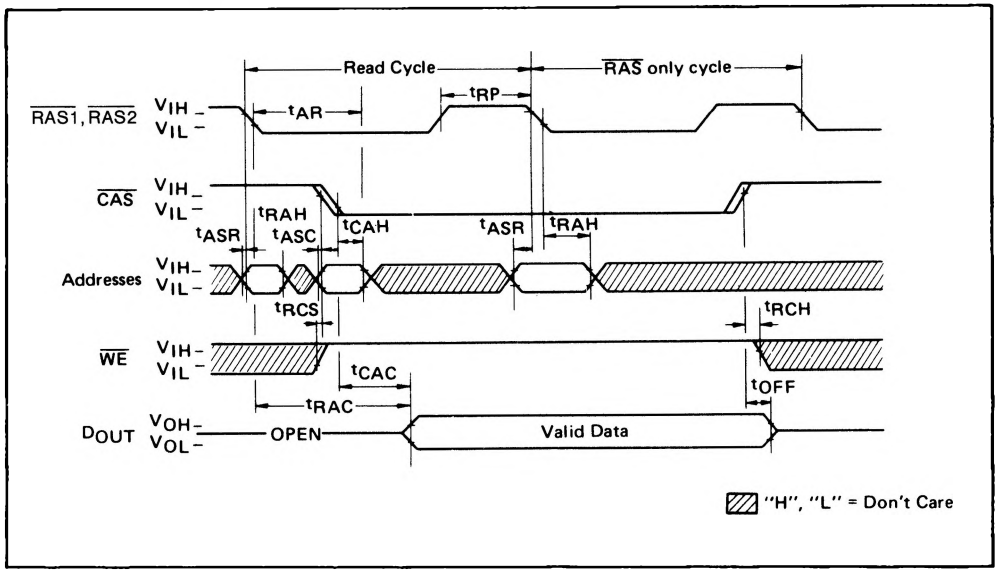
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the one module. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses. The top module or bottom module is selected with $\overline{RAS1}$ input and $\overline{RAS2}$ input.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM37S64 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM37S64 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at

each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.