OKI semiconductor

MSM3764 AAS/RS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-004-32)

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

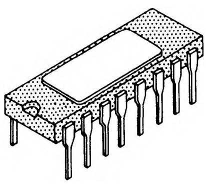
Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

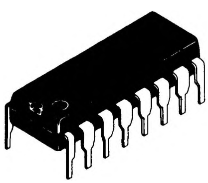
The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

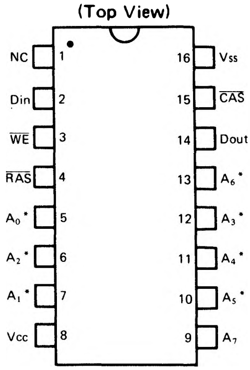
- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MSM3764A-12)
  150 ns max (MSM3764A-15)
  200 ns max (MSM3764A-20)
- Cycle time,
  230 ns min (MSM3764A-12)
  260 ns min (MSM3764A-15)
  330 ns min (MSM3764A-20)
- Low power: 330 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance





PIN CONFIGURATION

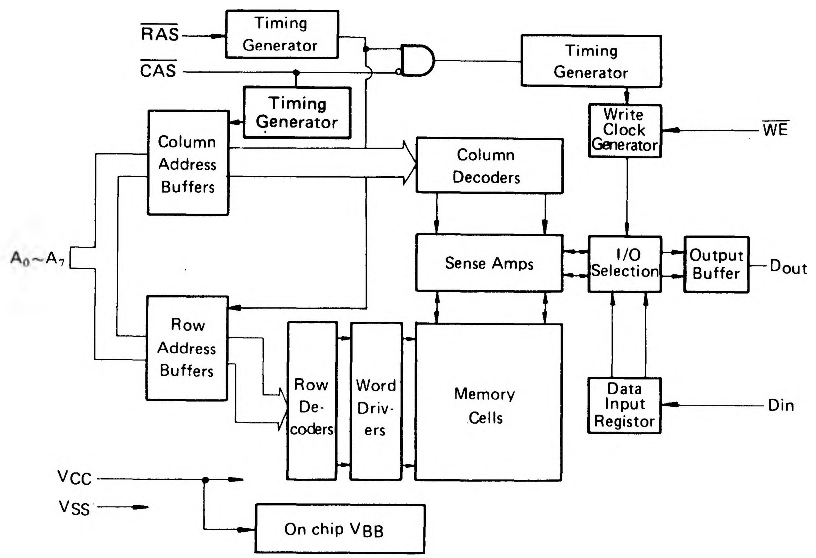
(Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	-55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		60	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		40	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
Input Leakage Current Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{LO}	−10	10	μA	
Output Levels					
Output high voltage (I_{OH} = −5 mA)	V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4	V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	8	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

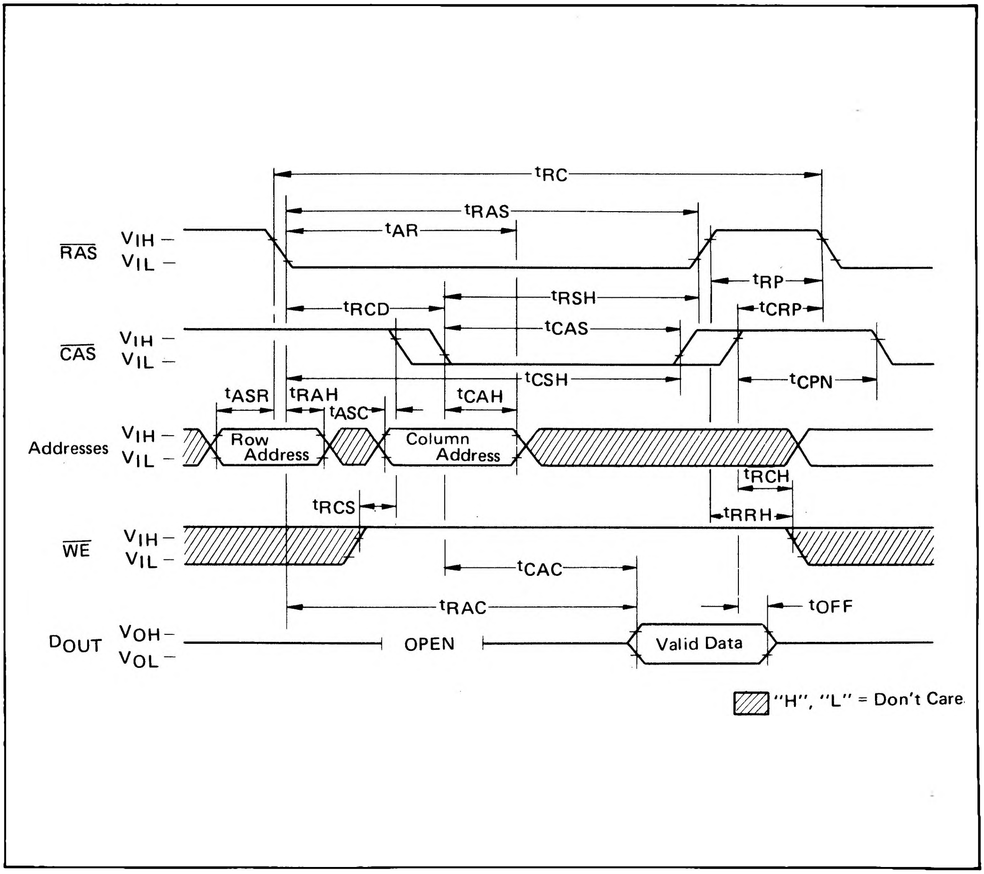
(Recommended operating conditions unless otherwise noted.)

Note 1,2,3

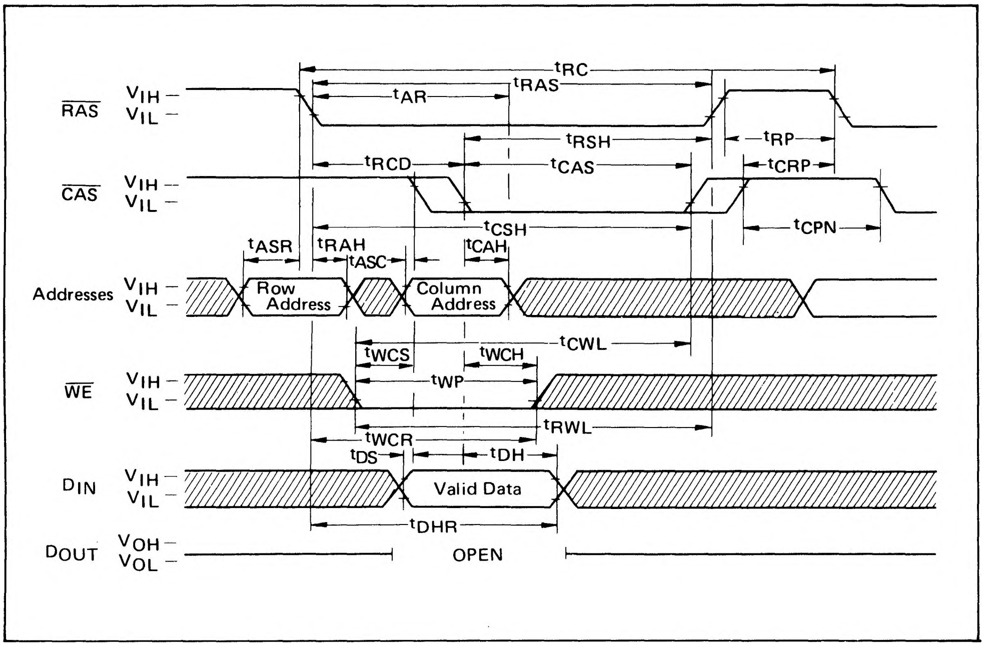
Parameter	Symbol	Units	MSM3764A-12		MSM3764A-15		MSM3764A-20		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2		2	
Random read or write cycle time	t_{RC}	ns	220		260		330		
Read-write cycle time	t_{RWC}	ns	245		280		345		
Page mode cycle time	t_{PC}	ns	120		145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	0	50	
Transition time	t_T	ns	3	35	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		100		
$\overline{CAS}$ precharge time (Page cycle)	t_{CP}	ns	50		60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		0		
Row Address set-up time	t_{ASR}	ns	0		0		0		
Row Address hold time	t_{RAH}	ns	15		15		20		
Column Address set-up time	t_{ASC}	ns	0		0		0		
Column Address hold time	t_{CAH}	ns	20		20		25		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	80		95		125		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		−10		8
Write command hold time	t_{WCH}	ns	40		45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		155		
Write command pulse width	t_{WP}	ns	40		45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		55		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	40		45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		45		55		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		120		155		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	0		0		0		
$\overline{CAS}$ precharge time	t_{CPN}	ns	30		35		45		

NOTES:
1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the oata out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

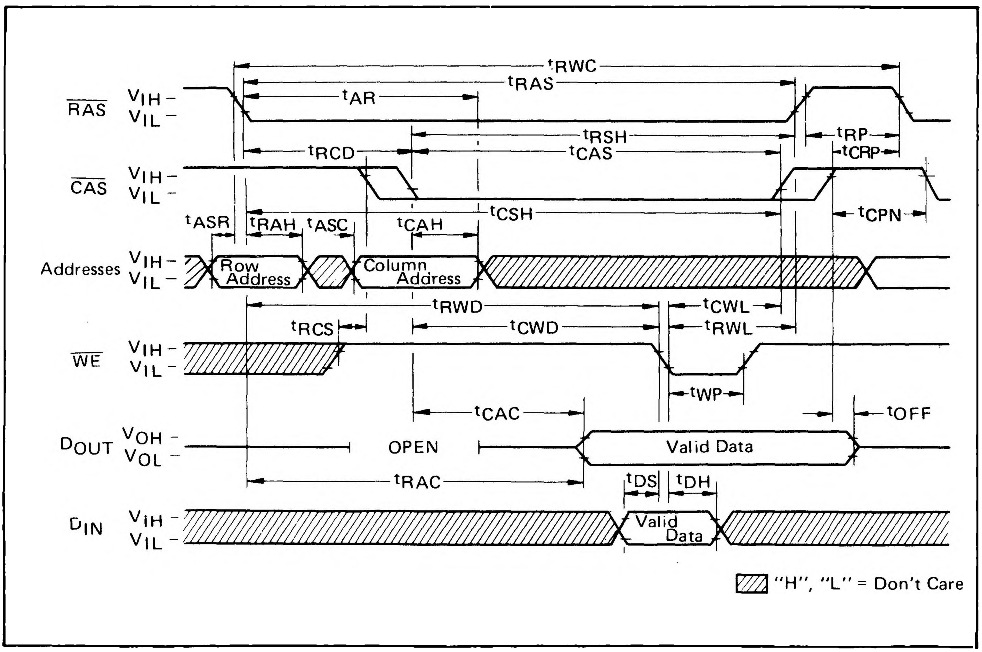
READ CYCLE TIMING



WRITE CYCLE TIMING
(EARLY WRITE)

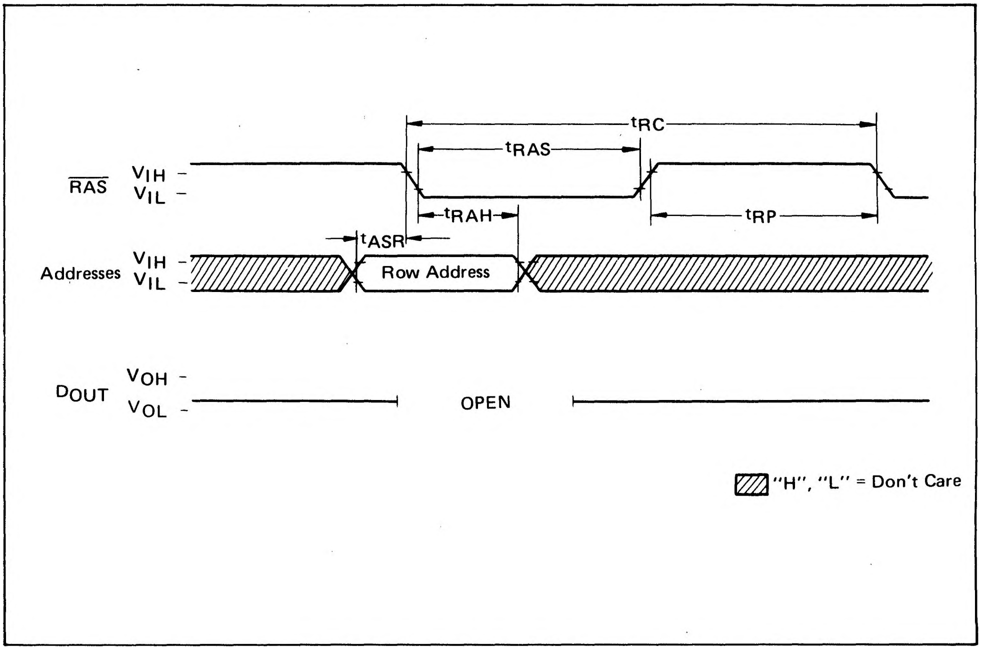


READ-WRITE/READ-MODIFY-WRITE CYCLE

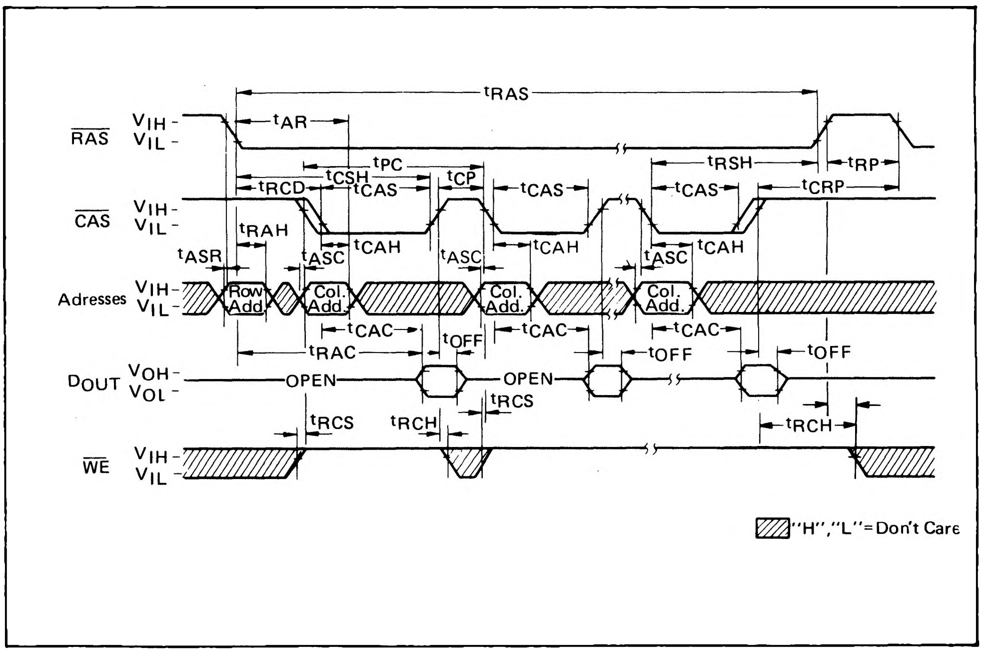


$\overline{RAS}$ ONLY REFRESH TIMING

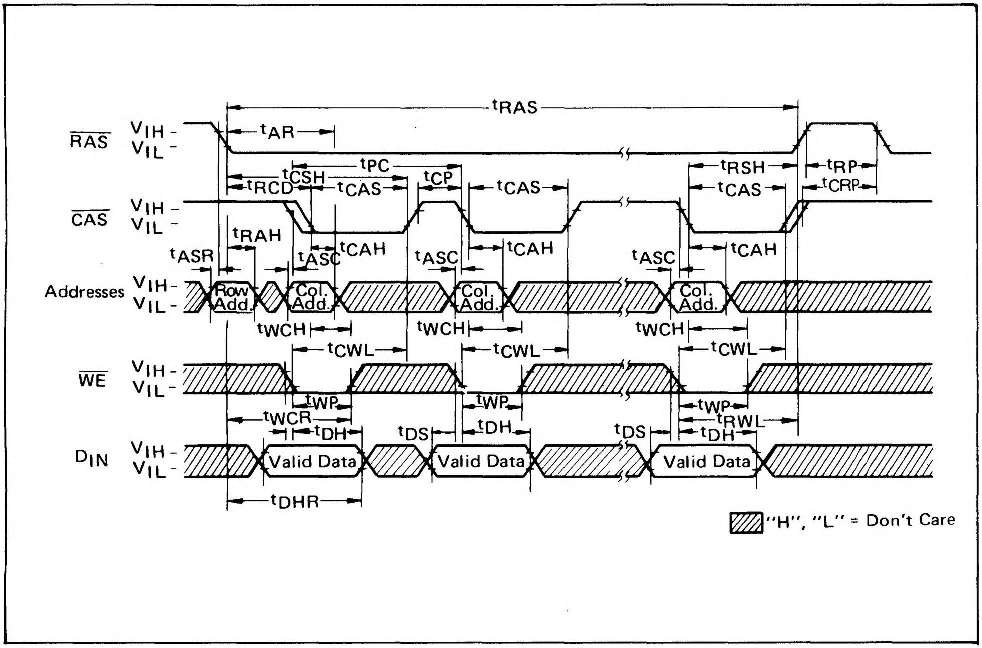
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & DIN: Don't care)



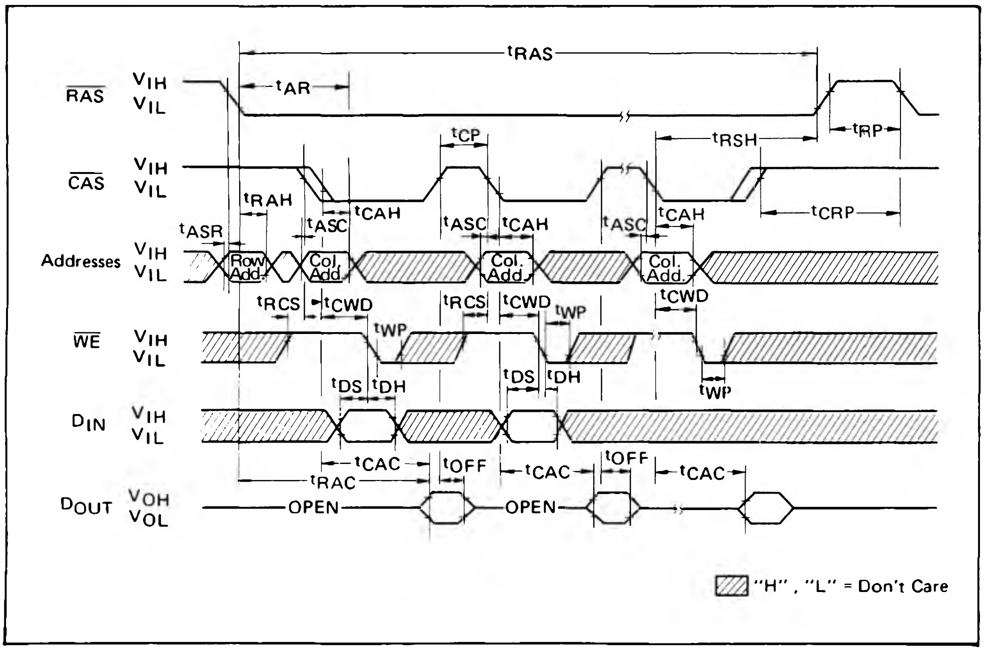
PAGE MODE READ CYCLE



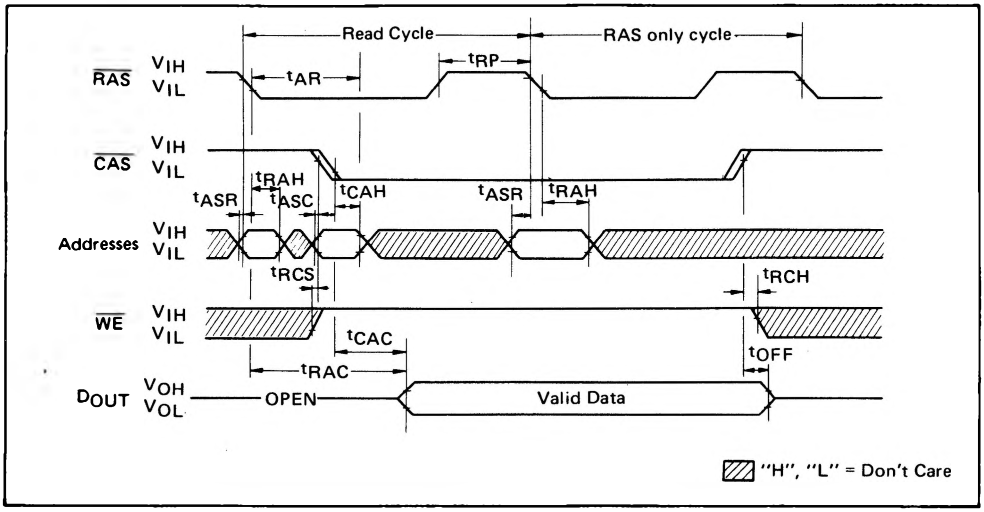
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764A. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

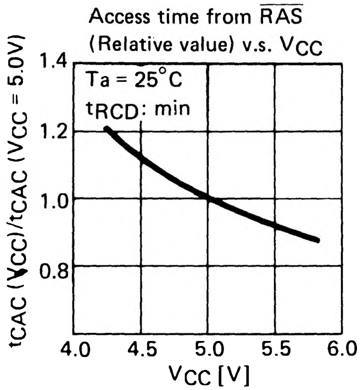
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

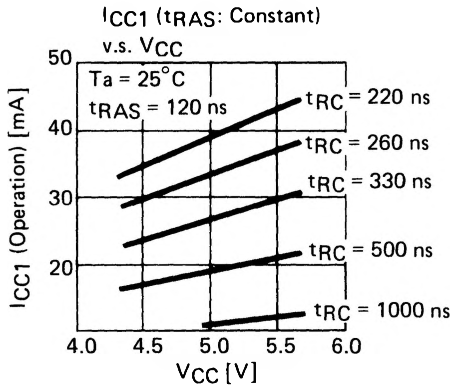
Hidden Refresh:

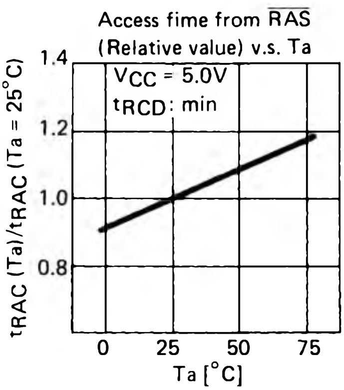
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

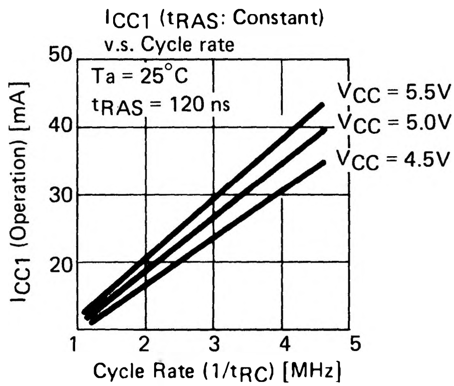
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

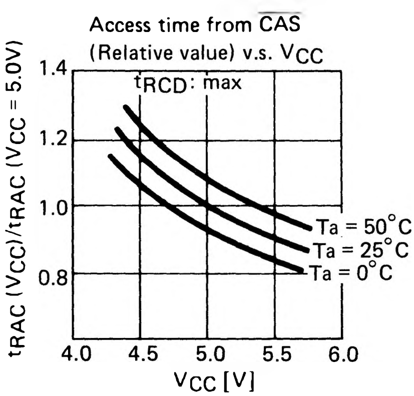
TYPICAL CHARACTERISTICS

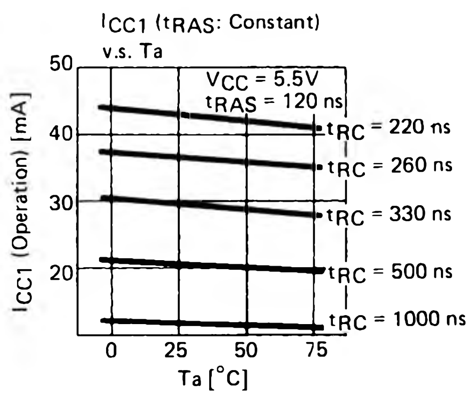


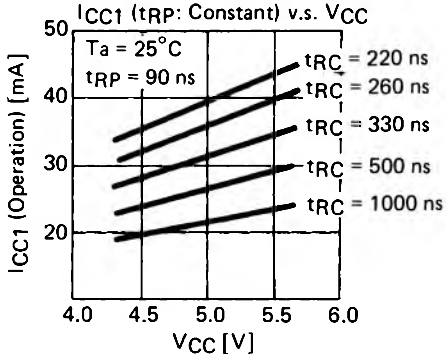


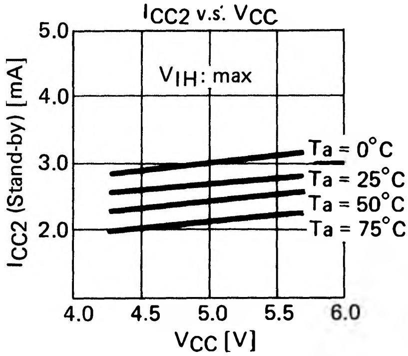


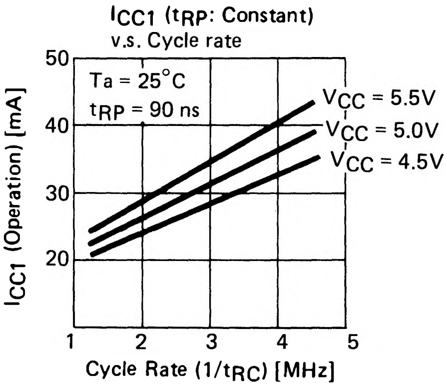


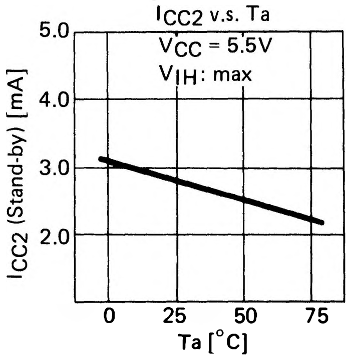


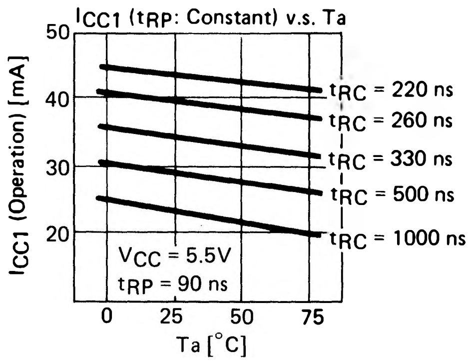



ICC1 (tRP: Constant) v.s. VCC
Ta = 25°C
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC1 (Operation) [mA]
50
40
30
20
4.0
4.5
5.0
5.5
6.0
VCC [V]

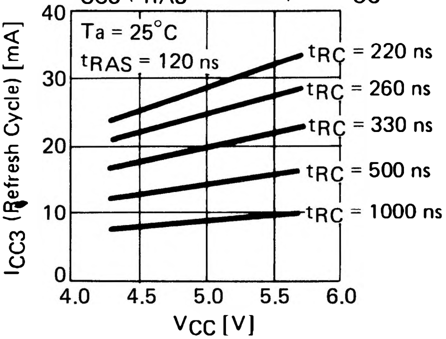

ICC2 v.s. VCC
VIH: max
Ta = 0°C
Ta = 25°C
Ta = 50°C
Ta = 75°C
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
4.0
4.5
5.0
5.5
6.0
VCC [V]


ICC1 (tRP: Constant)
v.s. Cycle rate
Ta = 25°C
tRP = 90 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC1 (Operation) [mA]
50
40
30
20
1
2
3
4
5
Cycle Rate (1/tRC) [MHz]

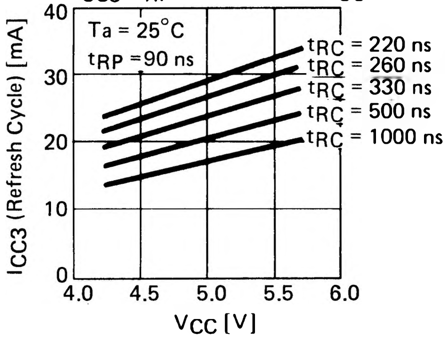

ICC2 v.s. Ta
VCC = 5.5V
VIH: max
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
0
25
50
75
Ta [°C]


ICC1 (tRP: Constant) v.s. Ta
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
VCC = 5.5V
tRP = 90 ns
ICC1 (Operation) [mA]
50
40
30
20
0
25
50
75
Ta [°C]

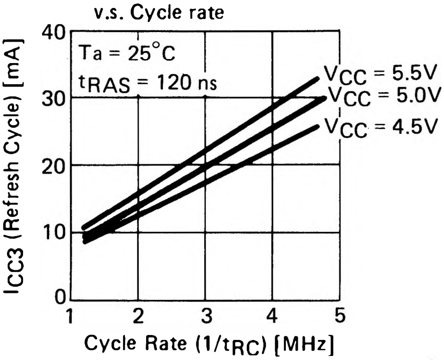
I_{CC3} (t_{RAS}: Constant) v.s. V_{CC}



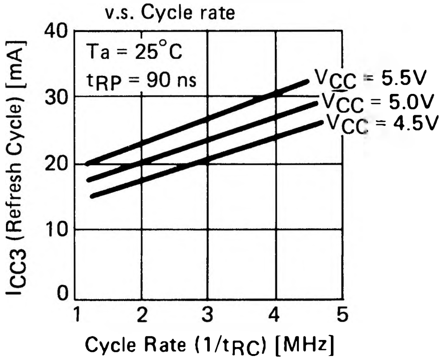
I_{CC3} (t_{RP}: Constant) v.s. V_{CC}



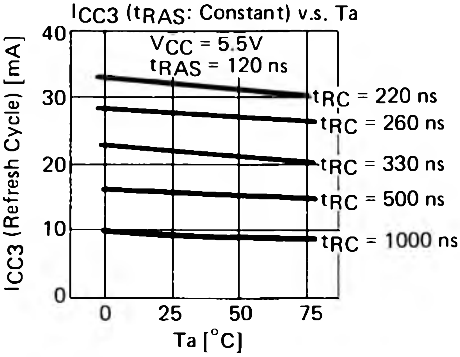
I_{CC3} (t_{RAS}: Constant)
v.s. Cycle rate



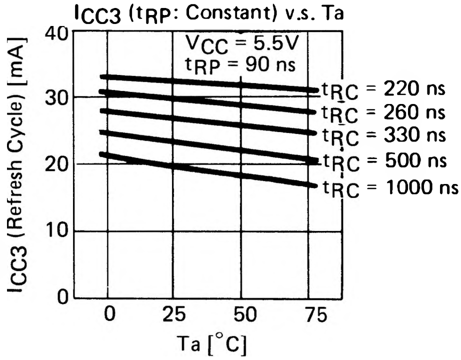
I_{CC3} (t_{RP}: Constant)
v.s. Cycle rate

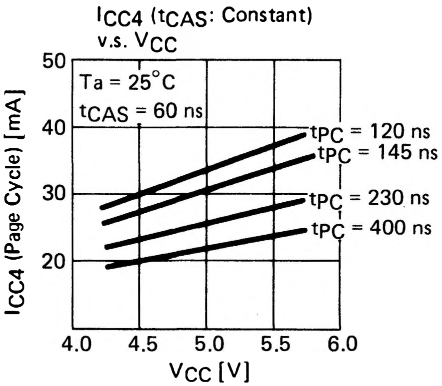


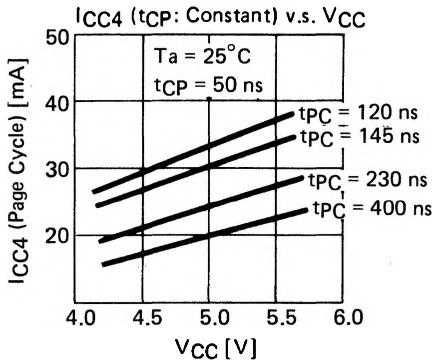
I_{CC3} (t_{RAS}: Constant) v.s. Ta

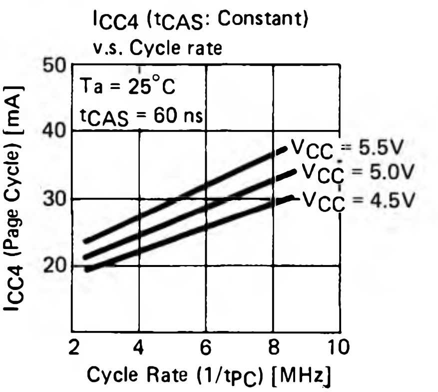


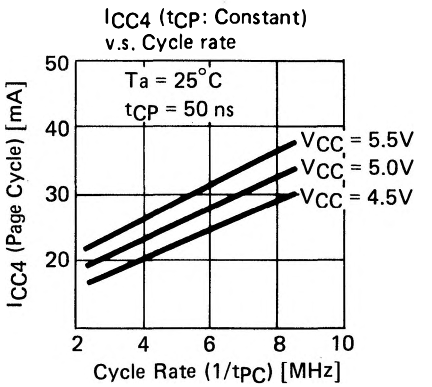
I_{CC3} (t_{RP}: Constant) v.s. Ta

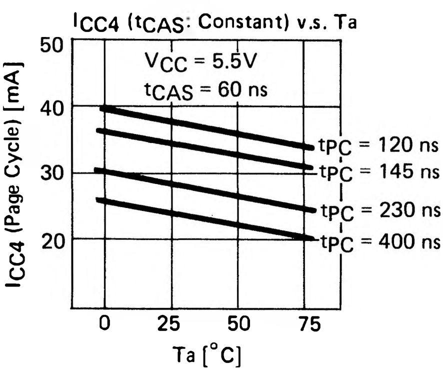


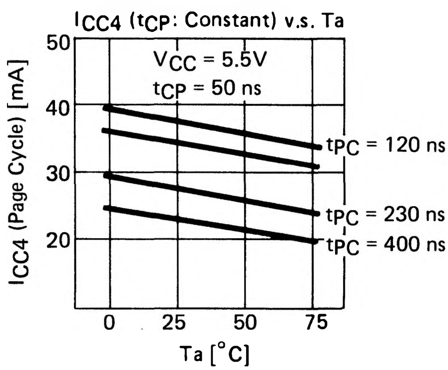

ICC4 (tCAS: Constant)
v.s. VCC
Ta = 25°C
tCAS = 60 ns
tPC = 120 ns
tPC = 145 ns
tPC = 230 ns
tPC = 400 ns
ICC4 (Page Cycle) [mA]
50
40
30
20
4.0
4.5
5.0
5.5
6.0
VCC [V]

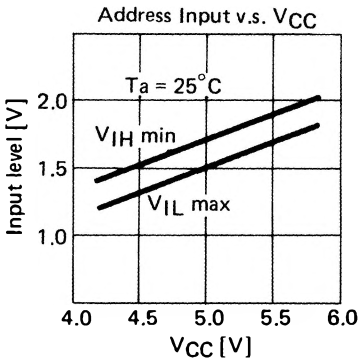

ICC4 (tCP: Constant) v.s. VCC
Ta = 25°C
tCP = 50 ns
tPC = 120 ns
tPC = 145 ns
tPC = 230 ns
tPC = 400 ns
ICC4 (Page Cycle) [mA]
50
40
30
20
4.0
4.5
5.0
5.5
6.0
VCC [V]

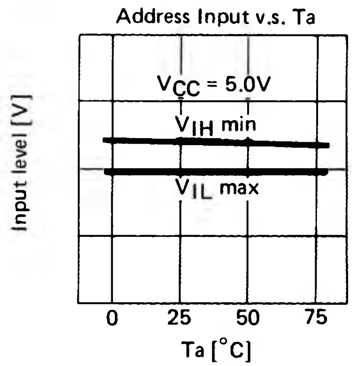

ICC4 (tCAS: Constant)
v.s. Cycle rate
Ta = 25°C
tCAS = 60 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC4 (Page Cycle) [mA]
50
40
30
20
2
4
6
8
10
Cycle Rate (1/tPC) [MHz]

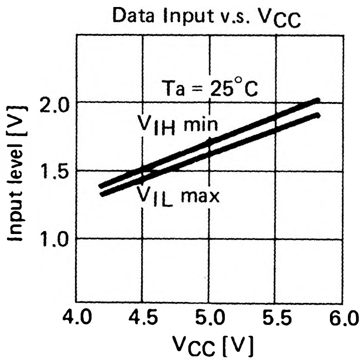

ICC4 (tCP: Constant)
v.s. Cycle rate
Ta = 25°C
tCP = 50 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC4 (Page Cycle) [mA]
50
40
30
20
2
4
6
8
10
Cycle Rate (1/tPC) [MHz]

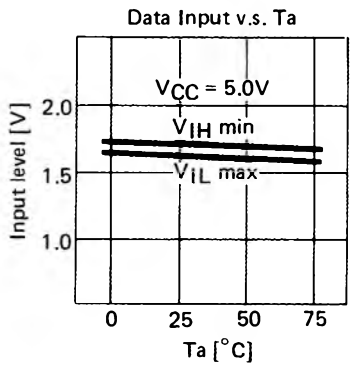

ICC4 (tCAS: Constant) v.s. Ta
VCC = 5.5V
tCAS = 60 ns
tPC = 120 ns
tPC = 145 ns
tPC = 230 ns
tPC = 400 ns
ICC4 (Page Cycle) [mA]
50
40
30
20
0
25
50
75
Ta [°C]

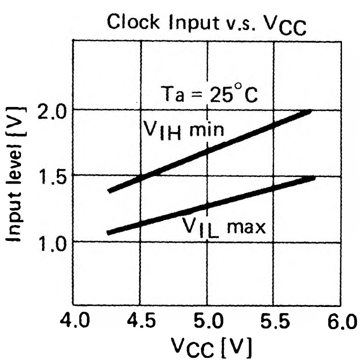

ICC4 (tCP: Constant) v.s. Ta
VCC = 5.5V
tCP = 50 ns
tPC = 120 ns
tPC = 230 ns
tPC = 400 ns
ICC4 (Page Cycle) [mA]
50
40
30
20
0
25
50
75
Ta [°C]

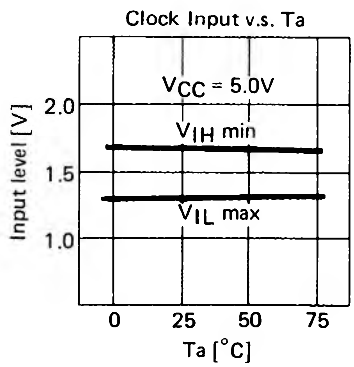

Address Input v.s. VCC
Ta = 25°C
VIH min
VIL max
Input level [V]
2.0
1.5
1.0
4.0
4.5
5.0
5.5
6.0
VCC [V]

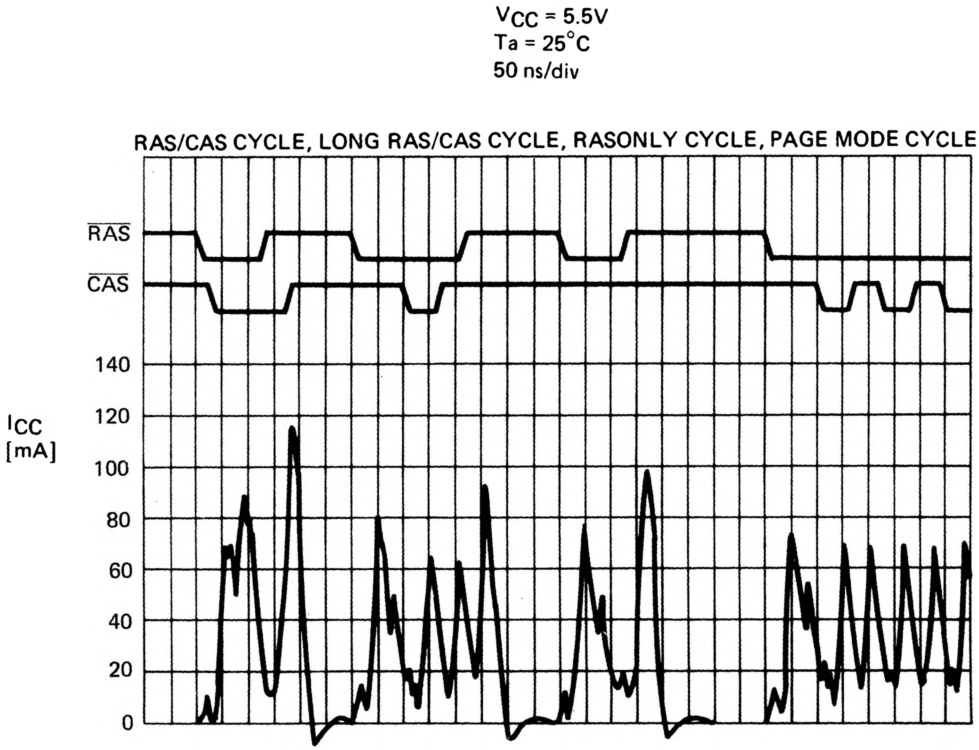

Address Input v.s. Ta
VCC = 5.0V
VIH min
VIL max
Input level [V]
0
25
50
75
Ta [°C]


Data Input v.s. VCC
Ta = 25°C
VIH min
VIL max
Input level [V]
2.0
1.5
1.0
4.0
4.5
5.0
5.5
6.0
VCC [V]


Data Input v.s. Ta
VCC = 5.0V
VIH min
VIL max
Input level [V]
2.0
1.5
1.0
0
25
50
75
Ta [°C]


Clock Input v.s. VCC
Ta = 25°C
VIH min
VIL max
Input level [V]
2.0
1.5
1.0
4.0
4.5
5.0
5.5
6.0
VCC [V]


Clock Input v.s. Ta
VCC = 5.0V
VIH min
VIL max
Input level [V]
2.0
1.5
1.0
0
25
50
75
Ta [°C]


V_{CC} = 5.5V
Ta = 25°C
50 ns/div
RAS/CAS CYCLE, LONG RAS/CAS CYCLE, RASONLY CYCLE, PAGE MODE CYCLE
$\overline{RAS}$
$\overline{CAS}$
I_{CC} [mA]
140
120
100
80
60
40
20
0

MSM3764A Bit MAP (Physical-Decimal)