OKI semiconductor

MSM2128-1AS

16,384-BIT (2048 x 8) STATIC RAM

GENERAL DESCRIPTION

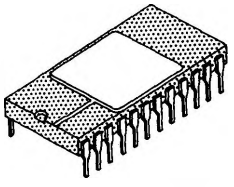
The Oki MSM2128-1 is a 16384-bit static Random Access Memory organized as 2048 words by 8 bits using Oki's Advanced N-channel Silicon Gate MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM2128-1 series is offered in an 24-pin dual-in-line ceramic (AS suffix) package. Operation is guaranteed from 0°C to 70°C.

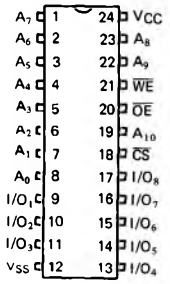
FEATURES

- Low Power Dissipation
- Single +5V Supply (±10% Tolerance)
- 2048-word x 8-bit Organization
- Fully Static Operation
- Common I/O Capability using Three-State Outputs
- Directly TTL Compatible
- Advanced N-channel Silicon Gate MOS Technology
- Pin compatible with MSM2716, 16,384 Bit UV Erasable PROM

	2128-1	2128-13
Max. Access Time (NS)	200	300
Max. Power Dissipation (MW)	800	800

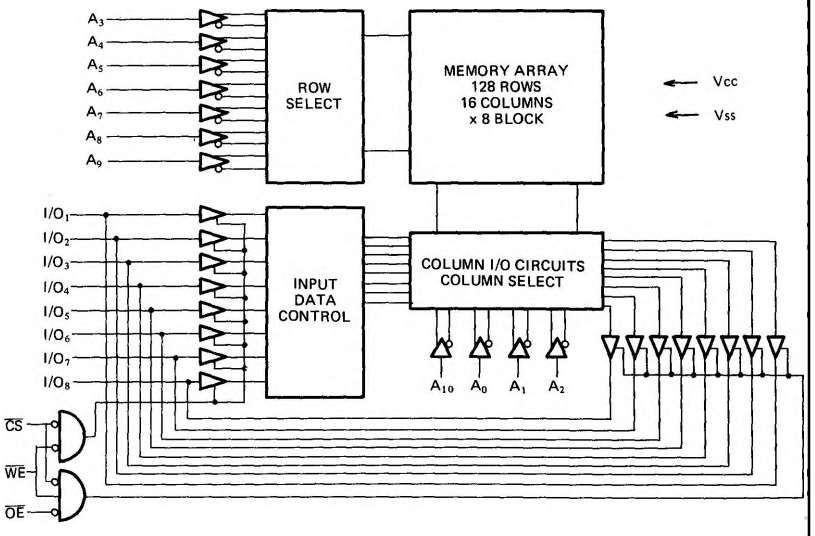


PIN CONFIGURATION



A_0~A_{10}: Address Inputs
I/O_1~I/O_8: Data Input/Output
V_{CC}: +5V Supply
V_{SS}: Ground
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$\overline{OE}$: Output Enable

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Temperature Under Bias	T_{op}	0 to + 70	°C	
Storage Temperature	T_{stg}	−55 to + 150	°C	
Supply Voltage	V_{CC}	−0.5 to + 7	V	Respect to V_{SS}
Input Voltage	V_{IN}	−0.5 to + 7	V	
Output Voltage	V_{OUT}	−0.5 to + 7	V	
Power Dissipation	P_D	1.0	W	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
Input Signal Level	V_{IH}	2.0	5	6.0	V	Respect to V_{SS}
	V_{IL}	−0.5	5	0.8	V	
Operating Temperature	Topr	0		+70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ±10%; Ta = 0°C to + 70°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}	−10		10	μA	V_{CC} = +5.5 V_{IN} = 0 to V_{CC}
I/O Leakage Current	I_{LO}	−10		10	μA	$\overline{CS}$ = $\overline{OE}$ = 2.4V V_{CC} = +5.5V V_{OUT} = 0 to V_{CC}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −1.0 mA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Power Supply Current	I_{CC}			145	mA	V_{CC} = +5.5V $I_{I/O}$ = 0 mA

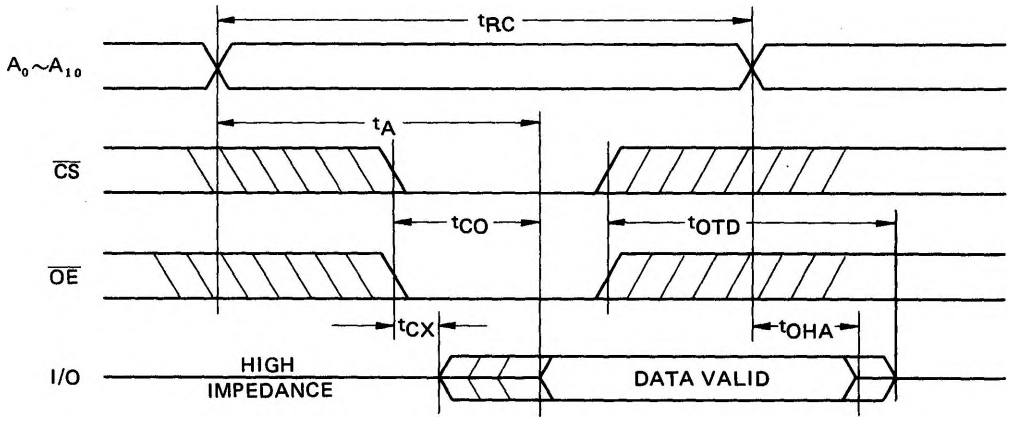
AC CHARACTERISTICS

READ CYCLE

(V_{CC} = 5V ±10%, Ta = 0°C to +70°C)

Parameter	Symbol	MSM2128−1		MSM2128−13		Unit
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	200		300		ns
Access Time	t_A		200		300	ns
Chip Selection to Output Valid	t_{CO}		70		100	ns
Chip Selection to Output Active	t_{CX}	10		10		ns
Output 3-State from Deselection	t_{OTD}		60		80	ns
Output Hold from Address Change	t_{OHA}	20		20		ns

READ CYCLE



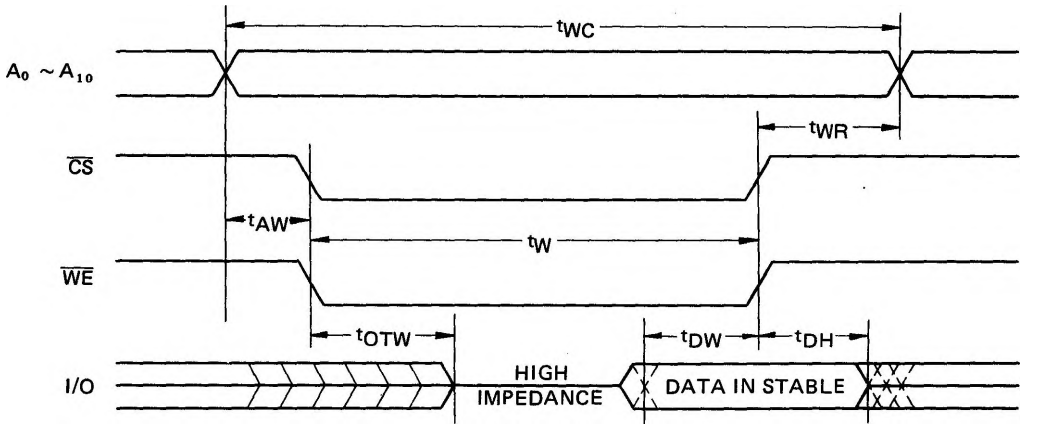
Notes:
1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CO} and t_{CX} are specified from $\overline{CS}$ or $\overline{CE}$, whichever occurs last.
3. t_{OTB} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OTD} and t_{OHA} are specified by the time when DATA OUT is floating.
5. Input Pulse Levels: 0.8V to +2.0V
6. Input Rise and Fall Time: 10 ns
7. Timing Measurements Reference Level: 1.5V
8. Output Load: 1 TTL Gate and C_L = 50 pF

WRITE CYCLE

(V_{CC} = 5V ±10%, Ta = 0°C to +70°C)

Parameter	Symbol	MSM2128-1AS		MSM2128-13AS		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		300		ns
Write Time	t_W	120		150		ns
Write Release Time	t_{WR}	20		30		ns
Output 3-State from Write	t_{OTW}		60		80	ns
Data to Write Time Overlap	t_{DW}	120		150		ns
Data Hold from Write Time	t_{DH}	0		0		ns
Address to Write Setup Time	t_{AW}	0		0		ns

WRITE CYCLE



Notes:
1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
2. OE may be both high and low in a Write Cycle.
3. t_{AW} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is a overlap time of a low $\overline{CS}$ and low $\overline{WE}$.
5. t_{WR}, t_{DW} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.
8. Input Pulse Levels: 0.8V to + 2.0V
9. Input Rise and Fall Time: 10 ns
10. Timing Measurements Reference Level: 1.5V

CAPACITANCE

(T_a = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$		4	6	pF
Input Capacitance	C_{IN}		4	6	pF

Note: This parameter is periodically sampled and not 100% tested.