MSC2304YS8/KS8

262,144 BY 8 BIT DYNAMIC RAM MODULE

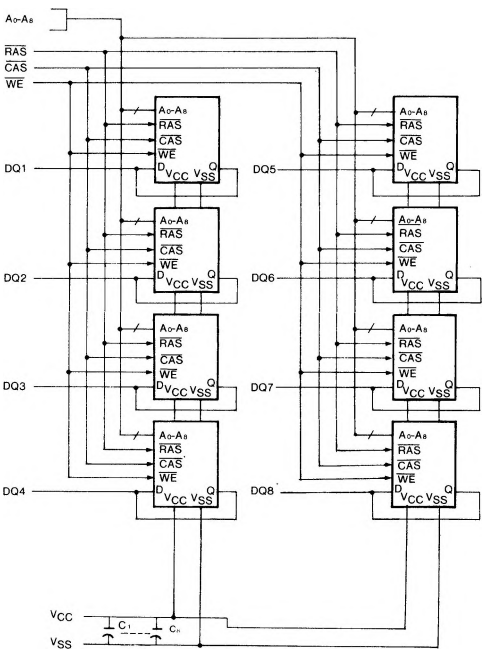
GENERAL DESCRIPTION

The Oki MSC2304YS8/KS8 is a fully decoded, 262,144 words × 8 bit NMOS dynamic random access memory composed of eight 256K DRAMs in plastic leaded chip carrier (MSM41256JS). The mounting of eight PLCCs together with eight 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS8/KS8 are quite same as the original MSM41256JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

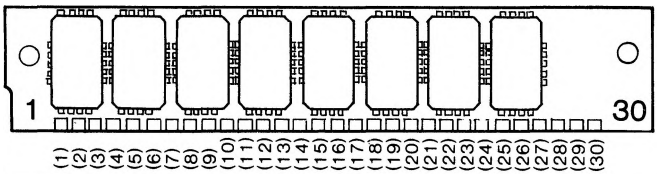
- 262,144 word × 8 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Row Access Time;
  120ns max. (MSC2304-12YS8/KS8)
  150ns max. (MSC2304-15YS8/KS8)
- Low Power Dissipation;
  3080mW max. (MSC2304-12YS8/KS8)
  2860mW max. (MSC2304-15YS8/KS8)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

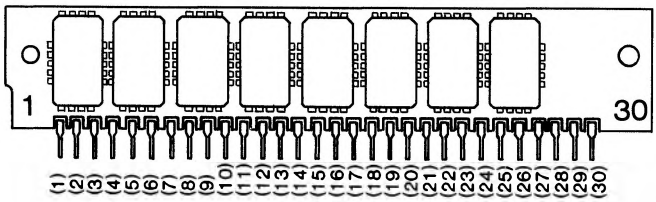


PIN ASSIGNMENT

MSC2304YS8



MSC2304KS8



PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	16	DQ5
2	$\overline{CAS}$	17	A8
3	DQ1	18	NC
4	A0	19	NC
5	A1	20	$\overline{DQ6}$
6	DQ2	21	$\overline{WE}$
7	A2	22	VSS
8	A3	23	DQ7
9	VSS	24	NC
10	DQ3	25	DQ8
11	A4	26	$\overline{NC}$
12	A5	27	$\overline{RAS}$
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	8	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; t_{RC} = min.)	I_{CC1}		560		520	mA
Standby Current Power supply current (RAS = CAS = V_{IH})	I_{CC2}		40		40	mA
Refresh Current Average power supply current (RAS cycling, CAS = V_{IH}; t_{RC} =min.)	I_{CC3}		440		400	mA
Page Mode Current* Average power supply current (RAS = V_{IL}, CAS cycling; t_{PC} =min.)	I_{CC4}		440		400	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−80	80	−80	80	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	37	60	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Parameter	Symbol	Units	MSC2304-12YS/KS		MSC2304-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	230		260		
Page mode cycle time	t_{PC}	ns	125		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	40	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time	t_{CP}	ns	55		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		

AC CHARACTERISTICS (CONT.)

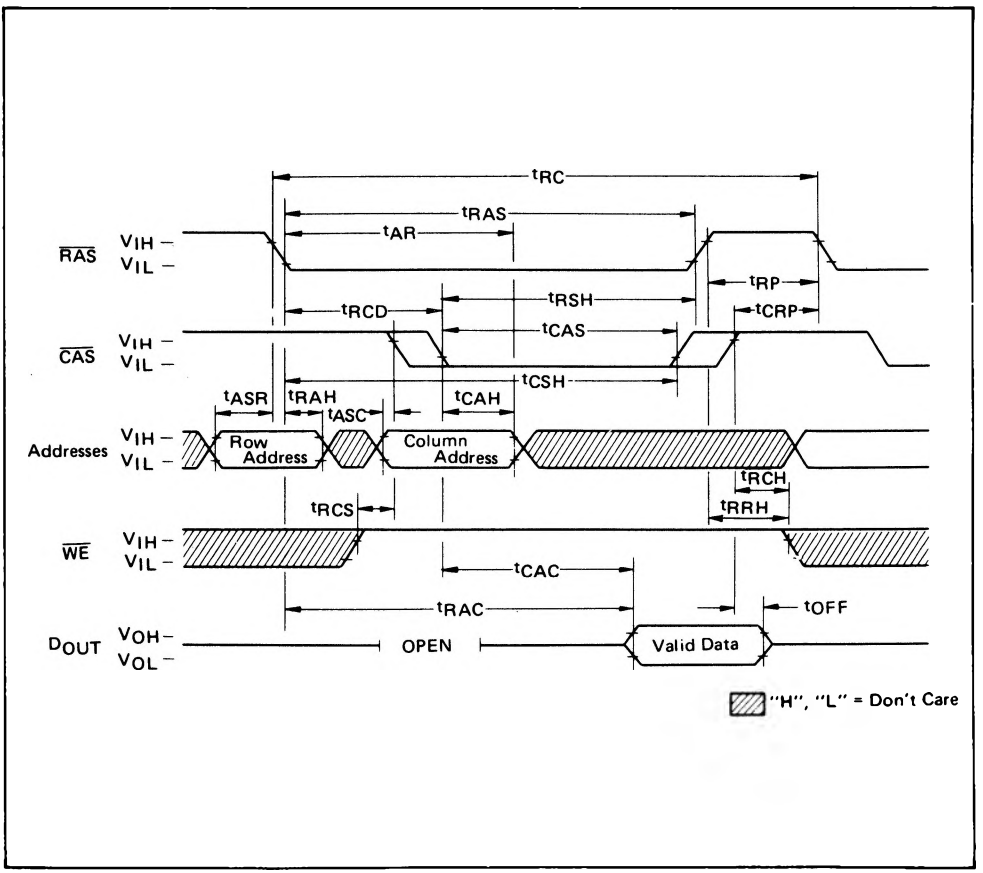
Parameter	Symbol	Units	MSC2304-12YS/KS		MSC2304-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	30		35		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	90		110		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	0		0		
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		

Note 1, 2, 3: Under recommended operating conditions

Notes:

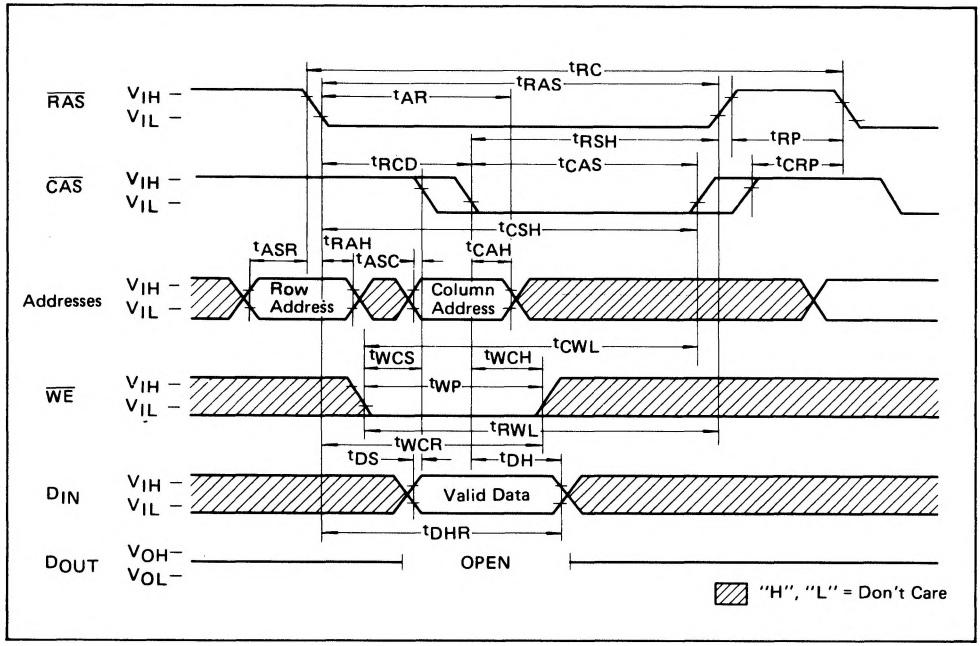
1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. AC measurements assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$ (Max.)
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5. Assumes that $t_{RCD} < t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.

READ CYCLE TIMING



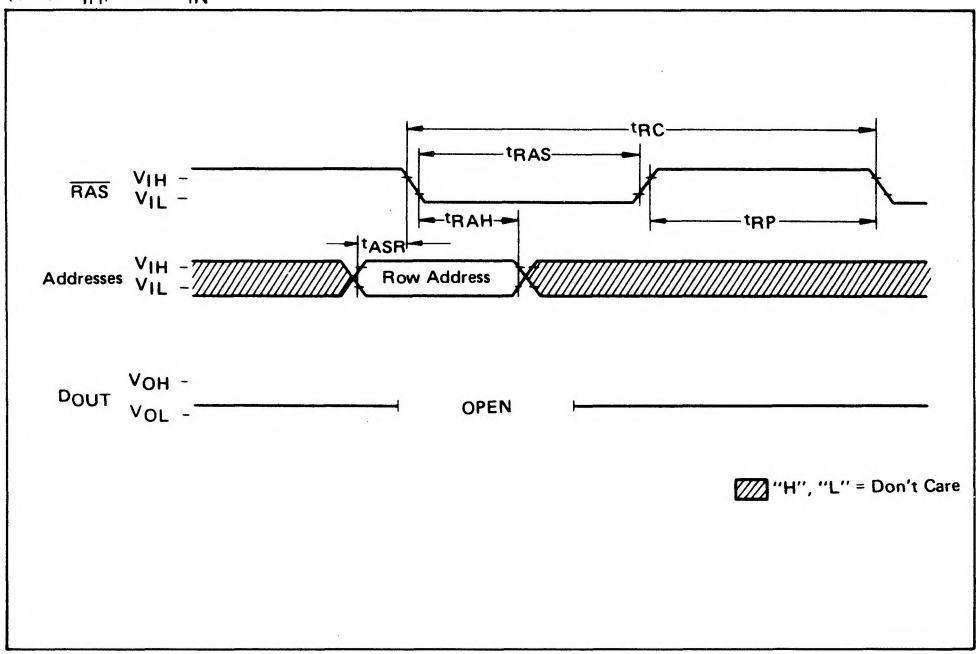
WRITE CYCLE TIMING

(EARLY WRITE)

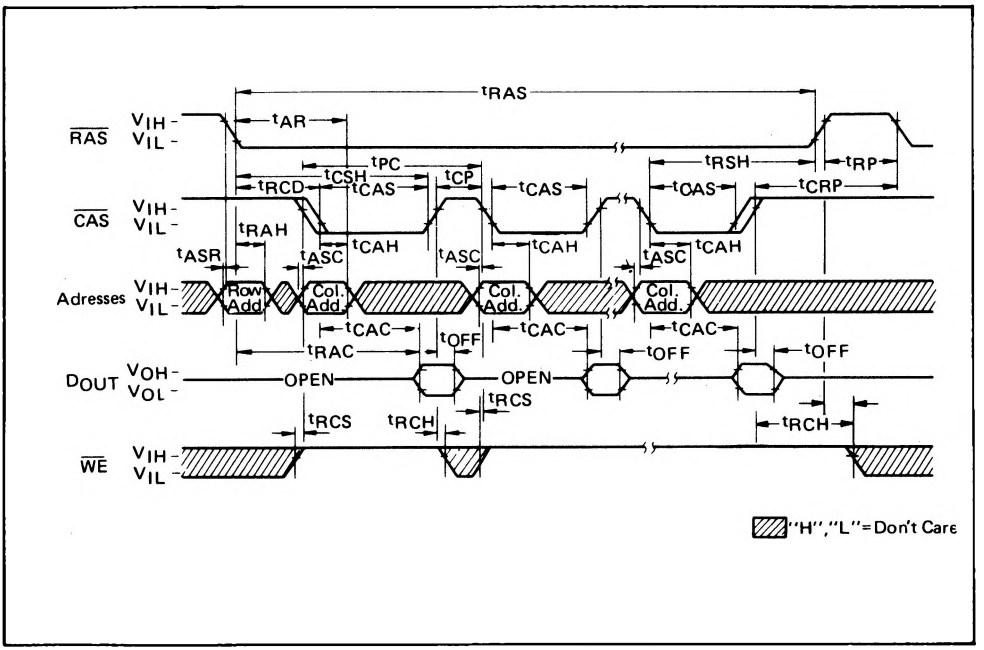


RAS ONLY REFRESH TIMING

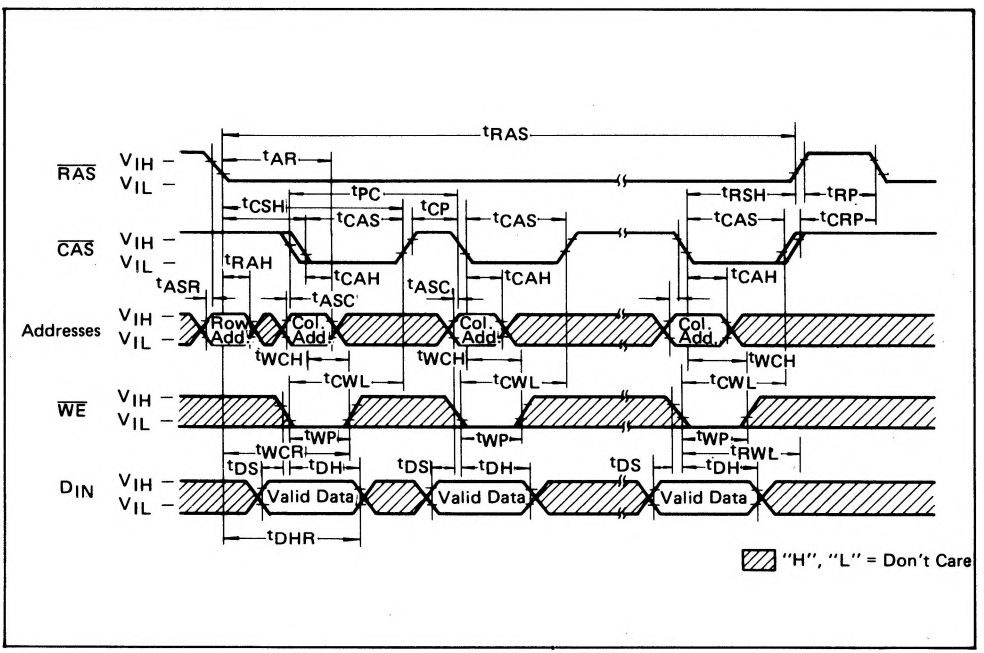
(CAS: V_{IH}, WE & D_{IN}: Don't care)



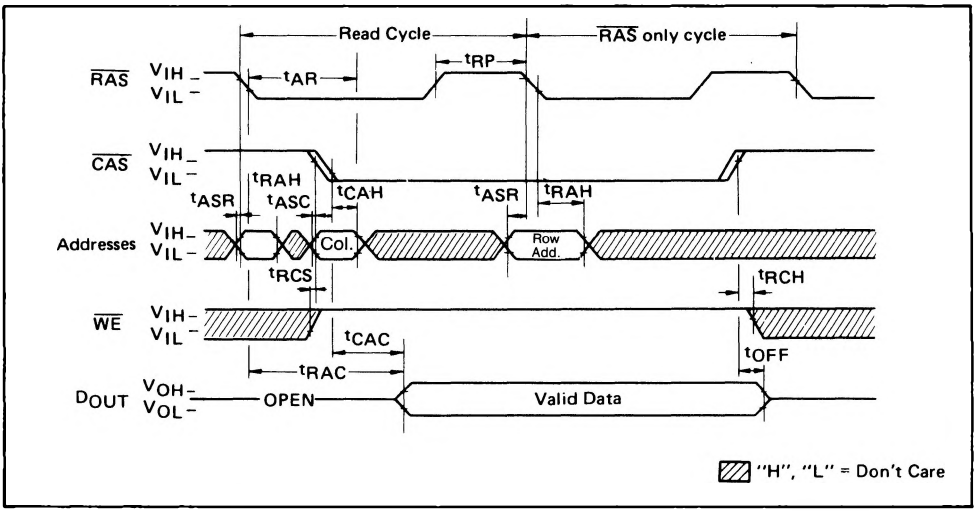
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSC2304. Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The Nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2304 during a write. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSC2304 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

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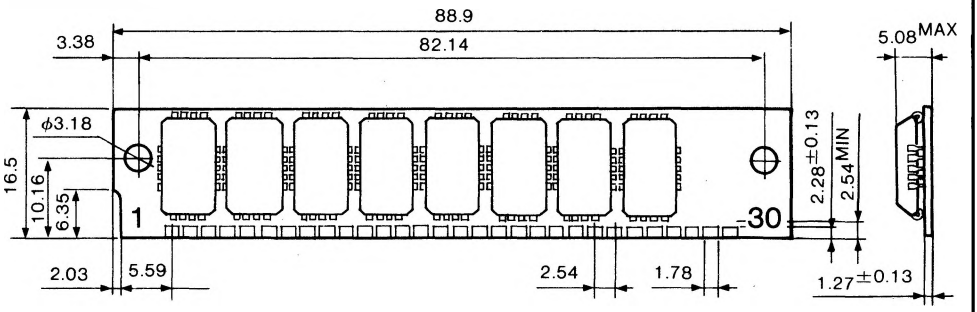

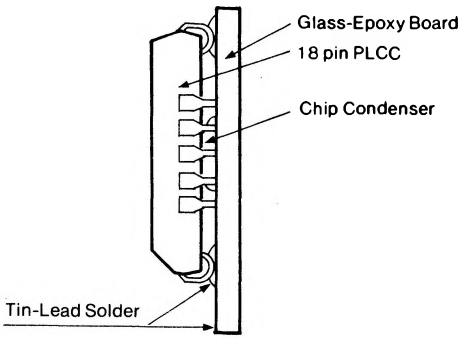

1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^{t})
4. Surface Coating: Photo Film Resist

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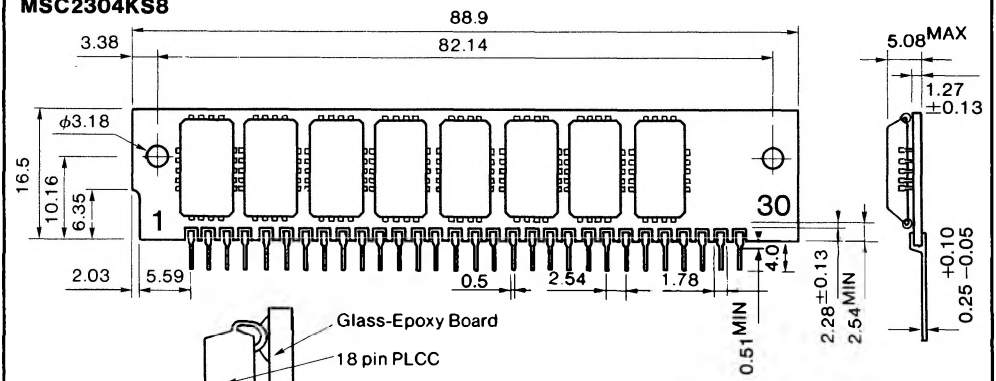

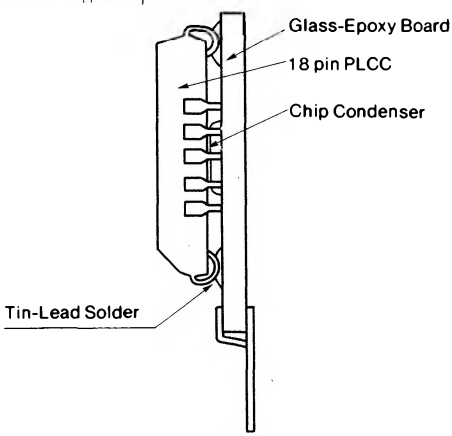

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4. Surface Coating: Photo Film Resist

MSC2304YS8/KS8 (SIP/SIM) DERATING CURVE