



# MP7545B

CMOS

Buffered Multiplying 12-Bit  
Digital-to-Analog Converter

## FEATURES

- Full Four Quadrant Multiplication
- 12-Bit Resolution
- Gain Error Tempco (2 ppm/°C max.)
- Latch-Up Free
- Single +5 V to +15 V Supply
- TTL/15 V CMOS Compatible
- Rugged 2000 V ESD Protection
- 3 V Version: MP75L45
- TTL/5 V VMOS Version: MP7645B

## APPLICATIONS

- Industrial Automation
- Automatic Test Equipment
- Disk Drive Servo Systems
- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratiometric A/D Conversion
- Function Generation
- Digitally Controlled Filters

## GENERAL DESCRIPTION

The MP7545B is a 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the  $\overline{CS}$  and  $\overline{WR}$

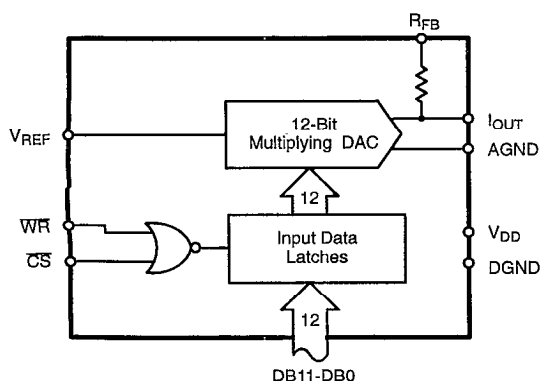
inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The MP7545B is particularly suitable for single supply operation and applications with wide temperature variations.

The MP7545B can be used with any supply voltage from +5 V to +15 V. With CMOS logic levels at the inputs the device dissipates less than 0.5 mW for  $V_{DD} = +5$  V.

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## SIMPLIFIED BLOCK DIAGRAM

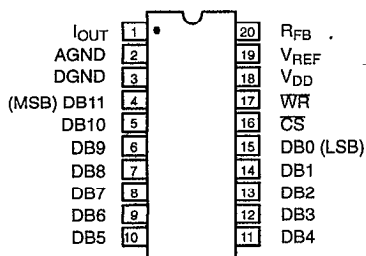


## ORDERING INFORMATION

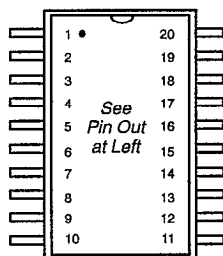
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	-40 to +85°C	MP7545BKN	±1	±1	±3
Plastic Dip	-40 to +85°C	MP7545BLN	±1/2	±1	±2
SOIC	-40 to +85°C	MP7545BKS	±1	±1	±3
SOIC	-40 to +85°C	MP7545BLS	±1/2	±1	±2
PLCC	-40 to +85°C	MP7545BKP	±1	±1	±3
PLCC	-40 to +85°C	MP7545BLP	±1/2	±1	±2

## PIN CONFIGURATIONS

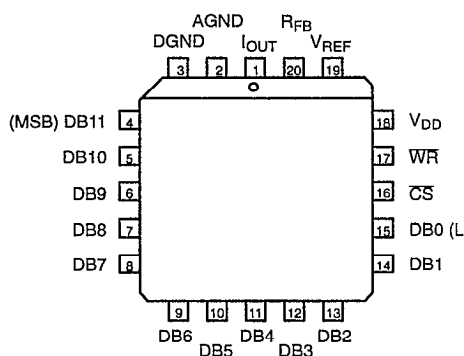
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")  
N20



20 Pin SOIC (Jedec, 0.300")  
S20



20 Pin PLCC  
P20

## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
1	I <sub>OUT</sub>	Output Current	11	DB4	Data Input Bit 4
2	AGND	Analog Ground	12	DB3	Data Input Bit 3
3	DGND	Digital Ground	13	DB2	Data Input Bit 2
4	DB11	Data Input Bit 11 (MSB)	14	DB1	Data Input Bit 1
5	DB10	Data Input Bit 10	15	DB0	Data Input Bit 0 (LSB)
6	DB9	Data Input Bit 9	16	CS	Chip Select (Active Low)
7	DB8	Data Input Bit 8	17	WR	Write (Active Low)
8	DB7	Data Input Bit 7	18	V <sub>DD</sub>	Digital Supply Voltage
9	DB6	Data Input Bit 6	19	V <sub>REF</sub>	Reference Input
10	DB5	Data Input Bit 5	20	R <sub>FB</sub>	Feedback Resistor

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = + 5 V, V<sub>REF</sub> = +10 V unless otherwise noted)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
STATIC PERFORMANCE <sup>1</sup>								
Resolution (All Grades)	N	12			12		Bits	End Point Linearity
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K				±1		±1		
L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	Using Internal R <sub>FB</sub>
K				±1		±1		
L				±1		±1		
Gain Error	GE						LSB	
K				±3		±4		ΔGain/ΔTemperature
L				±2		±3		
Gain Temperature Coefficient <sup>2</sup>	TC <sub>GE</sub>					±2	ppm/°C	
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	
Output Leakage Current K, L	I <sub>OUT</sub>			±10		±50	nA	ΔGain/ΔV <sub>DD</sub>   ΔV <sub>DD</sub> = ± 5%
DYNAMIC PERFORMANCE <sup>2</sup>								
Current Settling Time	t <sub>S</sub>			1		1	μs	R <sub>L</sub> =100Ω, C <sub>L</sub> =13pF Full Scale Change to 1/2 LSB V <sub>REF</sub> = 10kHz, 20 Vp-p sinewave. From 50% of digital input to 90% of final analog output current
AC Feedthrough at I <sub>OUT</sub>	F <sub>T</sub>		5				mV p-p	
Propagation Delay	t <sub>PD</sub>		50				ns	
REFERENCE INPUT								
Input Resistance	R <sub>IN</sub>	7		25	7	25	kΩ	
DIGITAL INPUTS <sup>3</sup>								
Logical "1" Voltage	V <sub>IH</sub>	2.4			2.4		V	
Logical "0" Voltage	V <sub>IL</sub>			0.8		0.8	V	
Input Leakage Current	I <sub>LKG</sub>			±1		±10	μA	
Input Capacitance <sup>2</sup>								
Data	C <sub>IN</sub>			5		5	pF	
Control	C <sub>IN</sub>			20		20	pF	
ANALOG OUTPUTS								
Output Capacitance <sup>2</sup>								DAC Inputs all 1's DAC Inputs all 0's
	C <sub>OUT</sub>		100				pF	
	C <sub>OUT</sub>		50				pF	

## ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY <sup>5</sup>								
Functional Voltage Range	V <sub>DD</sub>	5		15	5	15	V	All digital inputs = 0 V or V <sub>DD</sub>
Supply Current	I <sub>DD</sub>			1		1	mA	
SWITCHING CHARACTERISTICS <sup>2, 4</sup>								
Chip Select to Write Set-Up Time	t <sub>CS</sub>	100					ns	
Chip Select to Write Hold Time	t <sub>CH</sub>	0					ns	
Data Valid to Write Set-Up Time	t <sub>DS</sub>	100					ns	
Data Valid to Write Hold Time	t <sub>DH</sub>	10					ns	
Write Pulse Width	t <sub>WR</sub>	100					ns	

## NOTES:

- 1 Full Scale Range (FSR) is 10V for unipolar mode.
- 2 Guaranteed but not production tested.
- 3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 See timing diagram.
- 5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

**ELECTRICAL CHARACTERISTICS**

(V<sub>DD</sub> = + 15 V, V<sub>REF</sub> = +10 V unless otherwise noted)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
<b>STATIC PERFORMANCE<sup>1</sup></b>								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K				±1		±1		
L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
K				±1		±1		
L				±1		±1		
Gain Error	GE						LSB	Using Internal R <sub>FB</sub>
K				±6		±7		
L				±5		±6		
Gain Temperature Coefficient <sup>2</sup>	TC <sub>GE</sub>					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	ΔGain/ΔV <sub>DD</sub>   ΔV <sub>DD</sub> = ± 5%
Output Leakage Current K, L	I <sub>OUT</sub>			±10		±50	nA	
<b>DYNAMIC PERFORMANCE<sup>2</sup></b>								
Current Settling Time	t <sub>S</sub>			1		1	μs	R <sub>L</sub> =100Ω, C <sub>L</sub> =13pF
AC Feedthrough at I <sub>OUT</sub>	F <sub>T</sub>		5				mV p-p	Full Scale Change to 1/2 LSB
Propagation Delay	t <sub>PD</sub>		50				ns	V <sub>REF</sub> = 10kHz, 20 Vp-p sinewave. From 50% of digital input to 90% of final analog output current
<b>REFERENCE INPUT</b>								
Input Resistance	R <sub>IN</sub>	7		25	7	25	kΩ	
<b>DIGITAL INPUTS<sup>3</sup></b>								
Logical "1" Voltage	V <sub>IH</sub>	13.5			13.5		V	
Logical "0" Voltage	V <sub>IL</sub>			1.5		1.5	V	
Input Leakage Current	I <sub>LKG</sub>			±1		±10	μA	V <sub>IN</sub> = 0 or V <sub>DD</sub>
Input Capacitance <sup>2</sup>								
DB0-DB11	C <sub>IN</sub>			5		5	pF	V <sub>IN</sub> = 0
WR, CS	C <sub>IN</sub>			20		20	pF	V <sub>IN</sub> = 0
<b>ANALOG OUTPUTS</b>								
Output Capacitance <sup>2</sup>								
	C <sub>OUT</sub>		100				pF	DAC Inputs all 1's
	C <sub>OUT</sub>		50				pF	DAC Inputs all 0's

## ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
POWER SUPPLY <sup>5</sup>								
Functional Voltage Range	V <sub>DD</sub>	5		15	5	15	V	All digital inputs = 0 or V <sub>DD</sub>
Supply Current	I <sub>DD</sub>			1		1	mA	
SWITCHING CHARACTERISTICS <sup>2, 4</sup>								
Chip Select to Write Set-Up Time	t <sub>CS</sub>	75					ns	
Chip Select to Write Hold Time	t <sub>CH</sub>	0					ns	
Data Valid to Write Set-Up Time	t <sub>DS</sub>	100					ns	
Data Valid to Write Hold Time	t <sub>DH</sub>	10					ns	
Write Pulse Width	t <sub>WR</sub>	75					ns	

## NOTES:

- 1 Full Scale Range (FSR) is 10V for unipolar mode and  $\pm 10V$  for bipolar.
- 2 Guaranteed but not production tested.
- 3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 See timing diagram.
- 5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

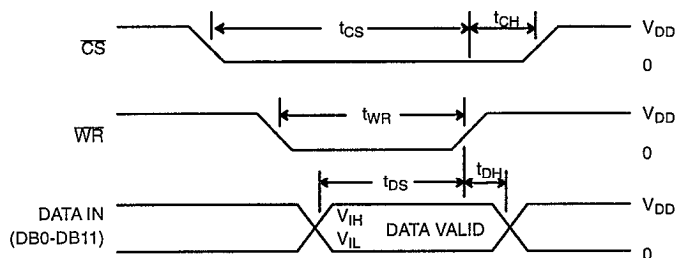
ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25°C unless otherwise noted)<sup>1, 2, 3</sup>

V <sub>DD</sub> to GND	0 to +17 V	Storage Temperature	-65°C to +150°C
Digital Input Voltage to GND	GND -0.5 to V <sub>DD</sub> +0.5 V	Lead Temperature (Soldering, 10 seconds)	+300°C
I <sub>OUT1</sub> , I <sub>OUT2</sub> to GND	GND -0.5 to V <sub>DD</sub> +0.5 V	Package Power Dissipation Rating to 75°C	
V <sub>REF</sub> to GND	$\pm 25$ V	PDIP, SOIC, PLCC	900mW
V <sub>RFB</sub> to GND	$\pm 25$ V	Derates above 75°C	12mW/°C
AGND to DGND	$\pm 0.5$ V		

## NOTES:

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100 $\mu$ s.
- 3 GND refers to AGND and DGND.

## WRITE CYCLE TIMING DIAGRAM



## APPLICATION NOTES

Refer to Section 8 for Applications Information

## Digital Section

Figure 2. shows the digital structure for one bit.

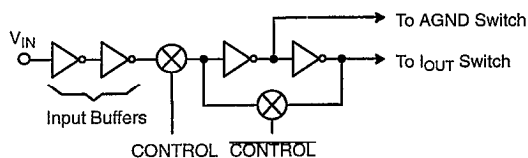


Figure 1. Digital Input Structure

The digital signals CONTROL and  $\overline{\text{CONTROL}}$  are generated from  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$ .

The input buffers are simple CMOS inverters designed such that when the MP7545B is operated with  $V_{DD} = 5\text{ V}$ , the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When  $V_{IN}$  is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails ( $V_{DD}$  and DGND) as is practically possible.

The MP7545B may be operated with any supply voltage in the range  $5 \leq V_{DD} \leq 15$  volts. With  $V_{DD} = +15\text{ V}$  the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

## MICROPROCESSOR INTERFACING OF THE MP7545B

The MP7545B can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 3. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

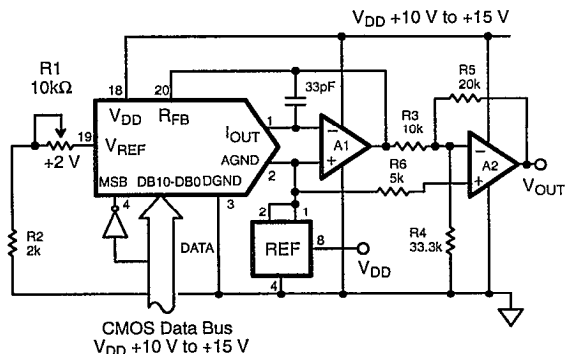


Figure 2. Single Supply "Bipolar" 2's Complement D/A Converter

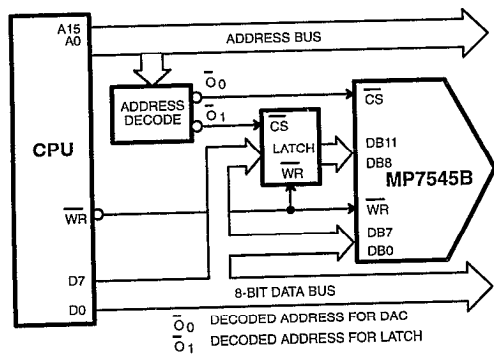


Figure 3. 8-Bit Processor to MP7545B Interface

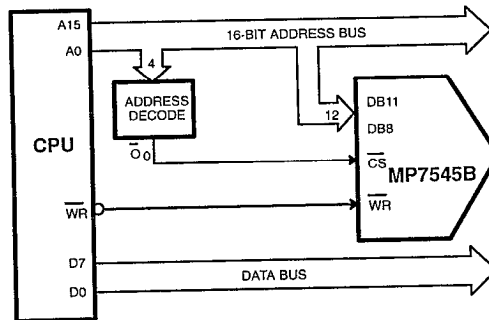
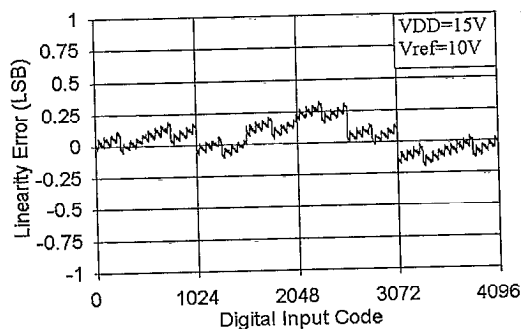


Figure 4. Connecting the MP7545B to 8-Bit Processors via the Address Bus

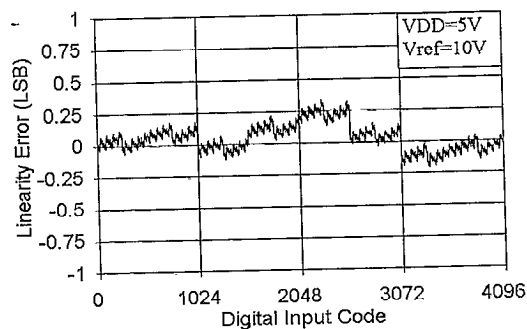
Figure 4. shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bush such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each MP7545B connected in this way uses 4k bytes of ad-

dress locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

## PERFORMANCE CHARACTERISTICS



Graph 1. Linearity Error vs. Digital Input Code



Graph 2. Linearity Error vs. Digital Input Code

## APPLICATION NOTES

Refer to Section 8 for Applications Information

Rev. 2.00

TQM™