

MM74C945, MM74C947 4-Digit Up/Down Counter/Latch/Decoder Driver

General Description

The MM74C943, MM74C947 are 4-digit counters for directly driving LCD displays. The MM74C945 contains a 4-decade up/down counter, output latches, counter/latch select multiplexer and 7-segment decoders. Also included are the backplane oscillator/driver, segment drivers and display blanking circuitry.

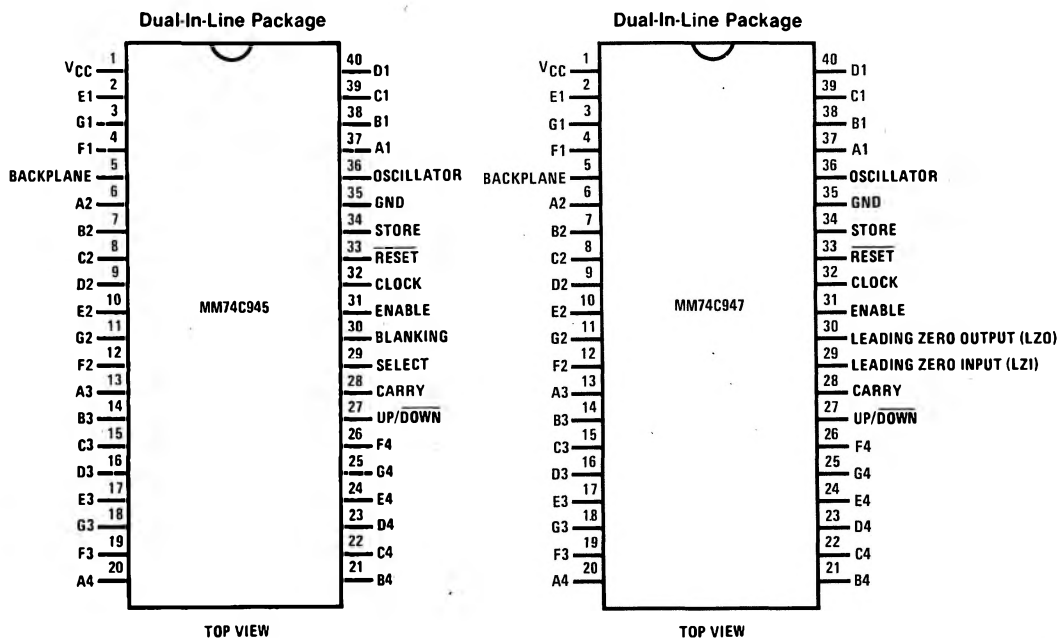
The MM74C947 differs from the MM74C945 in that it has no counter/latch multiplexer, but provides true leading zero blanking. All leading zeroes are automatically blanked except the least significant digit, which can be optionally blanked.

Both devices provide 28-segment outputs to drive a 4-digit display. Segment and backplane waveforms are generated internally, but can also be slaved to an external signal. This facilitates cascading of multiple displays.

Features

- 4-decade up/down count
- Direct 4-digit drive for high contrast and long display life
- Carry/borrow out for cascading counters
- Schmitt trigger clock input
- MM74C945 has display select to allow viewing of counter or latch
- Store and reset inputs allow operation as frequency or period counter
- MM74C947 has true ripple blanking; least significant digit may be optionally blanked

Connection Diagrams



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$	Package Dissipation	500 mW
Operating Temperature Range MM74C945/MM74C947	-40°C to +85°C	Operating V_{CC} Range	3.0V to 6.0V
Storage Temperature Range	-65°C to +150°C	Absolute Maximum V_{CC}	6.5V
		Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	$V_{CC} = 5V$		3.3		V
V_{T-} Negative Going Threshold Voltage (Clock Only)	$V_{CC} = 5V$		1.8		V
Hysteresis ($V_{T+} - V_{T-}$) (Clock Only)	$V_{CC} = 5V$		1.5		V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Inputs Except Clock)	$V_{CC} = 5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Inputs Except Clock)	$V_{CC} = 5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 5V, I_O = -10 \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 5V, I_O = +10 \mu A$			0.5	V
Logical "1" Input Current ($I_{IN(1)}$) (Note 2)	$V_{CC} = 5V, V_{IN} = 5V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$) (Note 2)	$V_{CC} = 5V, V_{IN} = 0V$	-1.0	-0.005		μA
Oscillator Input Current (I_{OSL})	$V_{CC} = 5V, V_{IN} = 0V/5V$		± 2		μA
Supply Current (I_{CC}) (Note 3)	$V_{CC} = 5V, V_{IN} = 0V/5V$		10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) (Clock Input)	$V_{CC} = 5V$	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$) (Clock Input)	$V_{CC} = 5V$			0.7	V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Inputs Except Clock)	$V_{CC} = 5V$	$V_{CC} - 1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Inputs Except Clock)	$V_{CC} = 5V$			0.4	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT DRIVE					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC} = 5V$ $T_A = 25^\circ C$		2.6		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC} = 5V$ $T_A = 25^\circ C$		2.8		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC} = 5V$ $T_A = 25^\circ C$		1.9		mA
Output Sink Current (I_{SINK}) (Segment Output)	$V_{CC} = 5V$ $T_A = 25^\circ C$		1.6		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC} = 5V$ $T_A = 25^\circ C$		16.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC} = 5V$ $T_A = 25^\circ C$		13.0		mA

AC Electrical Characteristics $T_j = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified.

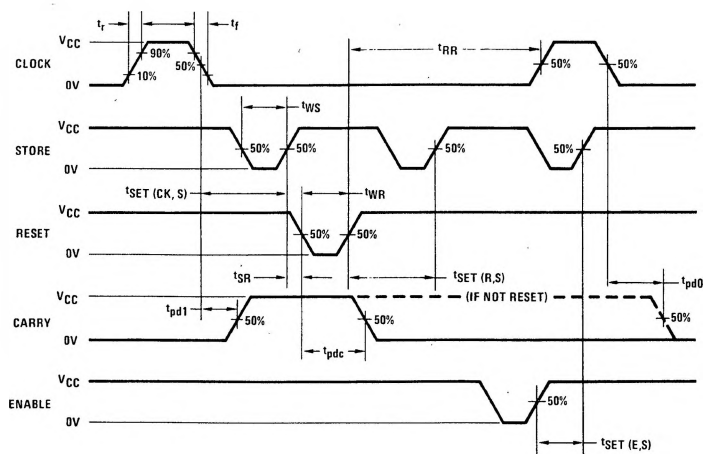
	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry					
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\text{V}$		2		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0\text{V}$			No Limit	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0\text{V}$				ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0\text{V}$				ns
$t_{\text{SET(CK, S)}}$	Clock to Store Set-Up Time	$V_{CC} = 5.0\text{V}$				ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0\text{V}$				ns
$t_{\text{SET(R, S)}}$	Reset to Store Set-Up Time	$V_{CC} = 5.0\text{V}$				ns
$t_{\text{SET(E, S)}}$	Enable to Store Set-Up Time	$V_{CC} = 5.0\text{V}$				ns
t_{RR}	Reset Removal	$V_{CC} = 5.0\text{V}$				ns
t_{pdc}	Propagation Delay Reset to Carry	$V_{CC} = 5.0\text{V}$				ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating		125		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 2)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{\text{load}} = 200\text{ pF}$		0.5		μs
t_{rtb}	Backplane Rise/Fall Time	$C_{\text{load}} = 5000\text{ pF}$		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating		16		kHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

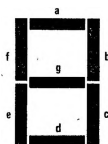
Note 2: Does not apply to backplane and oscillator pins.

Note 3: Display blanked. See test circuit.

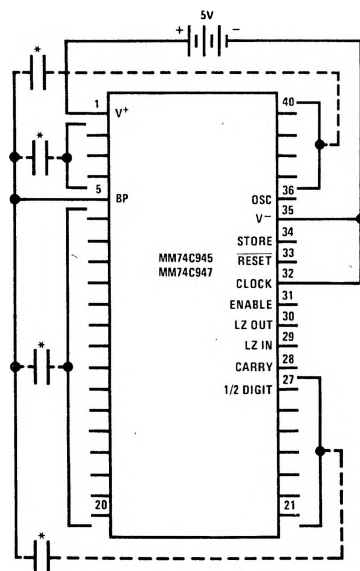
AC Waveforms



Segment Identification

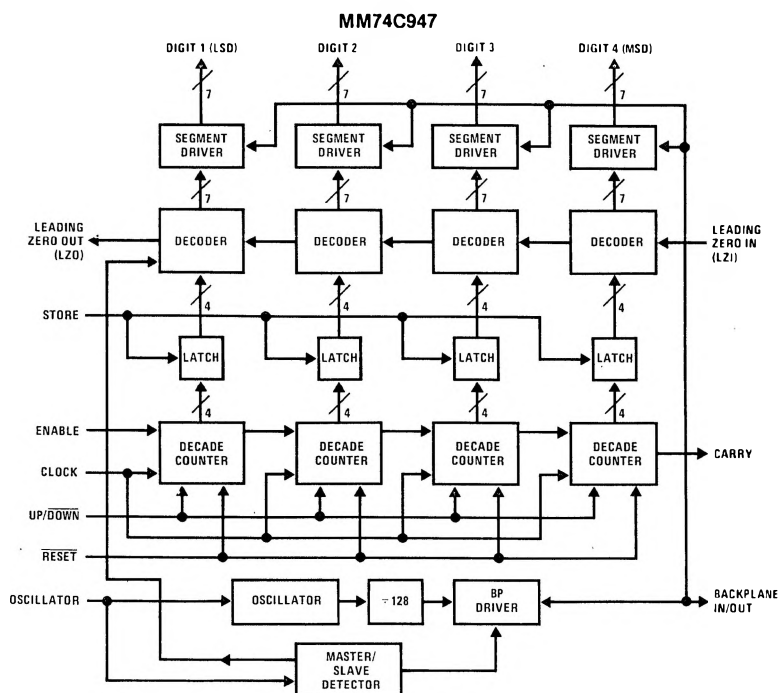
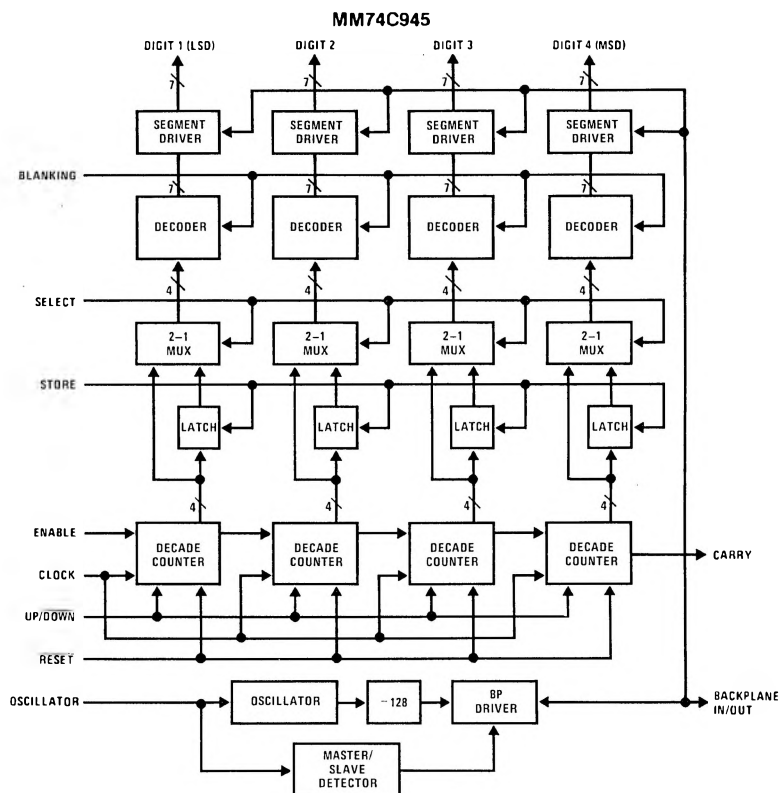


Test Circuit



* Each segment to backplane with 200 pF capacitor.

Block Diagrams



Pin Description

Backplane In/Out—When the oscillator input is grounded this pin is an input allowing an external device to generate a backplane waveform. When the oscillator input is left open this pin is an output supplying backplane drive for the display.

Oscillator—The oscillator frequency may be lowered by tying a capacitor to this pin. On the MM74C947 when the oscillator pin is open the LSD is inhibited from blanking when leading zero blanking is enabled. If this pin is grounded the backplanes on both parts become inputs, slaving the device to an external backplane.

Store—This input controls the on-chip latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high, the data on the counter outputs are stored in the latches.

Reset—When low, counters are reset to zero.

Clock—Advances counters on negative edge.

Enable—When low, halts counter operation.

Leading Zero Input (LZI)—(MM74C947) When high, enables leading zero blanking.

Leading Zero Output (LZO)—(MM74C947) This output goes high when the latch contents equal zero, LZI is high and the oscillator pin is open.

Blanking—(MM74C945) When high, blanks display.

Select—(MM74C945) When high, the contents of the counter are displayed. When low, the contents of the latch are displayed.

Carry—This output goes high when 9999 is reached (up) or 0000 is reached (down).

Up/Down—When high, the counter counts up. When low, the counter counts down.

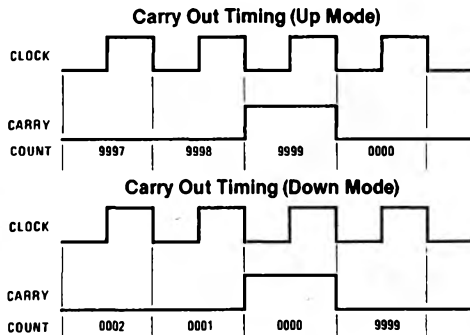
A1-G1—Digit 1 segment outputs.

A2-G2—Digit 2 segment outputs.

A3-G3—Digit 3 segment outputs.

A4-G4—Digit 4 segment outputs.

Timing Diagrams



Application Hints

Display Circuitry Description

The MM74C945 and MM74C947 have 28 segment outputs capable of directly driving 4 digits of 7 segments. Both the segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life.

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. This allows several devices to be driven by a single master backplane waveform which can be generated by another MM74C945, MM74C947 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven by several counters. The maximum fanout of a master backplane driver is limited by its total capacitive load, which is the sum of the slaved backplane input capacitances and the display backplane capacitance. (The MM74C947 oscillator pin controls the least significant digit blanking as well.)

An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency is typically 125 Hz, but may be slowed by connecting an external capacitor between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane pin will be put in the slave (input) mode.

Counter Circuitry Description

The MM74C945, MM74C947 are 4-decade up/down counters. The direction of the count is controlled by the up/down input. A high level on this pin causes the counter to count up. The counter advances on the negative clock edge. The carry output is high for 1 clock period during a count of 9999 in up mode and also high during a count of 0000 in down mode. The carry is designed to enable cascading of several circuits in either ripple carry or synchronous modes.

Reset and Enable controls are provided to allow period and frequency measurements. The Reset control clears the counter when low and the Enable control disables counting when taken low.

The counter chain feeds a series of 4-bit flow-through latches. These latches enable the display to follow the counter when the Store input is low. When the Store pin is taken high the data on the counter outputs at this time become latched and the display will remain unchanged. (Assuming the latch display is selected on MM74C945.)

On the MM74C945 the latch outputs feed a multiplexer which selects either the latch outputs or counter outputs for display. This allows an intermediate count to be stored in the latches while the counter continues to be displayed. This is equivalent to a stopwatch lap feature.

The output of the MM74C945's multiplexer feeds a decoder which converts 4-bit input to 7-segment. A blank control into these decoders blanks the display.

Application Hints (Continued)

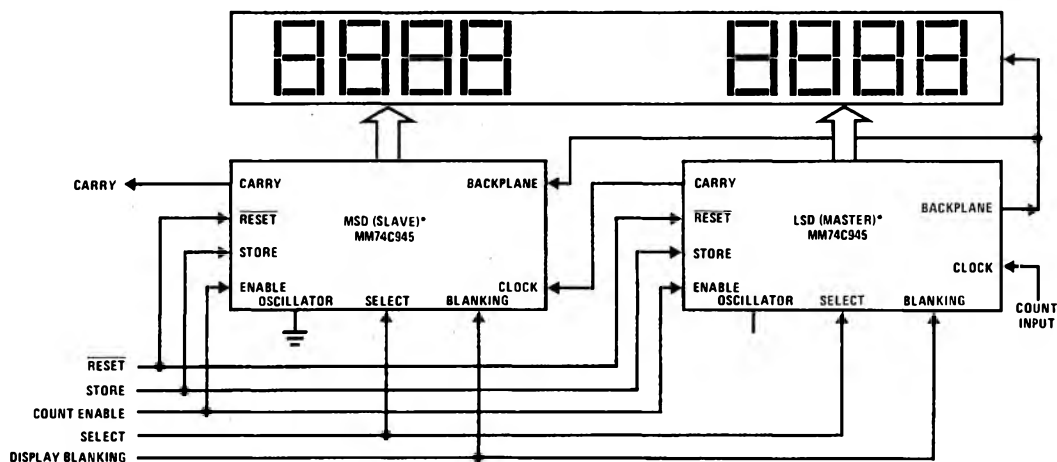
On the MM74C947 the latch outputs feed the decoders directly, but these decoders have a special ripple blanking capability that enables all leading zeroes except the least significant digit (LSD) to be blanked, even when counters are cascaded. Thus when the entire counter reads zero, instead of blanking all digits, the LSD will remain on. (When multiple counters are cascaded, all except the least signif-

icant counter will blank entirely on zeroes.) This feature is properly implemented by configuring the least significant device as the master (oscillator pin ungrounded) thereby inhibiting LSD blanking.

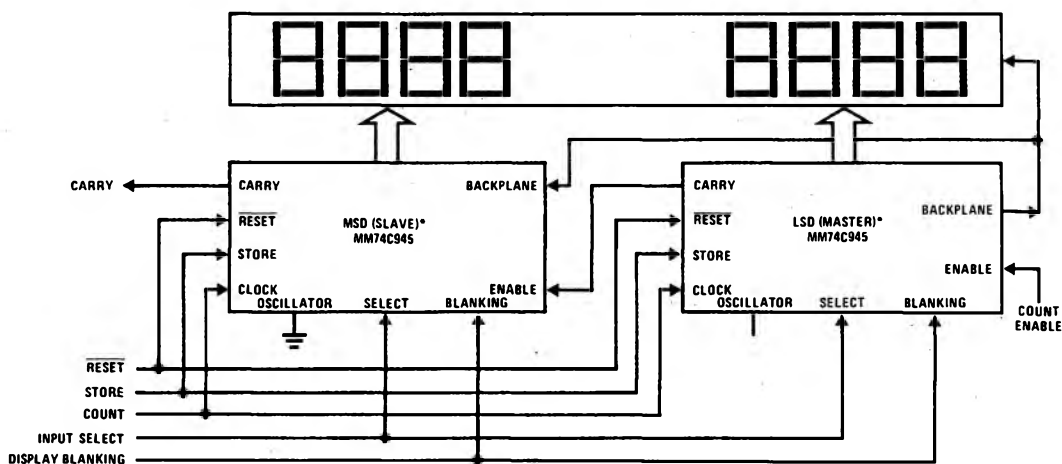
The outputs of the decoders for both devices control the segment drivers which in turn enable display operation.

Typical Applications

Ripple Carry Cascading—MM74C945



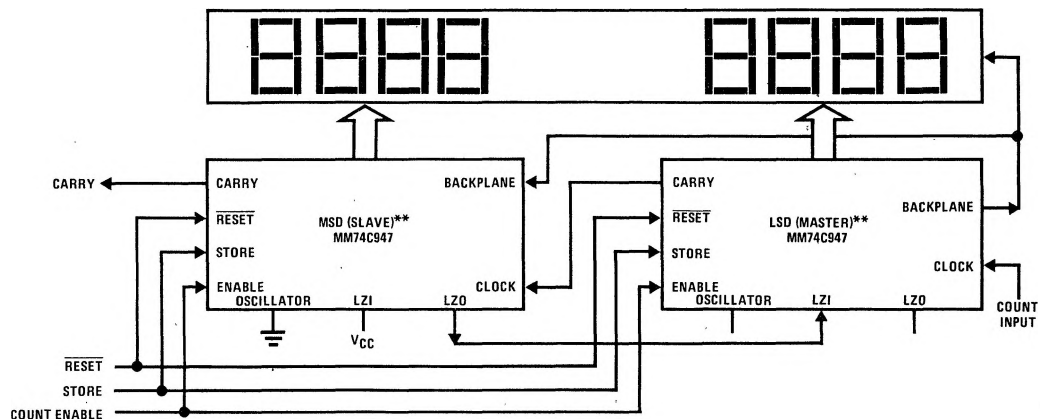
Synchronous Cascading—MM74C945



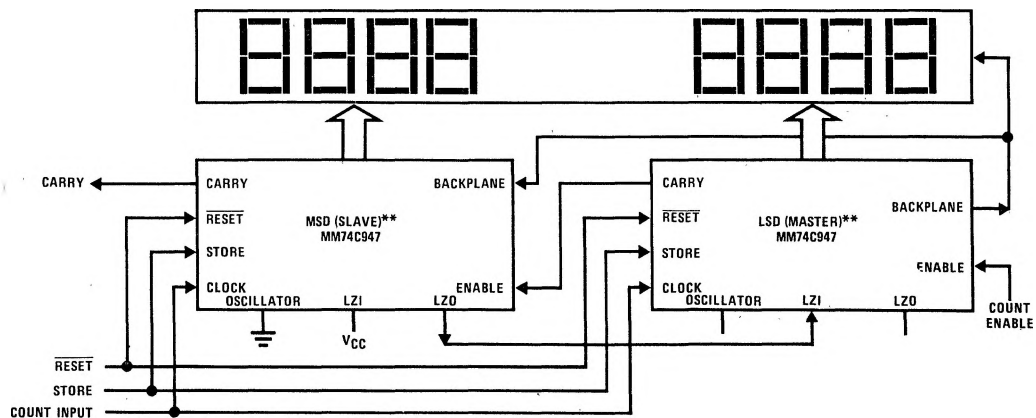
* Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

Typical Applications (Continued)

Ripple Cascading—MM74C947



Synchronous Cascading—MM74C947



** To correctly implement leading zero blanking the least significant device must be the master.