National Semiconductor

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs CES and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

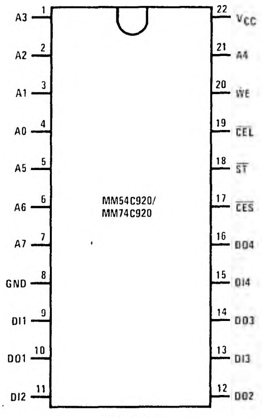
Complete address decoding as well as 2-chip select functions, CEL and CES, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

Features

- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C920-3, MM74C921-3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V_{CC} as low as 2V

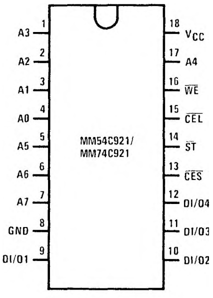
Connection Diagrams

Dual-In-Line Package



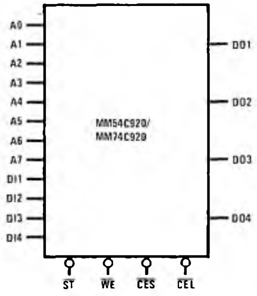
TOP VIEW

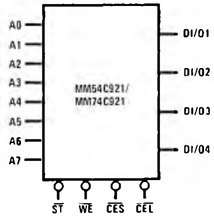
Dual-In-Line Package



TOP VIEW

Logic Symbols





Functional Description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1*. Input addresses and $\overline{\text{CES}}$ are clocked into the input latches by the falling edge of $\overline{\text{STROBE}}$. Input set-up and hold times must be observed on these signals (see timing diagrams). The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

The addressed word (4 bits) is fed to 4 sense amplifiers through the column decoders. The information from the sense amplifiers is latched into the output register when $\overline{\text{STROBE}}$ rises. The register drives the TRI-STATE® output buffers.

Chip select inputs, $\overline{\text{CEL}}$ and $\overline{\text{CES}}$, have identical functions except that $\overline{\text{CES}}$ (Chip Enable Stored) is clocked into a latch on the falling edge of $\overline{\text{STROBE}}$; $\overline{\text{CEL}}$ (Chip Enable Level) is not.

Note that set-up and hold times must be observed on $\overline{\text{CES}}$. Because $\overline{\text{CEL}}$ is not clocked by $\overline{\text{STROBE}}$, it may fall after $\overline{\text{STROBE}}$ has fallen without affecting access time provided that the t_{OE} requirement is met.

The outputs are in a high impedance state when the chip is not selected ($\overline{\text{CES}}$ or $\overline{\text{CEL}}$ high) or when writing ($\overline{\text{WE}}$ low). Note that the information stored in the output latches will be changed whenever $\overline{\text{STROBE}}$ falls, regardless of the logic states of $\overline{\text{WE}}$, $\overline{\text{CEL}}$ or $\overline{\text{CES}}$.

The switching time waveforms in *Figures 2, 3 and 4* define the read, write, and output enable/disable parameters respectively.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, $\overline{\text{ST}}$ logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*

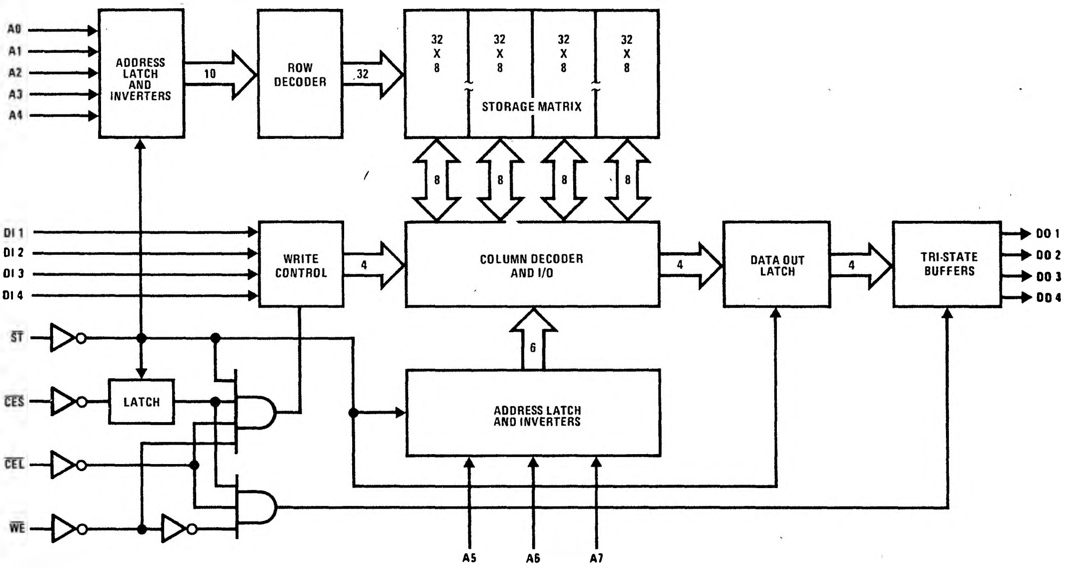


FIGURE 1. MM54C920/MM74C920

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*The logic diagram for the MM54C921/MM74C921 is identical to this except that data inputs (DI1–DI4) are connected to data outputs (DO1–DO4).

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C920, MM54C921	4.5	5.5	V
MM74C920, MM74C921	4.5	5.5	V
MM74C920-3, MM74C921-3	4.75	5.25	V
Ambient Temperature (T_A)			
MM54C920, MM54C921	−55	+125	°C
MM74C920, MM74C921	−40	+85	°C
MM74C920-3, MM74C921-3	0	+70	°C

DC Electrical Characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920−3, MM74C921−3		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−1.5	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \le V_{IN} \le V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	µA
I_O	Output Leakage	$0V \le V_O \le V_{CC}$, $\overline{CEL} = V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	µA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, V_O = 0V		20		10		100	µA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	$\overline{CEL} = V_{CC}$ = 2V, Typical at 25°C		0.01 (typ)		0.01 (typ)		0.1 (typ)	µA

Capacitance (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		4	7	pF
C_O	Output Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values above which the device may be permanently damaged. They do not mean the device may be operated at these values.

Note 2: These limits apply over the entire operating range specified in the "Operating Conditions" unless otherwise stated.

Note 3: $\overline{CEL} = V_{CC}$ − 2V or = 2V, whichever is greater.

Note 4. Capacitance is guaranteed by periodic testing.

Truth Table

$\overline{ST}$	$\overline{CES}$*	$\overline{CEL}$	$\overline{WE}$	DI*	FUNCTION
X	X	1	X	X	Output in Hi-Z state
0	1	X	X	X	Output in Hi-Z state
X	X	X	0	X	Output in Hi-Z state
0	0	0	0	0	Write "0", output in Hi-Z state
0	0	0	0	1	Write "1", output in Hi-Z state
0	0	0	1	X	Read data, output enabled

*Set-up and hold times must be met
X = don't care

AC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920–3 MM74C921–3		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		275		250		325	ns
t_{ACS}	Access Time From Strobe		250		225		300	ns
t_{AS}	Address Set-Up Time	25		25		25		ns
t_{AH}	Address Hold Time	25		25		25		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150		130		165		ns
t_{ST}	ST Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time	100		90		90		ns
t_{DH}	Data Hold Time	60		60		60		ns

Note 5: These limits apply over the operating range specified in the "Operating Conditions" with $t_{RISE} = t_{FALL} = 5$ ns, load = 1 TTL gate + 50 pF.

Switching Time Waveforms

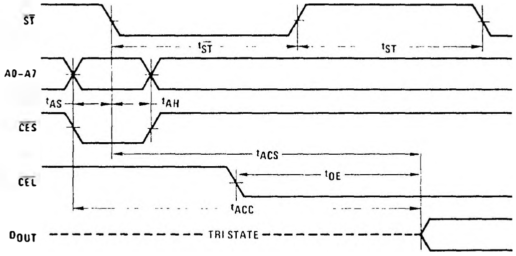
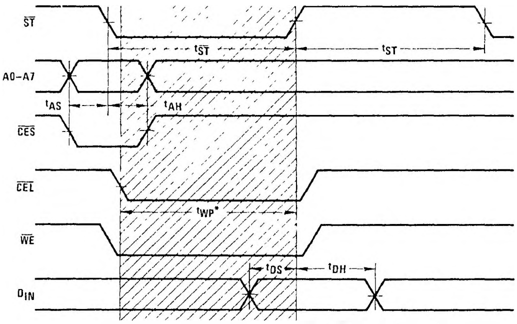


FIGURE 2. Read Cycle ($\overline{WE} = V_{IH}$)



*t_{WP} (the Write Pulse Width) is the time $\overline{ST}$, $\overline{CEL}$ and $\overline{WE}$ are coincidentally low

FIGURE 3. Write Cycle

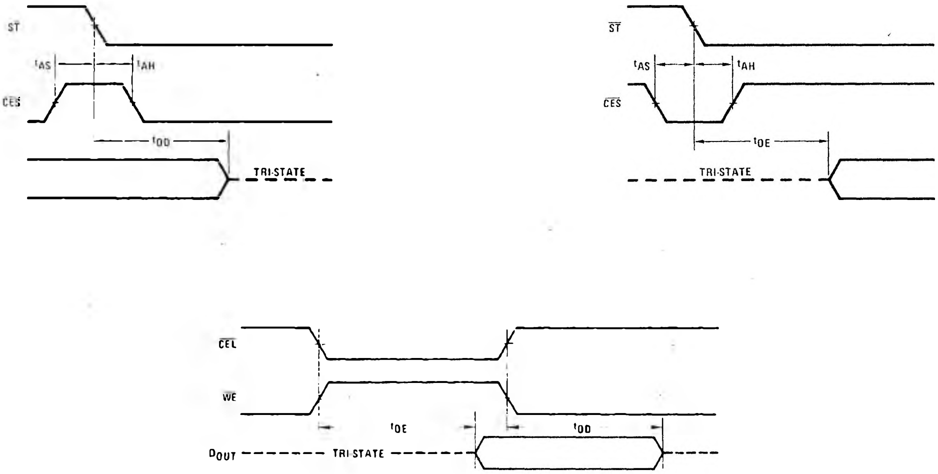
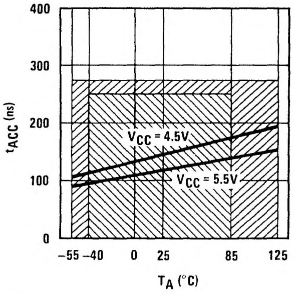


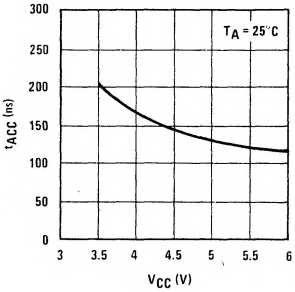
FIGURE 4. Output Enable/Disable

Typical Performance Characteristics

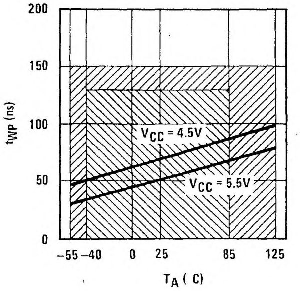
Access Time vs Ambient Temperature



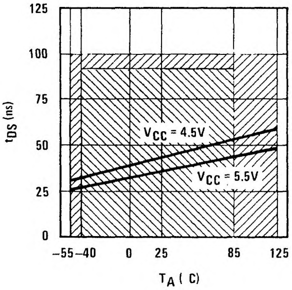
Access Time vs Power Supply Voltage



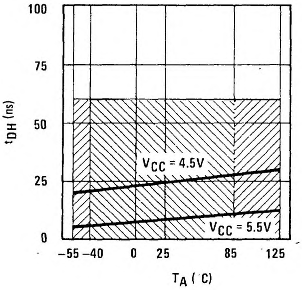
Minimum Write Pulse Width vs Ambient Temperature



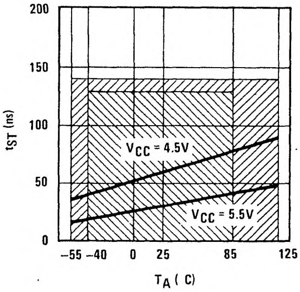
Data-In Setup Time vs Ambient Temperature



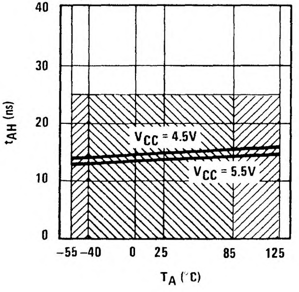
Data In Hold Time vs Ambient Temperature



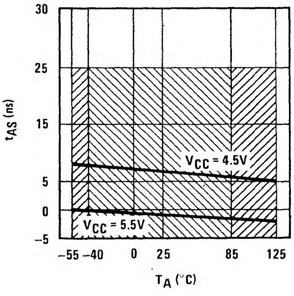
Minimum ST Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

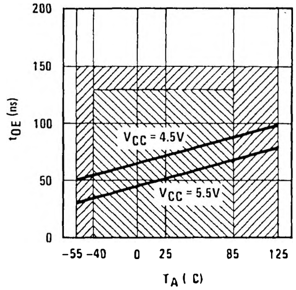


Address Setup Time vs Ambient Temperature

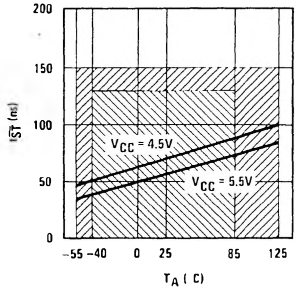


Typical Performance Characteristics (Continued)

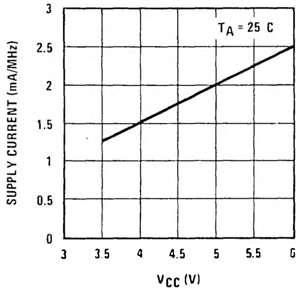
Output Enable Time vs Ambient Temperature



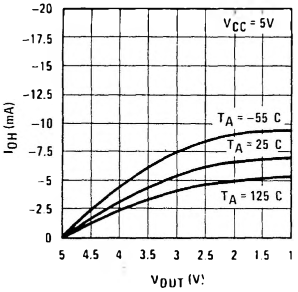
Minimum $\overline{ST}$ Pulse Width (Negative) vs Ambient Temperature



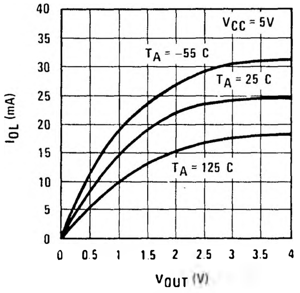
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



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Test Limit MM54C920, MM54C921

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Test Limit MM74C920, MM74C921