National Semiconductor

MM54C175/MM74C175 Quad D Flip-Flop

General Description

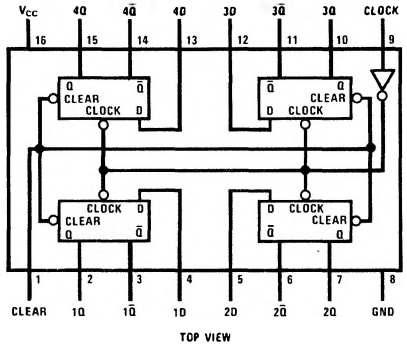
The MM54C175/MM74C175 consists of four positive-edge triggered D type flip-flops implemented with monolithic CMOS technology. Both are true and complemented outputs from each flip-flop are externally available. All four flip flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram and Truth Table



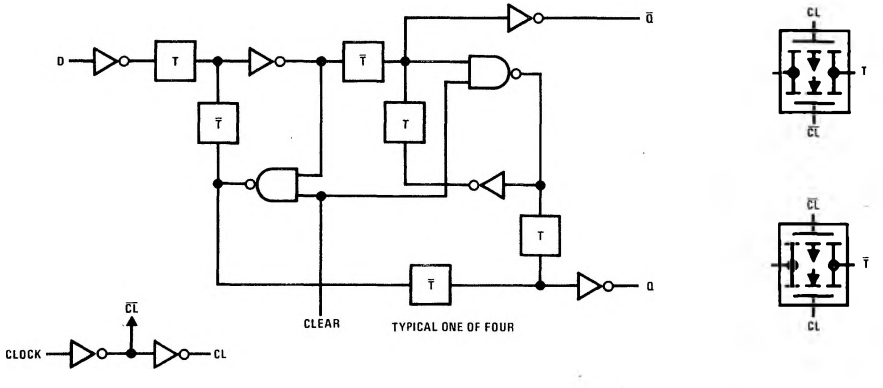
TOP VIEW

Each Flip-Flop

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

Logic Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C175	−55°C to +125°C
MM74C175	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V v
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360μA 74C V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360μA 74C V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V T_A = 25°C, V_{OUT} = 0V	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = 0V	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		190 75	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay time to a Logical "1" from Clear to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		230 90	400 150	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	100 40	45 16		ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0 0	−11 −4		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		130 45	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 45	250 100	ns ns
t_r	Maximum Clock Rise Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0	450 125		μs μs
t_f	Maximum Clock Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0	50 50		μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.0	3.5 10		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		10 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		130		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms

CMOS to CMOS