National Semiconductor

MM54C174/MM74C174 Hex D Flip-Flop

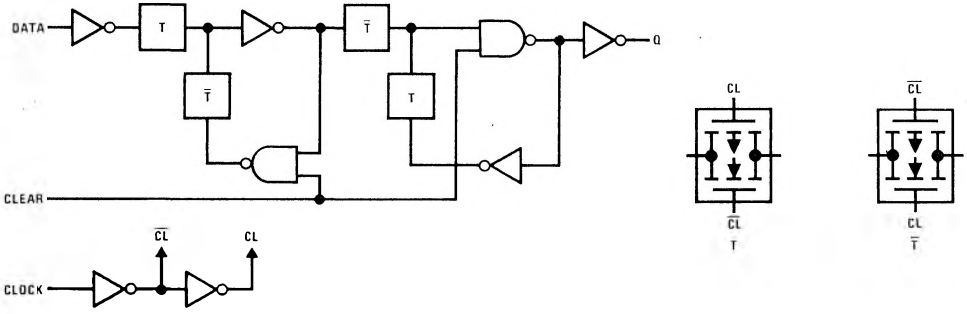
General Description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes To V_{CC} and GND.

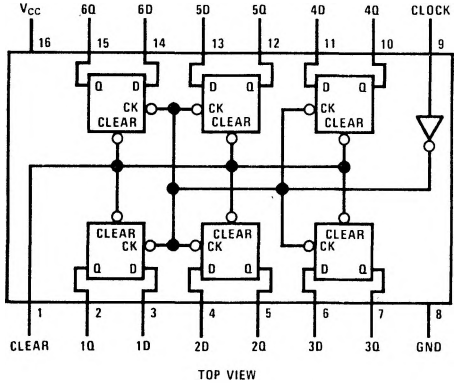
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Logic Diagrams



Connection Diagram



TOP VIEW

Truth Table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC} + 0.3\,V$
Operating Temperature Range	
MM54C174	$-55°C$ to $+125°C$
MM74C174	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\mu A$ $V_{CC} = 10\,V$, $I_O = -10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = +10\mu A$ $V_{CC} = 10\,V$, $I_O = +10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -360\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = -360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 360\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = 360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		110 50	300 110	ns ns
t_{S1}, t_{S0}	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	75 25			ns ns
t_{H1}, t_{H0}	Time after Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0 0	−10 −5.0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		50 35	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		65 35	140 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0	>1200 >1200		μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.0	6.5 12		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		11 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		95		pF

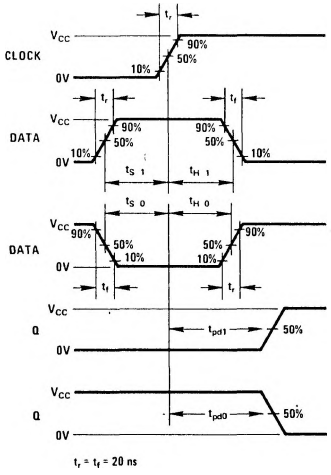
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms

CMOS to CMOS



$t_r = t_f = 20\,ns$

AC Test Circuit