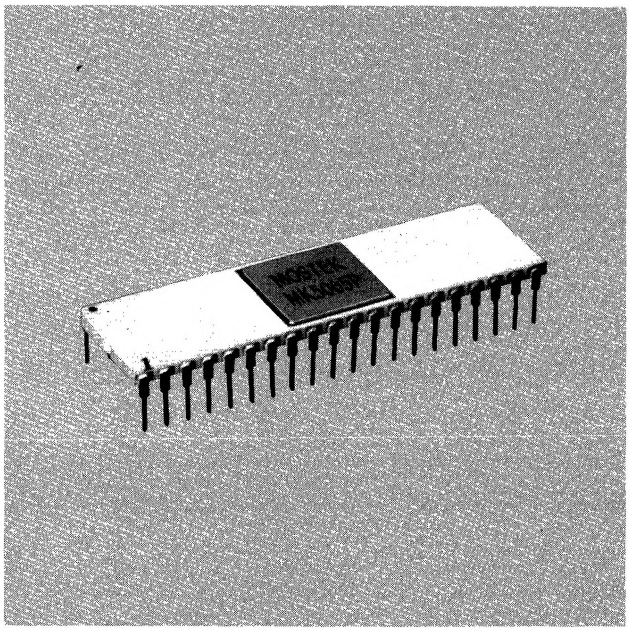
MK 5065P

8-BIT Microprocessor

MOSTEK

FEATURES:

- 8-bit parallel microprocessor on a single chip
- 51 basic instructions/81 instructions with modifications
- TTL compatible inputs and outputs
- Directly addresses 32Kx8 bit memory
- Triple level architecture for rapid interrupt servicing
- Single 40-pin package
- DMA capability
- Requires standard power supply voltages
- Indirect addressing capability



DESCRIPTION

Instructions and data are transmitted to the CPU on a bidirectional 8-bit bus. An 8-bit outbut bus is used along with the bidirectional bus to provide simultaneous memory addresses for addressing up to 32KX8 bits of memory.

Six control input signals provide control of the CPU and seven status output signals indicate the current status of the CPU.

Up to 32KX8 bits of memory may be addressed either directly or indirectly by the CPU. The memory is addressed in a page mode. Each page of memory consists of 256 locations, and there are 128 pages of memory. If subroutine call and return instructions are to be used, the first page of memory must be implemented with RAM because page zero is used as a subroutine return address stack. Thus up to 128 subroutine levels may be nested.

The MK 5065 is capable of executing 51 basic instructions. These basic instructions may be modified by instruction modification fields in the instruction format to expand the total number of executable instructions to 81. These instructions are divided into ten functional instruction categories:

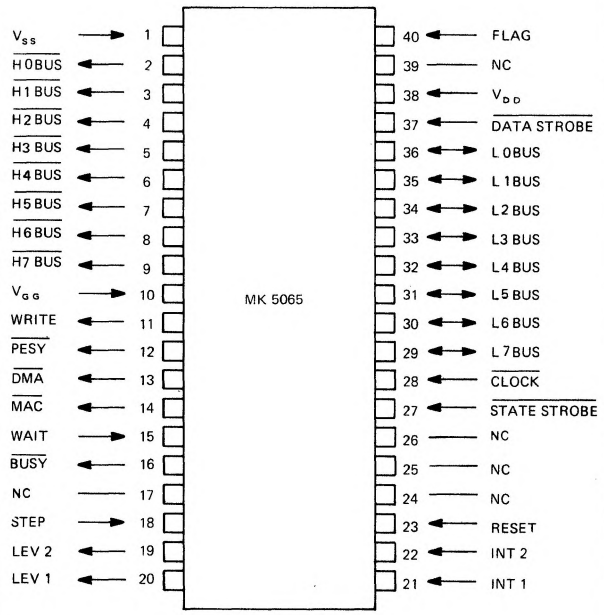
1. Accumulator Instructions
2. Immediate Instructions
3. Memory Instructions
4. Jump Instructions
5. Shift Instructions
6. Exchange Instructions
7. Skip Instructions
8. Status Change Instructions
9. Accumulator/Link Instructions
10. Input/Output Instructions

Seven instruction formats provide direct or indirect, page or entire memory addressing capability. Additionally operations involving immediate data may be performed. A 4-bit "free field" in the I/O instruction allows the user to define a program controlled peripheral communication language set.

Two independent interrupt lines which are selectively enabled under program control select one of three operating levels for the CPU.

DMA capability is provided by a wait input signal and a DMA output signal which indicates when the CPU has completed the last memory cycle in the current instruction execution.

PIN CONNECTION



NC = NO CONNECTION

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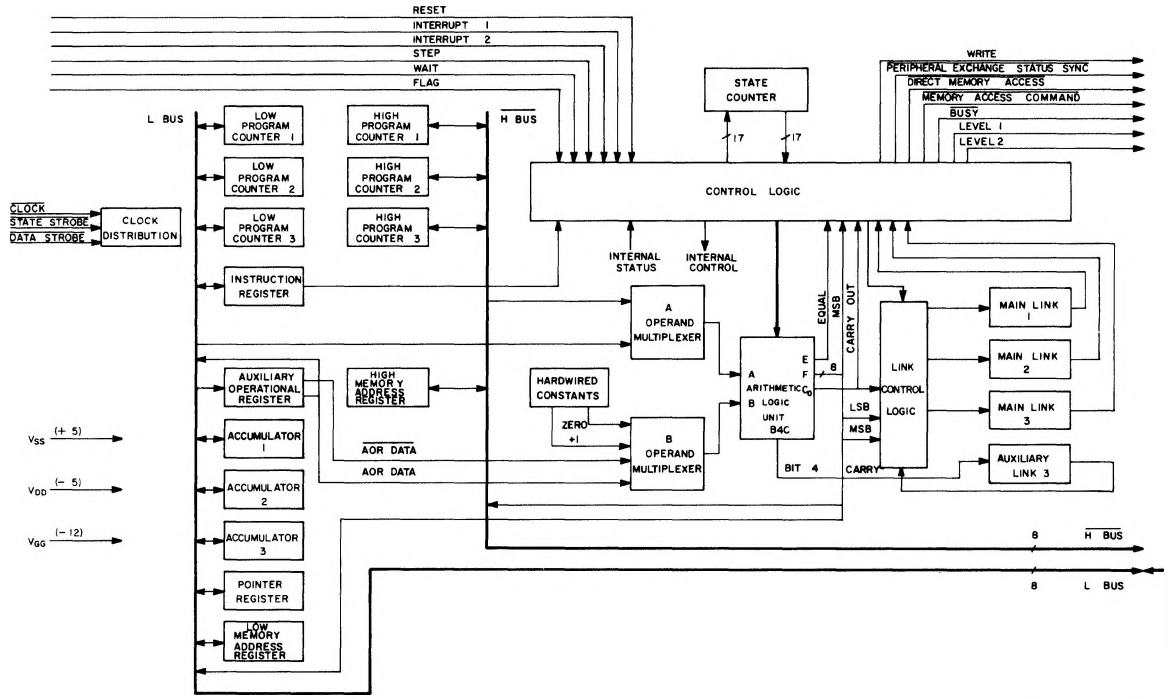
BLOCK DIAGRAM



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BLOCK DIAGRAM DESCRIPTION

As shown in the CPU Block Diagram above, the MK 5065 is organized as a triple level parallel central processing unit. Each of the three operating levels contains a program counter, accumulator, and main link. In addition to these elements, level 3 also has an auxiliary link for storage of carrys and borrows beyond the fourth bit.

Since each level has a program counter, accumulator, and main link for that level there is no need to store in memory the contents of the program counter, accumulator, and machine status information when servicing interrupts. Thus interrupt response is very rapid, the only delay being the time required for the CPU to complete the execution of the current instruction.

The CPU uses two 8-bit buses to communicate with the external devices that comprise the remainder of the system. The HBUS (High Bus) is an 8-bit parallel output bus that transmits the most significant byte of the memory address register contents to the program memory during memory read or write cycles. The LBUS (Low Bus) is a parallel 8-bit bidirectional bus that is used to transmit the least significant byte of the memory address register contents to the program memory during memory read or write cycles. Accumulator data is transmitted to the program memory during a memory write cycle over the LBUS too. This same bidirectional bus is also used to load memory instructions into the instruction register and immediate memory data into the accumulator.

A parallel arithmetic logic unit provides the capability of performing arithmetic or logical operations on two operands selected by the two operand multiplexers.

Instruction execution is controlled by the control logic and state counter.

The 32Kx8 bit memory is organized as eight 4K blocks. Each block consists of 16 pages. Each page consists of 256 words of 8 bits. The memory may be composed of a mix of ROM and RAM although page zero must be implemented with RAM if subroutine instructions are to be used. Page zero of the memory is used as subroutine return address stack. Each adjacent pair of bytes stores the absolute subroutine return address. Thus, up to a maximum of 128 subroutines may be nested. An 8-bit pointer register is used to store the address of the next free position in the stack.

Both direct and indirect memory addressing modes are available. In the direct addressing mode, an absolute memory address on either the current page or on page zero is specified by the second byte of the instruction. In the indirect mode of addressing, the second byte of the instruction specifys the absolute address on either the current page or page zero of the first of two adjacent bytes that contain the address of the operand. The most significant bit of this 16 bit address specifys whether the address is a direct or an indirect address. Since any memory location may contain either an operand or another indirect address, a chain of addresses in memory may specify the actual location of the operand referenced by an instruction.

Multiple interrupt handling capability is provided by two interrupt input signals. Level 3 is the lowest priority operating level. If the CPU is operating on level 3 and an interrupt two (INT2) signal is received, the CPU begins operating on level 2 at the completion of the execution of the instruction currently being executed on level 3 if the interrupt two input has been previously enabled by an Interrupt On or (ION) instruction.

Since the program counter, accumulator, and main links exist in triplicate it is not necessary to go through the usual procedure of saving the contents of these elements when servicing an interrupt or executing a subroutine call instruction. Similarly when executing a return from a subroutine it is not necessary to restore the contents of these units since their previous contents have been preserved in the hardware dedicated to that particular level.

Interrupt one (INT 1) has the highest priority level. Two Level signals (LEV 1 and LEV 2) define the level on which the CPU is operating. If the LEV 1 output signal is a logical one, the CPU is operating on level one. If the LEV 2 signal is a logical one, then the CPU is operating on Level two. If neither the LEV 1 nor the LEV 2 signal is a logical one, then the CPU is operating on Level 3.

I/O operations use the HBUS and the LBUS for transmitting data and commands to the peripherals and for transmitting data and status from the peripherals to the CPU. During the first state strobe pulse the least significant six bit byte of the input or output instruction and the contents of the accumulator are transmitted to the peripheral. During the second state strobe pulse peripheral data is clocked into the peripheral output register if an input instruction is being executed. During the third-state strobe pulse data in the peripheral output register is clocked into the CPU. Finally the fourth state strobe pulse defines the end of the transfer and may be used to reset the peripheral.

Instructions are grouped into ten classifications:

1. Accumulator Instructions — Instructions involving the accumulator.
2. Immediate Instructions — Instructions in which the operand is immediate data.
3. Memory Instructions — Instructions that modify memory contents.
4. Jump Instructions — Jump instructions and subroutine call and return instructions.
5. Shift Instructions — Instructions which rotate accumulator contents.
6. Exchange Instructions — Instructions which cause internal register and byte transfers.
7. Skip Instructions — Conditional instructions which cause the next instruction to be skipped.
8. Status Change Instructions — Instructions which modify machine status.
9. Accumulator/Link Instructions — Instructions which modify the accumulator and/or link contents.
10. Input/Output Instructions — Instructions that input and output data to and from the CPU.

Seven instruction formats are used in the instruction set. There are three two byte instruction formats and four single byte instruction formats.

In the first instruction format, the most significant six bits of the first byte of the instruction contain the instruction code. The two least significant bits of the first byte of the instruction are instruction modification bits. The least significant bit of the first byte of the instruction specifies that the operand address contained in the second byte of the instruction is on the current page when this bit is a logical one. When the LSB of the first byte is a logical zero, the address specified by the second byte is on page zero of the memory. The next MSB of the first byte of the instruction specifies direct addressing mode when this bit is a logical zero. A logical one specifies indirect addressing mode. The second byte of the instruction is an eight bit address field that contains the address of the operand or jump location on the specified page.

The second instruction format is also a two byte format. The four most significant bits of the first byte of the instruction contain the instruction code. The four least significant bits of the first byte of the instruction and the entire eight bit field of the second byte of the instruction form a 12-bit address field. This format is used for jump immediate and call subroutine immediate instructions. The location specified by the address field is located in the same 4KX8 block of memory as the instruction. That is, the four most significant bits of the address are the same as the four most significant bits of the memory address of the instruction.

The first byte of the third instruction format contains the instruction code. The second byte contains the immediate operand.

Jump shift, exchange, skip and status change instructions use the fourth instruction format. The entire eight bit field of this single byte instruction contains the instruction code.

I/O instructions use the fifth instruction format. The most significant four bits of the instruction contains the instruction code. The second four bit byte of the instruction is a free field. The CPU does not make use of this field of the instruction. Thus, this free field may be used to define an I/O peripheral communication code.

The accumulator/link instruction makes use of the sixth instruction format. The three most significant bits of the instruction contain the instruction code. The five least significant bits of the instruction specify one of 28 possible instruction modifications.

Interrupts may be selectively enabled or disabled using the seventh instruction format. The six most significant bits of this instruction contain the instruction code. The two least significant bits define the interrupt that is to be enabled or disabled by the instruction. The least significant bit specifys interrupt one and the second modifier bit specifies interrupt two.