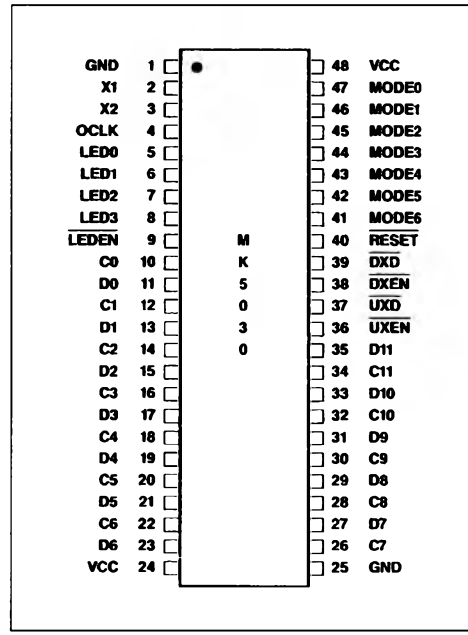
SGS-THOMSON MICROELECTRONICS

MK5030P/N

StarLAN HUB CHIP COMMUNICATIONS PRODUCTS

- COMPLETE HUB LOGIC DEVICE COMPATIBLE TO STARLAN SPECIFICATION
- SUPPORTS MULTI-POINT EXTENSION (MPE)
- AUTO COMPENSATION FOR WIRING REVERSAL
- 12 PORT HUB
- OPTIONAL RETIME CIRCUIT
- CASCADABLE. TWO LEVELS MAY BE CASCADED AND STILL APPEAR TO THE NETWORK AS ONE YIELDING UP TO A 121 PORT HUB
- AUTO PREAMBLE GENERATION TO MINIMIZE BIT LOSS
- SELECTABLE ACTIVE CARRIER POLARITY SENSE
- JABBER FUNCTION ISOLATES NETWORK FAILURES
- OPTIONAL MINIMUM FRAME LENGTH ENFORCEMENT
- COLLISION DETECTION
  - multiple inputs
  - missing mid-bit transition
  - transitions too close together
  - transitions too far apart
  - AT & T Release 1 Collision presence signal
- 6X CLOCK YIELDS 167NS JITTER TOLERANCE
- TRANSMIT DATA TRAILER ENFORCEMENT
- INPUT PROTECTION AT END OF FRAME (20µs)
- PIN SELECTABLE HIGH-END HUB VERSUS INTERMEDIATE HUB
- OPTIONAL INTERNAL PULSE STRETCHER FOR CARRIER SENSE SQUELCH
- UPLINK AND DOWNLINK ACTIVE STATUS OUTPUTS
- UPLINK AND DOWNLINK COLLISION STATUS OUTPUTS
- PER PORT JABBER STATUS OUTPUT
- ON CHIP CRYSTAL OSCILLATOR CIRCUITRY
- 35mW TYPICAL POWER DISSIPATION
- CMOS TECHNOLOGY
- 48 PIN DIP
- SINGLE 5-VOLT SUPPLY
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE*
- INDUSTRIAL VERSION AVAILABLE

Figure 1 : MK5030 Pin Assignment.



DESCRIPTION

The MK5030-HUB is a 48 pin CMOS VLSI device that simplifies the design and implementation of a StarLAN compatible HUB. This chip provides all the digital logic necessary in a HUB.

PIN DESCRIPTION

X1, X2 — Inputs. Either connect a 6.00 ± 0.05% MHz crystal between the pins, or leave X2 not connected and apply a 6.0MHz ± .01% square wave to X1. (Refer to figure 7).

OCLK — Output. Provides a TTL CLK output from the above crystal oscillator. This is useful when cascading devices.

C0-C11 — Schmitt inputs. Carrier sense inputs. Active state is selectable. Refer to MODE4 below.

D0-D11 — Inputs. Received data streams.

$\overline{UXD}$ — Output. UPLINK data stream to the next UPPER HUB, if any, in the network hierarchy.

$\overline{UXEN}$ — Output. UPLINK transmit enable indicating that $\overline{UXD}$ contains valid data.

$\overline{DXD}$ — Output. Downlink data stream to all ports. If MODE1 = 1, then this data stream is derived from Port 11. If MODE1 = 0 then this data stream is identical to $\overline{UXD}$.

$\overline{DXEN}$ — Output. Downlink transmit enable to all ports. If MODE1 = 1, then this data stream is derived from Port 11. If MODE1 = 0, then this data stream is identical to $\overline{UXEN}$.

MODE0 — Input. Testmode. Should be tied high for normal operation. Testmode is useful only for semiconductor device production test.

MODE1 — Input. If MODE1 = 1, then the chip is an intermediate hub ; and C0-10/D0-10 inputs will be used as UPLINK inputs and C11/D11 as the DOWNLINK input. If MODE1 = 0, then the chip is a high-end hub ; C0-11/D0-11 inputs will be used as UPLINK inputs and DOWNLINK outputs (DXD, DXEN) will internally be connected to the UPLINK outputs (UXD, UXEN). See figure 5.

MODE2 — Inputs. If MODE2 = 0, then the input carriers have been externally stretched and no internal stretcher is desired. This stretcher is required as part of the squelch function. Refer to figure 2. If MODE2 = 1, then the input carriers are threshold set off the incoming data stream and an internal pulse stretcher must be used. With MODE2 = 1, users do not need to use one-shots externally for each port.

MODE3 — Input. If MODE3 = 1, then the retimer circuit is enabled as specified by IEEE 802.3. If MODE3 = 0, then the retimer circuit is disabled. This allows HUBs in close physical proximity to be cascaded together and appear to the network as one HUB. Refer to figure 3.

MODE4 — Input. Selects carrier active state. If MODE4 = 0, then the carrier inputs (C0-C11) are active low. If MODE4 = 1 then the carrier inputs (C0-C11) are active high.

MODE5 — Input. If MODE5 = 1, then auto preamble generation is enabled. The chip will initiate preamble transmission once phase lock is obtained. Once the transmit FIFO is sufficiently full, transmit data is obtained from the FIFO. This decreases the amount of bits a HUB implementation will lose. Depending on the implementation, bits may actually be gained. If MODE5 = 0, then automatic preamble generation is disabled.

MODE6 — Input. If MODE6 = 1, then minimum frame length of 96 bits is enforced. If MODE6 = 0, then no minimum frame length is enforced.

$\overline{RESET}$ — Schmitt input. Active low. A low causes the device to reset. Input must be high for normal operation.

$\overline{LEDEN}$ — Input/output open drain. If $\overline{LEDEN}$ is externally connected to GND, then the LED (0-3) provide static status information. Otherwise, $\overline{LEDEN}$ should be pulled high through a 2Kohm pullup resistor and LED (0-3) will provide an ID of an internal status monitoring point and will pull $\overline{LEDEN}$ low if that monitoring point is active. This allows connection of a single external multiplexer to drive indicating devices. Refer to figure 4.

LED0-LED3 Output. If $\overline{\text{LEDEN}}$ is connected to GND :

LED0 UPLINK transmit enabled
LED1 UPLINK collision sense
LED2 DOWNLINK transmit enabled
LED3 DOWNLINK collision sense.

If $\overline{\text{LEDEN}}$ is not connected to GND, then $\overline{\text{LEDEN}}$ = 0 indicates that the LED (0-3) specified function is active :

LED3	LED2	LED1	LED0	Description		$\overline{\text{LEDEN}}$ = 0	$\overline{\text{LEDEN}}$ = 1
0	0	0	0	PORT 0	jabber	active	inactive
0	0	0	1	PORT 1	jabber	active	inactive
0	0	1	0	PORT 2	jabber	active	inactive
0	0	1	1	PORT 3	jabber	active	inactive
0	1	0	0	PORT 4	jabber	active	inactive
0	1	0	1	PORT 5	jabber	active	inactive
0	1	1	0	PORT 6	jabber	active	inactive
0	1	1	1	PORT 7	jabber	active	inactive
1	0	0	0	PORT 8	jabber	active	inactive
1	0	0	1	PORT 9	jabber	active	inactive
1	0	1	0	PORT 10	jabber	active	inactive
1	0	1	1	PORT 11	jabber	active	inactive
1	1	0	0	UPLINK		inactive	active
1	1	0	1	UPLINK Collision		yes	no
1	1	1	0	DOWNLINK		inactive	active
1	1	1	1	DOWNLINK Collision		yes	no

Note : 1. UPLINK and DOWNLINK status outputs are normally on and will blink off for 147mS when a frame is transmitted. LED on-time of 147mS is guaranteed between each off blink.
2. UPLINK and DOWNLINK collision outputs are normally off and will blink on for 147mS when a collision is detected. LED off time of 147ms is guaranteed between each on blink.

VCC Power supply pin. + 5 VDC ± 5%

GND Ground. 0 VDC.

Figure 2 : Internal Versus External Time Squelch.

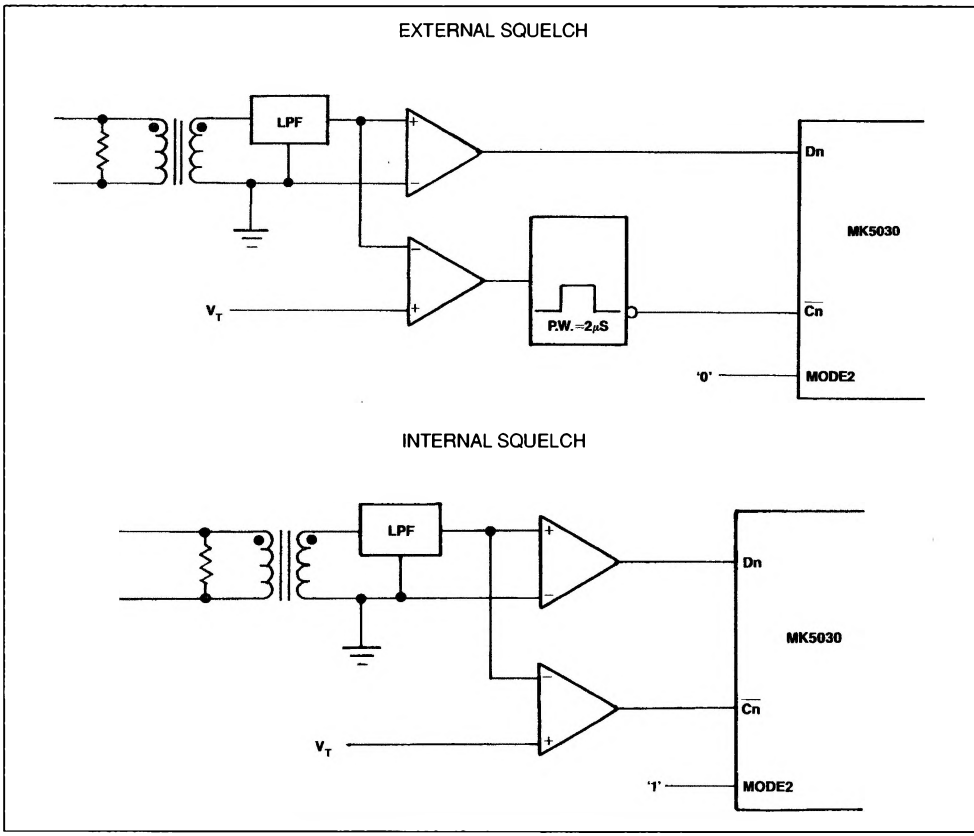
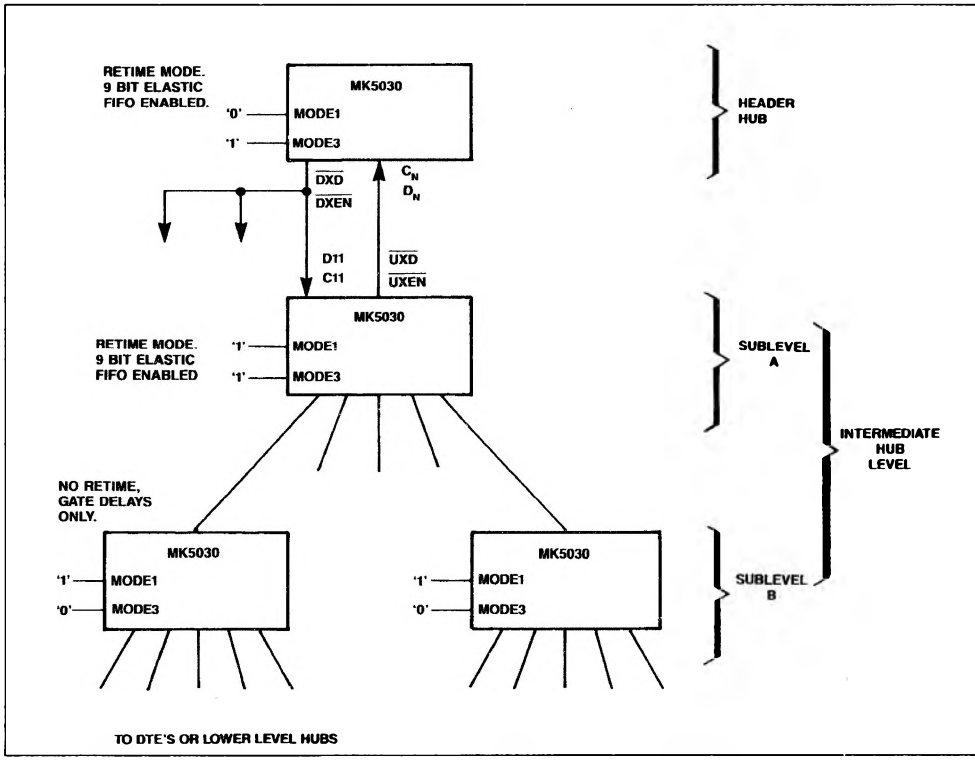
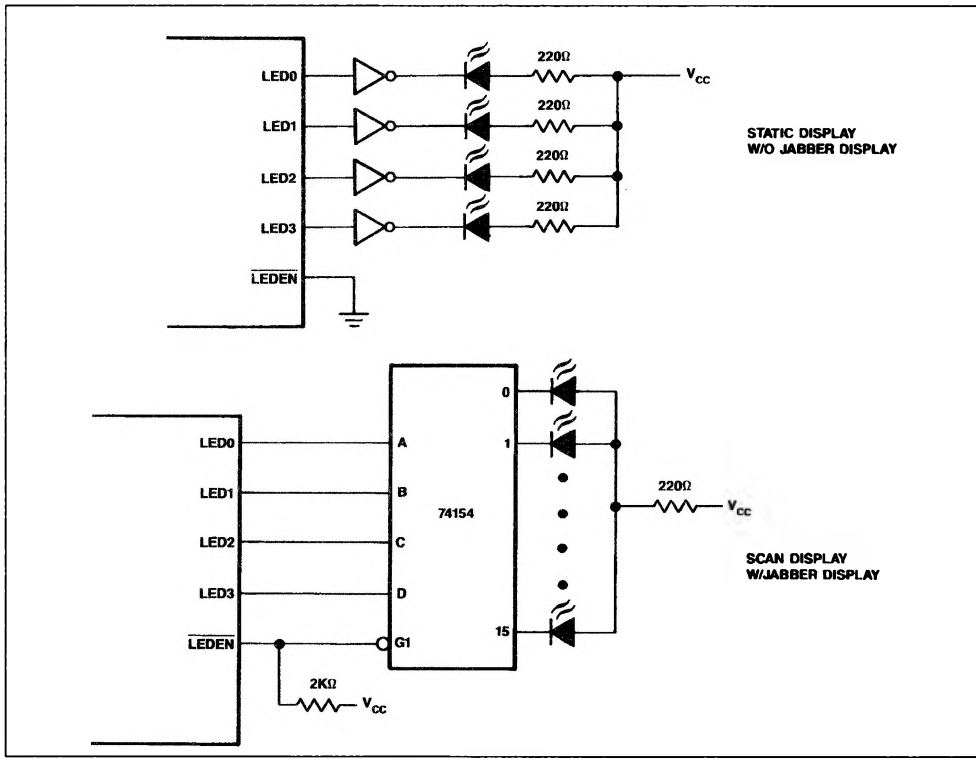


Figure 3 : Example Showing Retime and No-retime Modes.



Note : Sublevels A and B may either be on same circuit board or on separate boards located in close proximity.

Figure 4 : Status Display Modes.



OVERVIEW OF CIRCUIT DESCRIPTION

The MK5030 HUB chip consists of three sub-modules : the uplink, the downlink, and the status display module.

The uplink module multiplexes twelve inputs from stations and/or "lower" HUBS (see figure 3) and retimes the multiplexed data to remove jitter. The uplink also handles several optional features including retiming, disabled auto-preamble generation, and collision detection/transmission. Refer to figure 5, MK5030 HUB Block Diagram.

The downlink module is used only in the intermediate mode, and is nearly identical to the uplink (see figure 3).

The status display modules provide both static and scanned display of the line activity, detected collisions, and "jabbed" inputs.

THE UPLINK MODULE

The uplink module has a carrier processor which performs the following :

- Detects carrier and outputs a carrier presence signal.
- Detects collision and outputs a collision presence signal.
- Will ignore one, or more, inputs by the jabber or protection time functions.
- Provides time domain filtering to improve noise tolerance on carrier inputs.
- When in the retime mode :
  - Automatically compensates for wiring reversal.
  - Recovers clock using a DPLL (for internal HUB chip use only).
  - Passes data through a serial 9 bit FIFO buffer.

- When in minimum frame length mode, the frame length is guaranteed to be greater than 96 bits.
- Will perform Automatic Preamble Generation (APG) if the optional APG is selected.
- Detects end of-frame using the DPLL.

- When NOT in the retime mode, the DPLL, APG and FIFO are bypassed, and the output is taken from the selected input without any flip-flop delays (gate delays only).

CARRIER AND DATA INPUTS

When an input has a signal present, the carrier will be detected on the appropriate pin (CO-C11). The carrier input is user selected for either external squelch (with external one-shots) or internal squelch (a 2μS pulse stretcher is added by the HUB chip). MODE2 = 0 selects external squelch, and MODE2 = 1 selects internal.

Note, a carrier input must be active for at least three clock samples for it to be recognized by the chip. Any isolated pulse less than three clock samples wide will be ignored. However, when using internal carrier squelch, the carrier must be active for at least one clock sample time every 2μS to be considered valid beyond the initial carrier recognition. When not using internal squelch, the carrier must be active during the entire frame to avoid data loss. Ignoring carrier spikes provides extra noise protection and is also referred to as time domain filtering (TDF).

RETIME MODE

The selected valid data input is fed to a digital phase locked loop (DPLL). The DPLL is implemented with a counter which clears on each transition. This gives a jitter tolerance of 167ns peak to peak (83ns peak). This is 40% more tolerance than required by the StarLAN specification.

The valid input is passed through a 9 bit FIFO. Output from the FIFO is prevented until the FIFO is 4 bits full. This is called the 4 bit watermark, and gives the FIFO 4 bits of elasticity which is more than sufficient to absorb the allowable 0.01% clock tolerance.

AUTOMATIC PREAMBLE GENERATOR

If APG is enabled, preamble generation at the outputs DXD and UXD is started as soon as the DPLL acquires lock. When the FIFO reaches the 4 bit watermark, the output data are taken from the FIFO. The APG keeps the preamble from "shrinking" as a frame is passed from HUB to HUB. Without APG, a HUB chip will lose an average of 2 preamble bits, but with APG, an average of 2 preamble bits are gained. This two bit gain should be taken into account by system designers.

AUTOMATIC COMPENSATION FOR WIRING REVERSAL

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK5030 will automatically compensate for this reversal on a per port basis. Any frame that is received with inverse polarity will be detected and will be transmitted on the DXD and UXD pins with the correct polarity. This polarity compensation is active only while in the retime mode.

MINIMUM FRAME LENGTH ENFORCEMENT

When minimum frame length enforcement (FLE) is enabled (MODE6 = 1) and the MK5030 is in retime mode, the input carrier is assumed to be valid for at least 96 bit times. If either the incoming carrier goes inactive or EOF is detected prior to 96 bit times, the MK5030 will send collision presence (CP) for the remainder of the 96 bit times. This feature is important in multi-port environments where signal superposition may cause early carrier dropout. NOTE : IEEE standards committee is, at the printing, still defining FLE. The actual length guaranteed is subject to change.

NO-RETIME MODE

If the retime mode is disabled, then the DPLL, FIFO, and APG are bypassed. The outputs, DXD and UXD,are taken from the selected input without clocked delays (i.e., flip-flops). There are gate delays only. End-of-frame is detected by a counter instead of the DPLL. The advantage of the no-retime mode is that two HUBs cascaded together will appear to the network as one. See figure 3. In no-retime mode, an average of 2 bits will be lost as outputs are enabled after the first rising edge of the incoming data.

PROTECTION TIME

At the end of each frame, all carrier inputs are ignored for 20μS. This is called the protection time and insures immunity to post end-of-frame spikes caused by transformer coupling.

Figure 5 : MK5030 HUB Block Diagram.

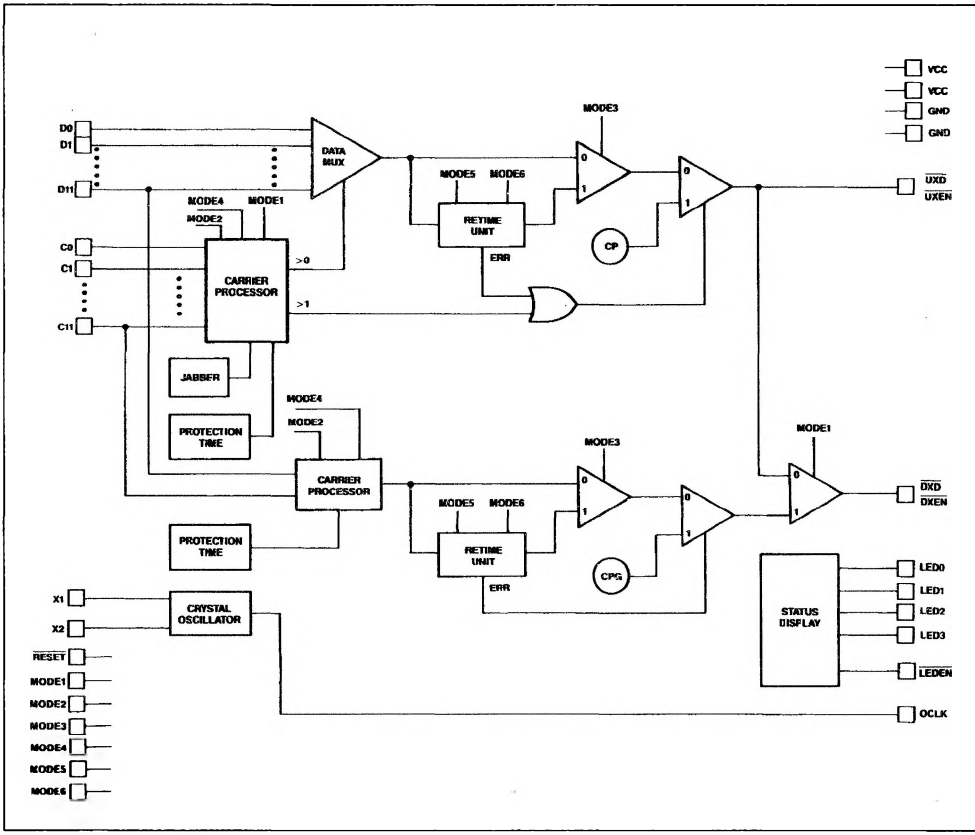
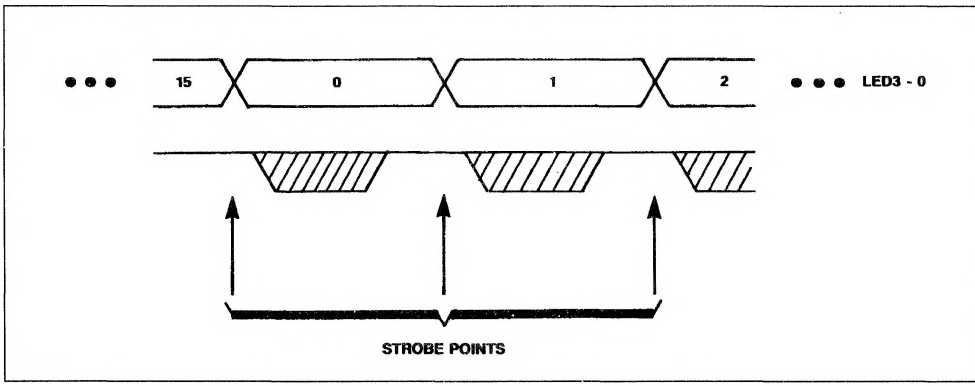


Figure 6 : Scan Display Timing.



COLLISION

A collision is defined when any one of the following five conditions exists : a. Multiple carrier inputs ; b. Manchester code violations ; c. FIFO underflow/overflow exception. d. PLL lock acquisition timeout ; e. frame length violation. An IEEE defined collision presence (CP) code is placed on the UXD output. The starting point of the CP sequence is adjusted to allow faster CP detection by the remote station or HUB. The HUB chip is fully upward compatible with the existing AT&T release 1 CP signal.

JABBER

If a station transmits data for greater than 27mS (which allows twice its normal maximum frame size) then the HUB will output a CP signal. This should correct the error in the station in most cases. However, if that station continues to transmit for up to a total time of 54mS, then the station is "jabbed". This means that the jabber function in the HUB chip will ignore that input and, in effect, remove the station from the network. If the "jabbed" station goes silent and then is the originator of new data, the station is allowed back onto the network by the HUB chip.

Thus, StarLAN networks automatically adjust as portions of the network fail and are repaired.

THE DOWNLINK MODULE

The downlink is identical to the uplink except without the multiplexer, frame length enforcement, and jabber functions. In the intermediate mode (MODE1 = 1), port 11 is a downlink input connected to the next "higher" HUB downlink output. See fig. 3. In the high-end mode (MODE1 = 0), all twelve ports feed the uplink, and DXD-DXEN are internally connected to UXD-UXEN.

STATUS DISPLAY

Two display modes are supported : static and scan. When LEDEN is externally tied to GND, then LED0 - LED3 provide static status information. When LEDEN is externally tied to VCC through a pull-up resistor, then an external demultiplexer (such as a 74154) may be used to provide 16 lines of status information. See Figures 4 and 6, and also see the description of pins LED0 - LED3.

OSCILLATOR

The MK5030 will accept two forms of clock input : a CMOS input or a crystal. If pin X2 is left unconnected, a 6.0MHz ± 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 6.0 ± 0.005% parallel resonant crystal is needed to insure the ± 0.01% frequency accuracy required for StarLAN. Refer to figure 7. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

OCLK provides a TTL CMOS level clock output useful for cascading HUB chips or driving surrounding logic.

RESET INPUT

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. In addition, if the mode inputs are changed after the application of power, reset must be reapplied. If either MODE1 or MODE3 is changed, an internal reset is generated automatically. Refer to fig. 8.

Figure 7 : Oscillator Operation.

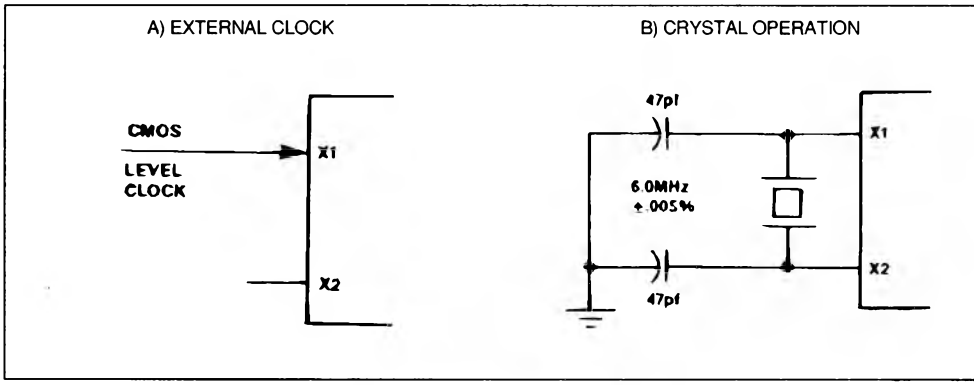
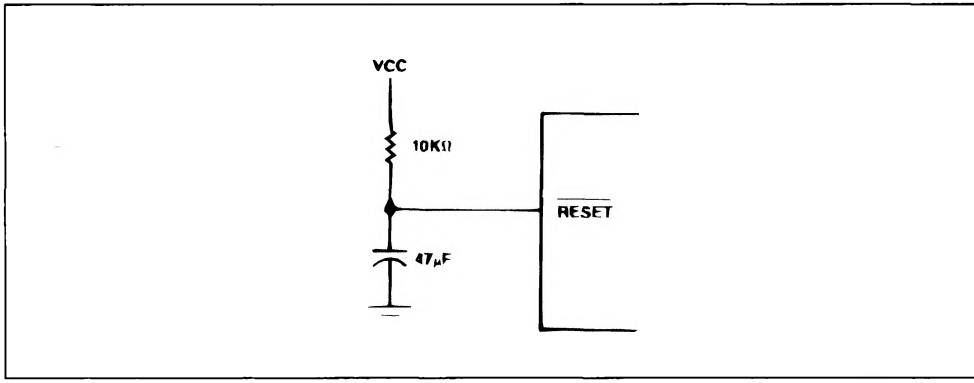


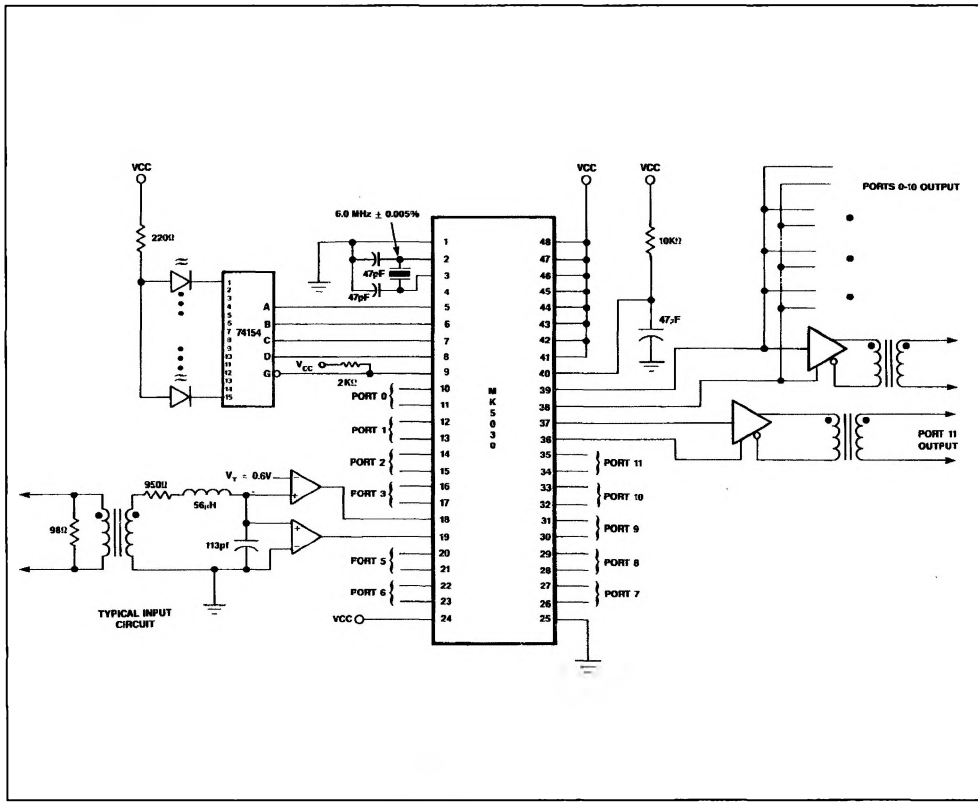
Figure 8 : Typical RC Connection for Power-On Reset.



SYSTEM PERFORMANCE CONSIDERATIONS USING THE MK5030

The MK5030 has several modes of operation. This allows designers flexibility in their design. Figure 9 shows a typical circuit diagram.

Figure 9 : MK5030 External Component Diagram.



ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance, and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (figure 10) and HUB Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Temperature under Bias	− 25 to + 100	°C
	Storage temperature	− 65 to + 150	°C
	Voltage on any Pin with Respect to Ground	− 0.5 to V_{CC} + 0.5	V
	Power Dissipation (no load)	125	mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = + 5V ± 5% unless otherwise specified.

Symbol	Test Condition	Min.	Max.	Unit
V_{IL}		− 0.5	+ 0.8	V
V_{IH}	Except Pin X1	+ 2.0	V_{CC} + 0.5	V
V_{IH}	Pin X1	+ 3.5	V_{CC} + 0.5	V
V_{OL}	@ I_{OL} = 3.2mA		+ 0.5	V
V_{OH}	@ I_{OH} = − 0.4mA	+ 2.4		V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}		± 10	µA
I_{CC}	@ T_{XI} = 6MHz		25	mA

CAPACITANCE F = 1MHz

Symbol	Test Condition	Min.	Max.	Unit
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = + 5V ± 5% unless otherwise specified, V_{TH} = 2.0V, V_{TL} =0.8V

#	Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	X_1	T_{XIT}	X1 Period	160			ns
2	X_1	T_{XIL}	X1 Low Time	60			ns
3	X_1	T_{XIH}	X1 High Time	60			ns
4	X_1	T_{XIR}	Rise Time of X1	0		10	ns
5	X_1	T_{XIF}	Fall Time of X1	0		10	ns
6	X2	T_{X2}	X2 Delay from X1		30		ns
7	OCLK	T_{OCLK}	OCLK Delay from X1			45	ns
8	$\overline{UXD}$	$T_{\overline{UXD}}$	$\overline{UXD}$ Delay from X1		45	65	ns
9	$\overline{UXEN}$	$T_{\overline{UXEN}}$	$\overline{UXEN}$ Delay from X1		48	75	ns
10	$\overline{DXD}$	$T_{\overline{DXD}}$	$\overline{DXD}$ Delay from X1		48	65	ns
11	$\overline{DXEN}$	$T_{\overline{DXEN}}$	$\overline{DXEN}$ Delay from X1		51	75	ns
12	$\overline{UXD}$	J_{UXD}	Transmit Jitter : $\lvert T_{\overline{UXD}}\uparrow - T_{\overline{UXD}}\downarrow \rvert \div 2$		2	4	ns
13	$\overline{DXD}$	J_{DXD}	Transmit Jitter : $\lvert T_{\overline{DXD}}\uparrow - T_{\overline{DXD}}\downarrow \rvert \div 2$		2	4	ns
14	C0-11	T_{CS}	C0-11 Setup to X1	15			ns
15	C0-11	T_{CH}	C0-11 Hold from X1	15			ns
16	D0-11	T_{DS}	D0-11 Setup to X1	15			ns
17	D0-11	T_{DH}	D0–11 Hold from X1	15			ns
18	D0-11	J_{DIN}	D0-11 Incoming Jitter Tolerance			162	ns
19	$\overline{UXD}$, $\overline{DXD}$	T_{PXD}	Delay from any D Input		42	60	ns
20	$\overline{UXD}$, $\overline{DXD}$	J_{NR}	No Retime Jitter : $\lvert T_{XD}\uparrow - T_{XD}\downarrow \rvert \div 2$		2	4	ns
21	LED0-3	T_{LED}	Delay from X1		50		ns
22	$\overline{LEDEN}$	T_{LEDENR}	Guaranteed Release Time until LED_{0-3} Change		2600		ns
23	$\overline{LEDEN}$	T_{LEDENR}	Delay from LED_{0-3} Transition		2660		ns

Figure 10 : Oscillator Timing Diagram.

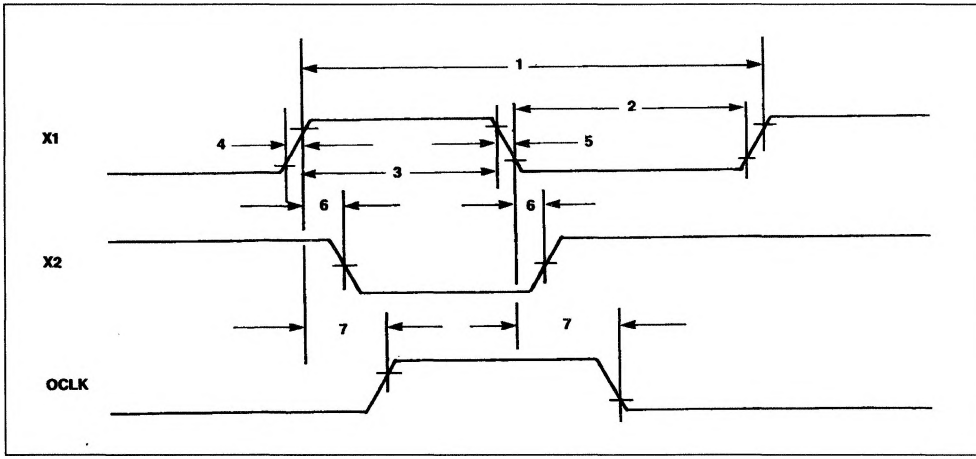


Figure 11 : Retimer Enabled (MODE3 = 1) Timing Diagram.

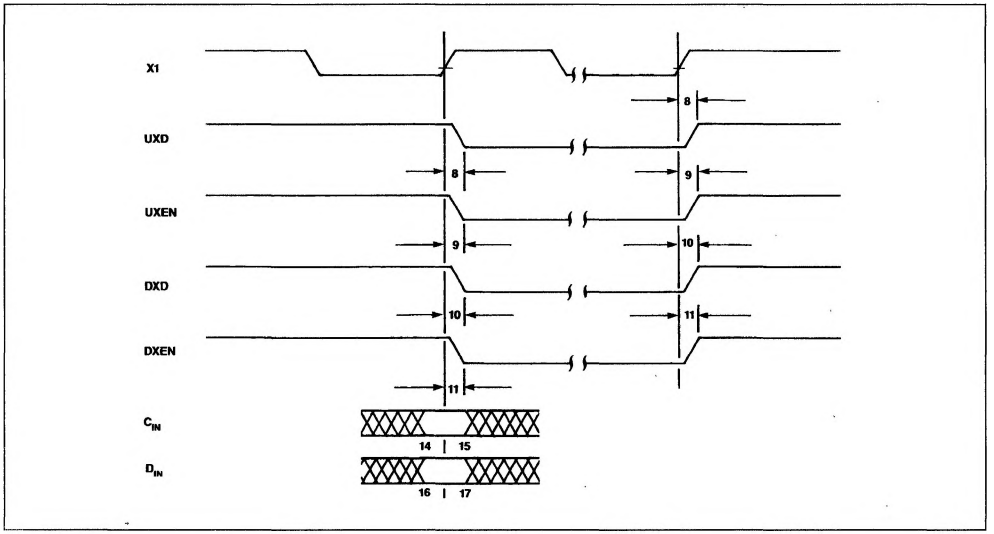


Figure 12 : Retimer Disabled (MODE3 = 0) Timing Diagram.

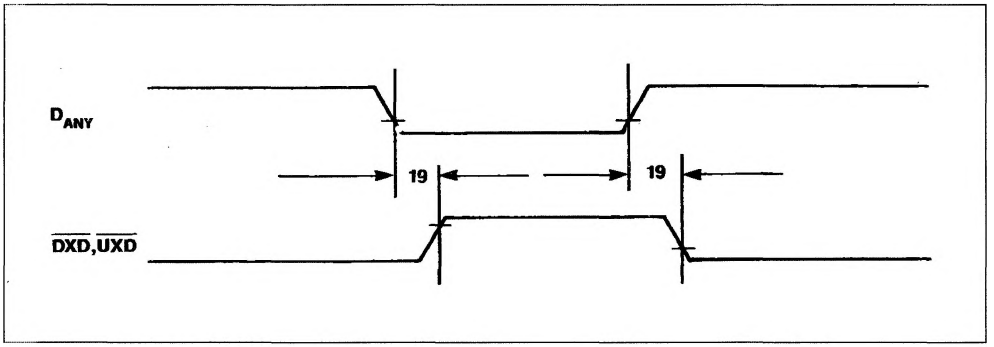


Figure 13 : Status Display Timing Diagram.

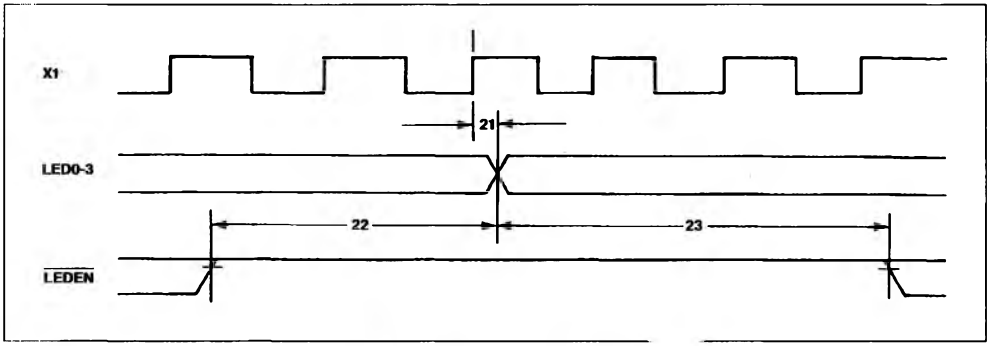
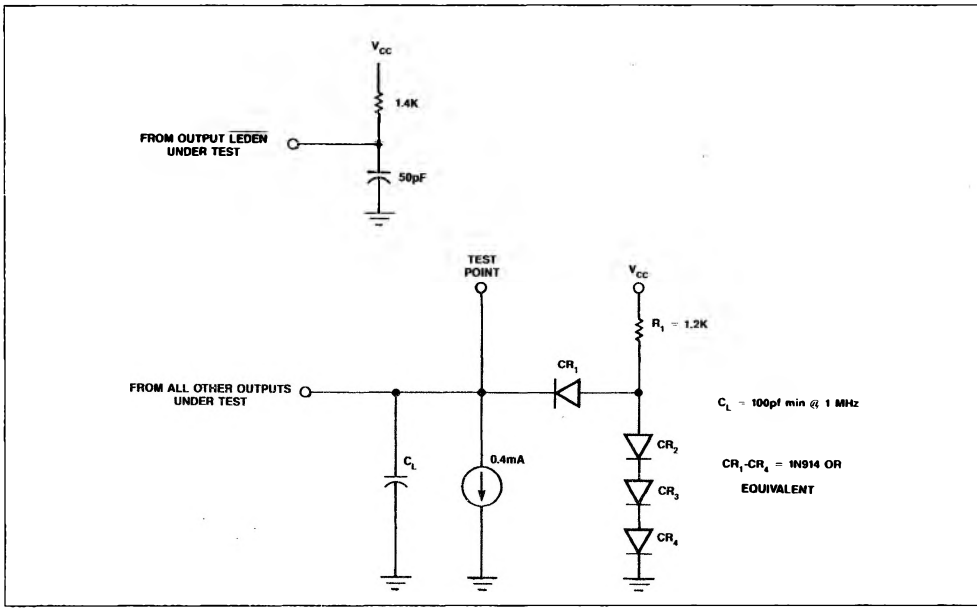


Figure 14 : Output Load Diagram.



GLOSSARY OF TERMS

automatic preamble generator (APG) — An optional circuit in the HUB chip which will begin preamble generation before the FIFO reaches the 4 bit watermark. The APG replaces a 2 bit loss in the preamble through a HUB with a 2 bit gain. See Retime Mode.

protection time — A 20µS period at the end of each frame where all carrier inputs are ignored. This protection insures immunity to post end-of-frame spikes caused by transformer coupling. See Protection Time.

downlink — The data path going from a "higher" HUB to the next "lower" HUB, or going from a HUB back to the stations.

high-end hub — A HUB that does not connect to another "higher" HUB. The downlink outputs, DXD and DXEN, are internally connected to the uplink outputs, UXD and UXEN.

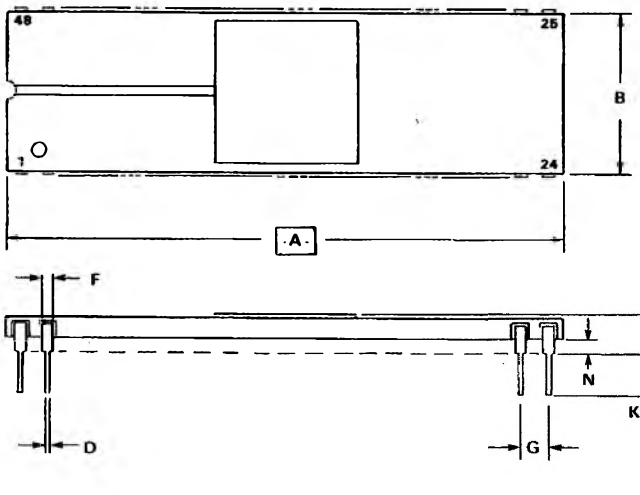
intermediate hub — A HUB that connects to another "higher" HUB. Pins C11 and D11 must be used as downlink inputs.

jabber — A circuit module inside the HUB chip which protects the network from a station which is constantly transmitting. See Jabber.

uplink — The data path going from a "lower" HUB to the next "higher" HUB, or going from the stations to a HUB.

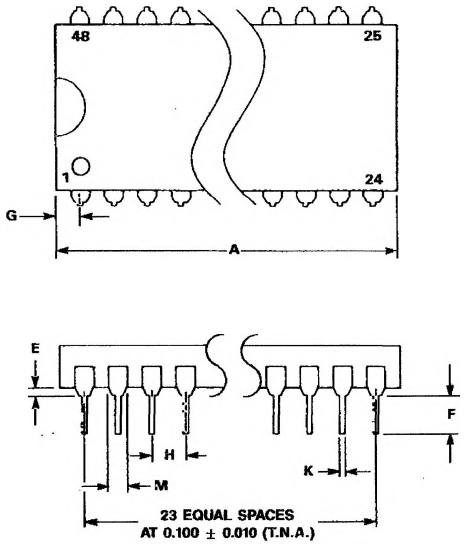
PACKAGE DESCRIPTION

48 Pin Ceramic - MK5030P



DIM.	INCHES	
	MIN	MAX
A	2.376	2.424
B	0.576	0.604
C	0.120	0.160
D	0.015	0.021
F	0.030	0.055
G	0.100 BSC	
J	0.008	0.013
K	0.100	0.165
L	0.590	0.616
M	0°	10°
N	0.040	0.060

48 Pin Plastic - MK5030N



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	61.468	62.738	2.420	2.470
B	14.986	16.256	.590	.640
C	13.462	13.97	.530	.550
D	3.556	4064	.140	.160
E	0.381	1.524	.015	060
F	3048	3.81	.120	.150
G	1.524	2.286	.060	.090
H	1.186	1.794	.090	.110
J	15.24	17.78	.600	.700
K	0.381	0.533	.015	.021
L	0.203	0.305	.008	.012
M	1.143	1.778	.045	.070