MK 50240/1/2P
MK 50240/1/2N

MOS Top Octave Frequency Generator

MOSTEK®

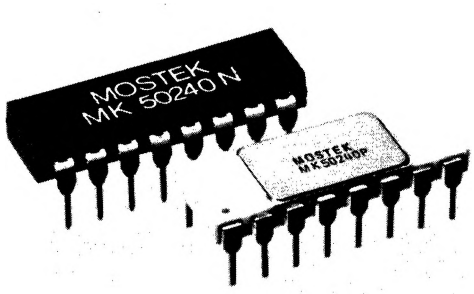
FEATURES

- ☐ Single Power supply
- ☐ Broad supply voltage operating range
- ☐ Low power dissipation
- ☐ High output drive capability

MK 50240 – 50% Output Duty Cycle

MK 50241 – 30% Output Duty Cycle

MK 50242 – 50% Output Duty Cycle



DESCRIPTION

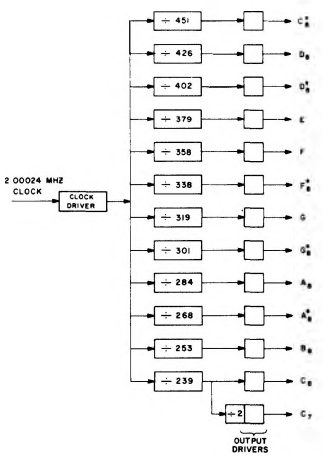
The MK 50240 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

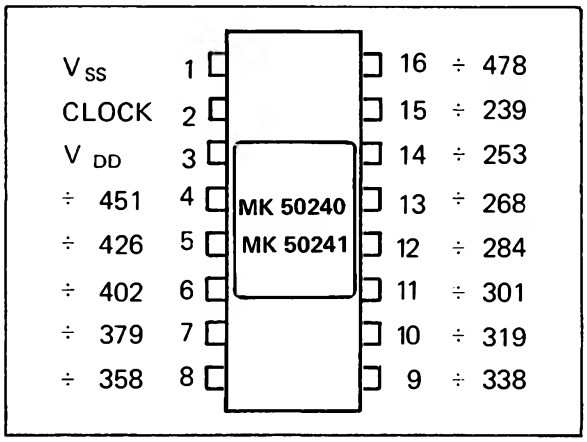
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the MK 50240 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 600 mW of power. The circuits are packaged in 16-pin ceramic dual-in-line packages.

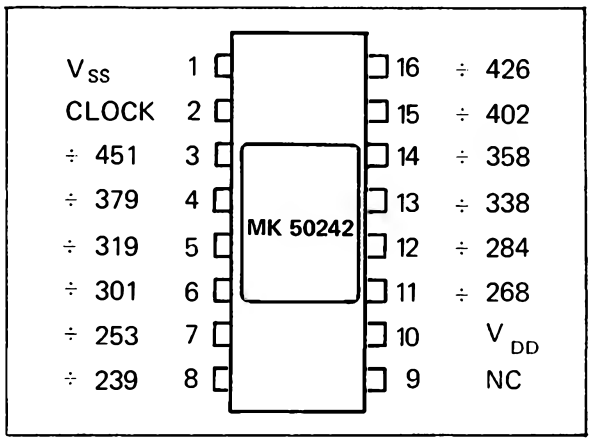
RFI emination and feed-through is minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise-time under no load conditions to reduce the R.F. harmonic content of each output signal.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS





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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3V to −20V

Operating Temperature (Ambient)..... 0°C to 50°C

Storage Temperature (Ambient)..... −40°C to 100°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 50°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−15.0	−16.0	V	

ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 50°C$; V_{SS} = 0, V_{DD} = −11 to −16V unless otherwise specified)

	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V_{IL}	Input Clock, Low	0		−1.0	V	FIG. 1
V_{IH}	Input Clock, High	V_{DD} + 1.0		V_{DD}	V	
f_I	Input Clock Frequency	100	2000.240	2500	kHz	
t_r , t_f	Input Clock Rise & Fall Times 10% to 90% @ 2.5 MHz			30	nsec	FIG 1
t_{on} , t_{off}	Input Clock On and Off Times @ 2.5 MHz		200		nsec	FIG. 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ .70 mA	V_{DD} + 1.5		V_{DD}	V	FIG. 2
V_{OL}	Output, Low @ .75 mA	V_{SS} − 1.0		V_{SS}	V	FIG. 2
t_{ro} t_{fo}	Output Rise & Fall Times, 500 pF Load	250		2500	nsec	FIG. 3
t_{on}, t_{off}	Output Duty Cycle MK 50240P & MK 50242P MK 50241P (Pin 16 50%)		50 30		% %	
I_{DD}	Supply Current		24	37	mA	outputs unloaded

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FIGURE 1
INPUT CLOCK WAVEFORM

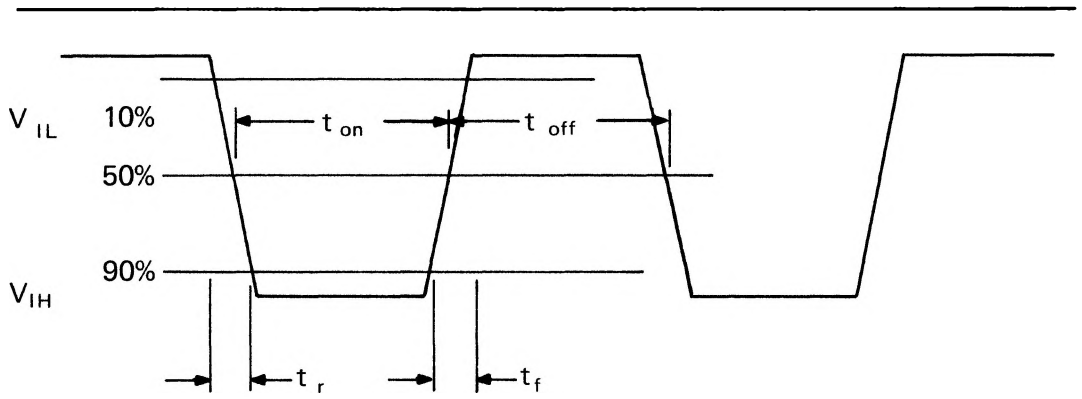
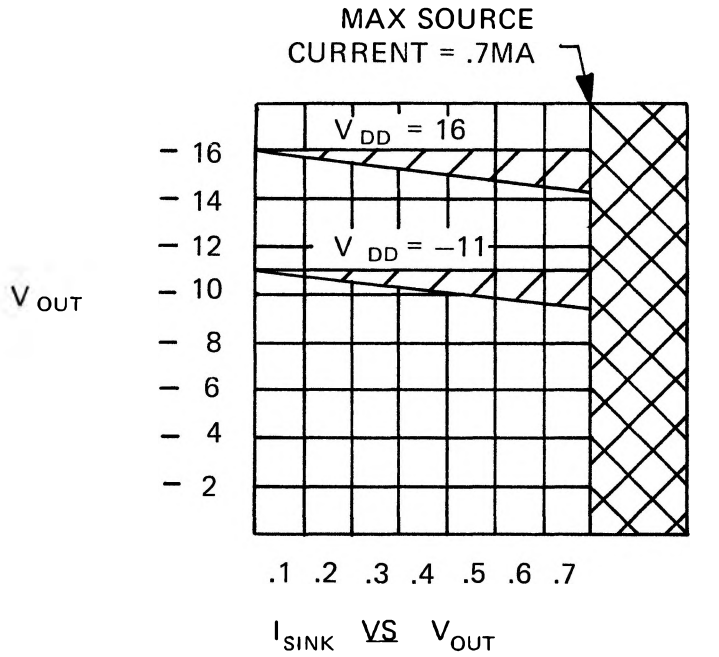
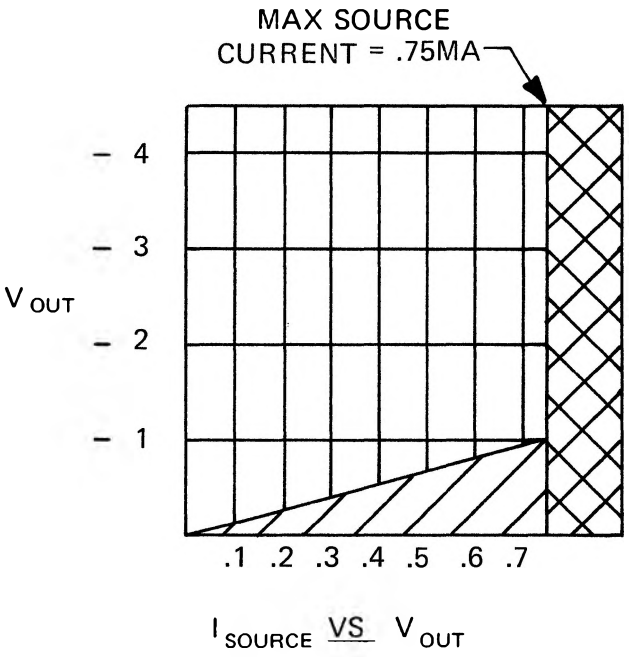


FIGURE 2
OUTPUT SIGNAL D. C. LOADING





SINK CURRENT TO CHIP V_{DD} — (OPERATING AREA)

SINK CURRENT FROM CHIP V_{SS} — (CURRENT OVERLOAD AREA)

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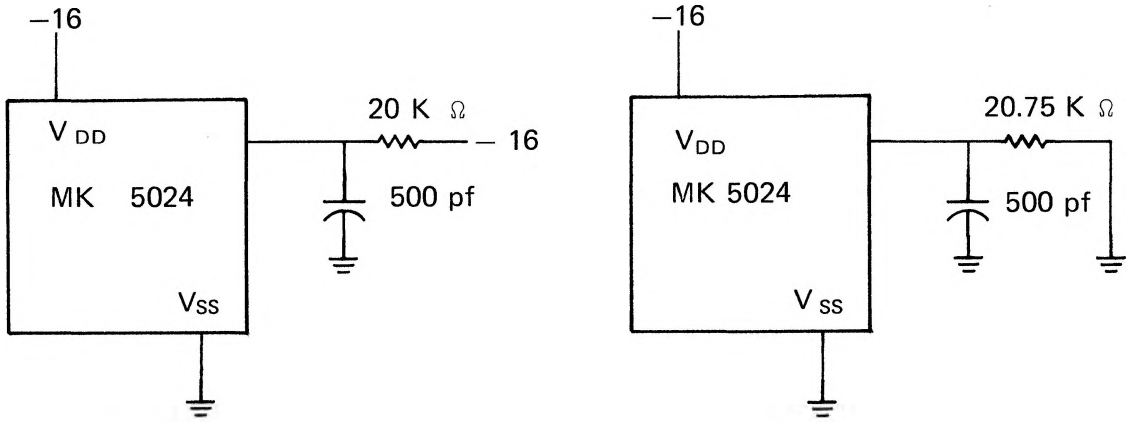
FIGURE 3
OUTPUT LOADING

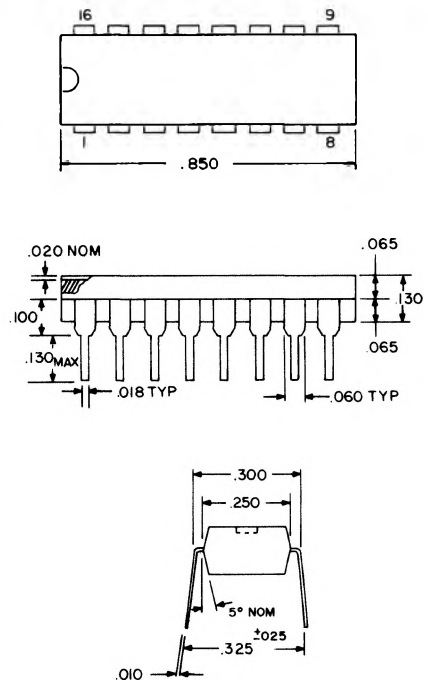


t_{fo} Test

t_{ro} Test

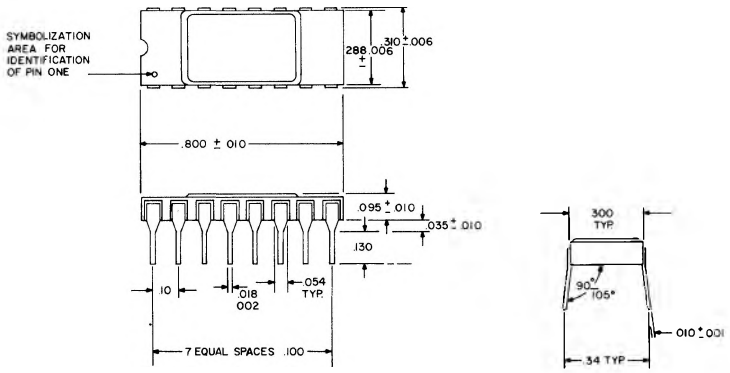
PHYSICAL DESCRIPTION

16–lead plastic dual-in-line hermetic package



Suffix N

16–lead side brazed ceramic dual-in-line hermetic package



Suffix P

NOTE:

A. Pin 1 indicated by index dot
B. All dimensions in inches

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