



HIGH SPEED 4K x 9 / 8K x 9 CMOS BIPORT™ FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 4K x 9, 8K x 9 ORGANIZATIONS
- LOW POWER, HIGH PERFORMANCE HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL AND RATE BUFFER APPLICATIONS
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE

DESCRIPTION

The MK45H04 and MK45H08 are members of the BiPORT FIFO Family from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half-full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of W (write), and R (read) input pins. Separate data in (D₀-D₈) and data out (Q₀-Q₈) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is as a rate buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H04 and MK45H08 incorporate 9-bit wide data arrays that provide for support control or parity bit functions.

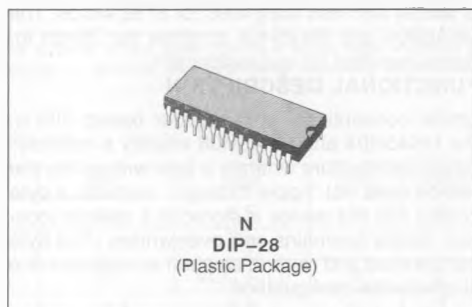
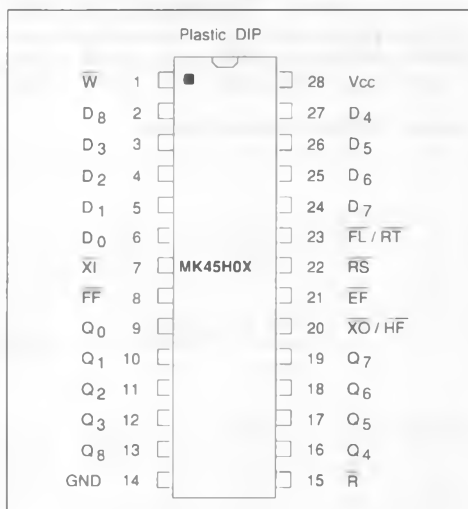


Figure 1 : Pin Connections.



PIN NAMES

W	= Write	XI	= Expansion in
R	= Read	XO	= Expansion out
RS	= Reset	FF	= Full Flag
FL/RT	= First Load/ Retransmit	EF	= Empty Flag
		HF	= Half-full Flag
D ₀₋₈	= Data in	V _{CC}	Power, + 5 Volts
Q ₀₋₈	= Data out	GND	= Ground

This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit (RT) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 4096, or 8192 words. The MK45H04 and MK45H08 continue our 28-pin industry standard pin-out assignment.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45H04 and MK45H08 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

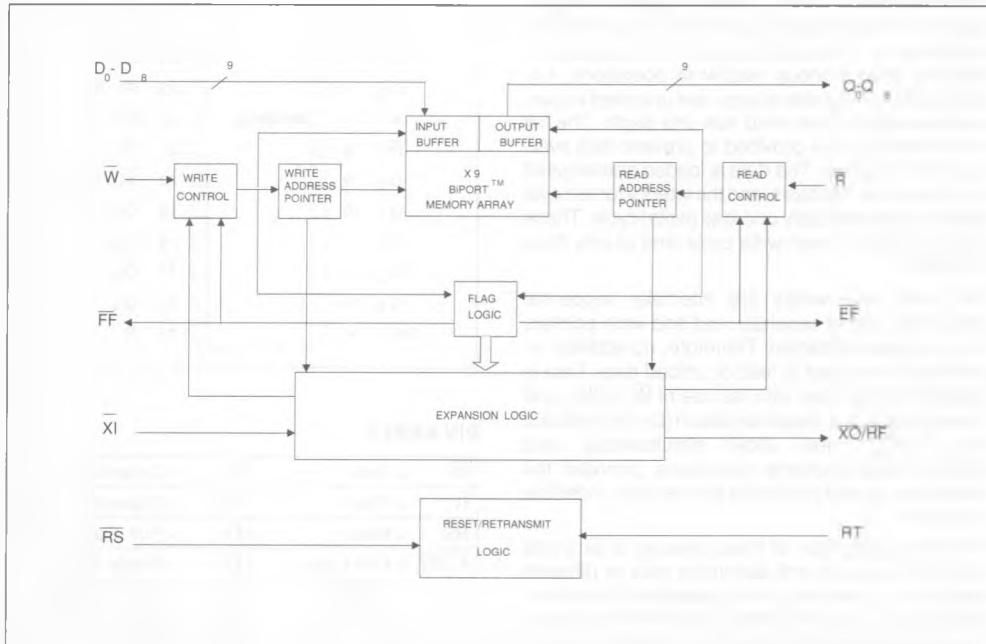
Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte

stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (4096 or 8192). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable in ripple through delays. The MK45H04 and MK45H08 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows connecting the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in (XI) and expansion-out (XO) pins.

Figure 2 : MK45HOX Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	- 0.3 to + 7.0	V
Operating Temperature	0 to + 70	°C
Storage Temperature	- 55 to + 125	°C
Power Dissipation	1	Watt
Output Current	20	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{CC}	Supply Voltage	4.5	5.5	V	3
GND	Ground	0.0	0.0	V	
V_{IH}	Logic 1 all Inputs	2.0	$V_{CC} + 1.0$	V	3
V_{IL}	Logic 0 all Inputs	- 0.3	0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) ($V_{CC} = 5.0 \pm 10\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
I_{CC1}	Average VCC power Supply Current		120	mA	6
I_{CC2}	Average Standby Current ($\bar{R} = \bar{W} = \bar{RS} = \bar{FL/RT} = V_{IH}$)		12	mA	6
I_{CC3}	Power Down Current (Inputs $\geq V_{CC} - 0.2V$)		2	mA	6
I_{IL}	Input Leakage Current (any input)	- 1.0	1.0	μA	4
I_{OL}	Output Leakage Current	- 10.0	10.0	μA	5
V_{OH}	Output Logic 1 Voltage ($I_{OUT} = -4.0\text{mA}$)	2.4		V	3
V_{OL}	Output Logic 0 Voltage ($I_{OUT} = 8.0\text{mA}$)		0.4	V	3

AC ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Capacitance on Input Pins		8	pF	8
C_O	Capacitance on Output Pins		12	pF	8.9

Notes : 8. Sampled : not 100% tested.

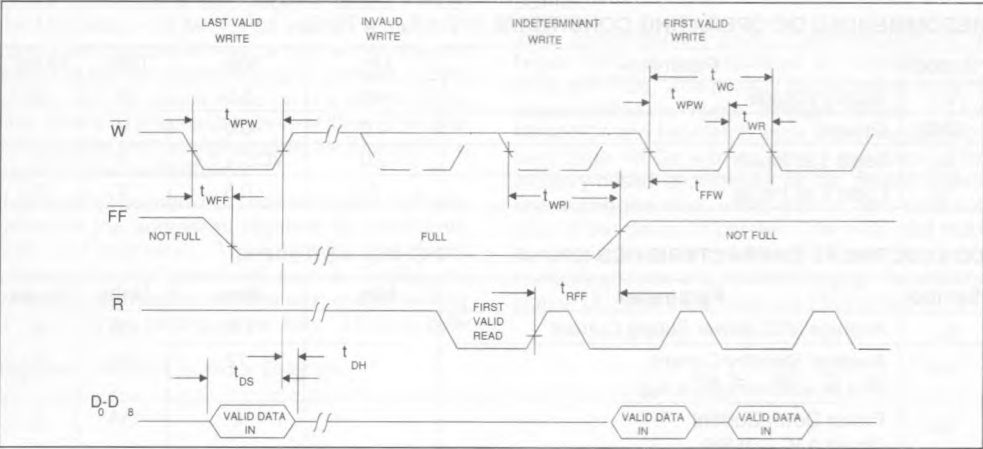
9. Output buffer deselected.

WRITE MODE

The MK45H0X initiates a Write Cycle (see Figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK45H0X becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go

high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that the second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3A : Write and Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5.0volts ± 10%)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{WC}	Write Cycle Time	35		45		65		80		140		ns	
t _{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t _{WR}	Write Recovery Time	10		10		15		15		20		ns	
t _{DS}	Data Set Up Time	15		18		30		30		40		ns	
t _{DH}	Data Hold Time	0		0		0		0		0		ns	
t _{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		30		35		45		60		60	ns	2
t _{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t _{RFF}	$\overline{R}$ High to $\overline{FF}$ High		30		35		45		60		60	ns	2
t _{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

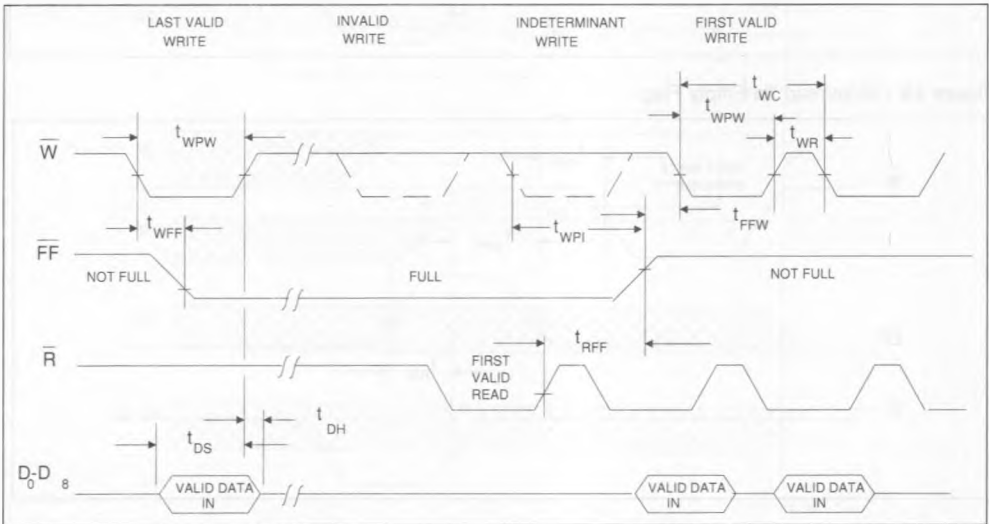
READ MODE

The MK45H0X initiates a Read Cycle (see Figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the read mode of operation, the MK45H0X provides a very fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all the data has been read from the

FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE Operation. $\overline{EF}$ will again go low t_{REF} from the beginning of a subsequent read operation, provided that a second WRITE has not been completed (see Figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 3B : Write And Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5.0\text{volts} \pm 10\%$)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		30		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Figure 4A : Read/write To Full Flag.

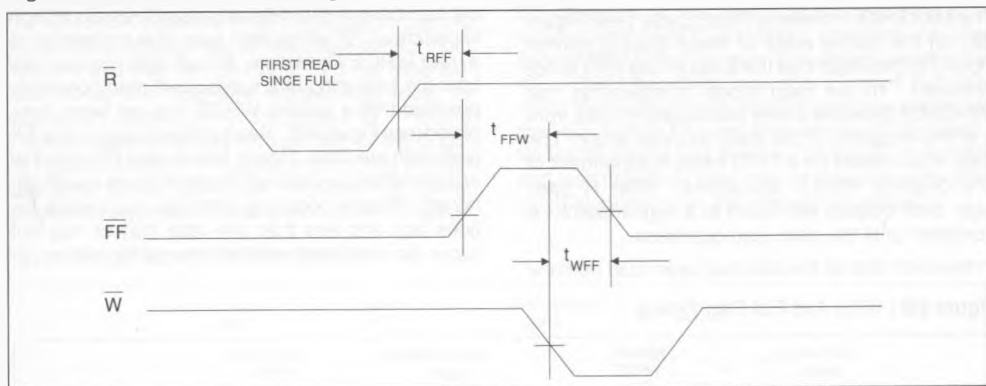
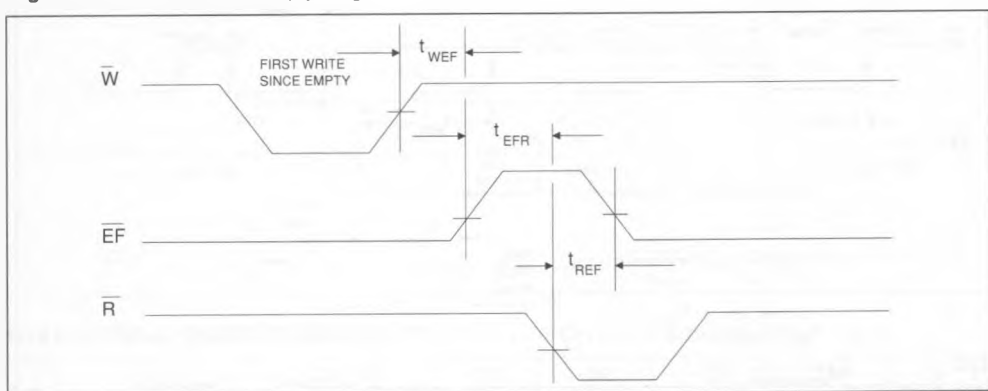


Figure 4B : Write/read To Empty Flag.

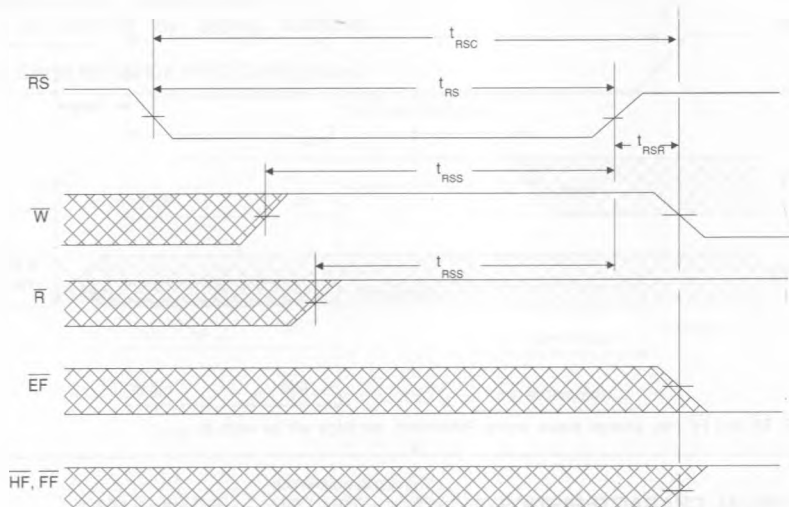


RESET

The MK45H0X is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need to be high when $\overline{RS}$ goes low, both $\overline{R}$ and $\overline{W}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSS} afterwards. Refer to the following discussion for the required state of $\overline{FL/RT}$ and $\overline{XI}$ during Reset.

Figure 5 : Reset.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC} .

AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5.0\text{volts} \pm 10\%$)

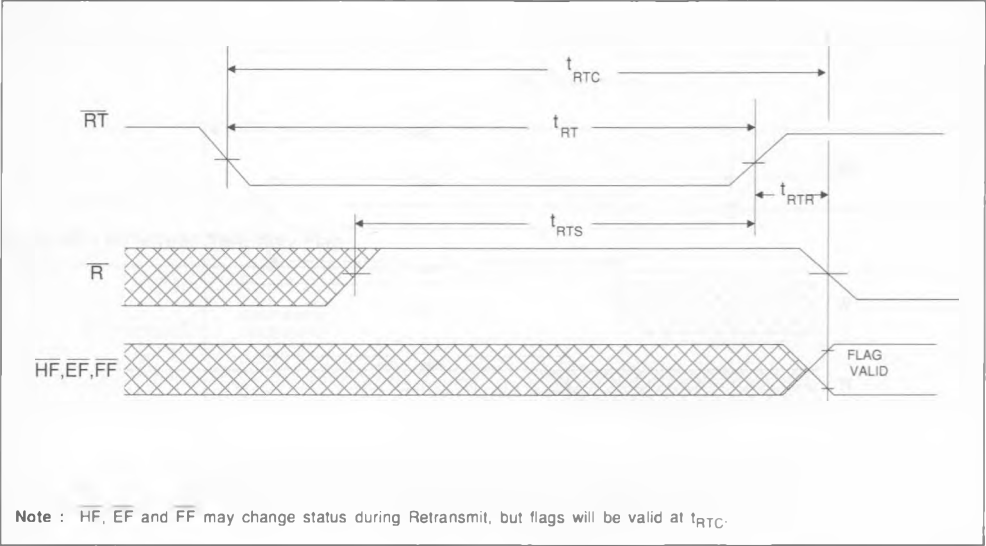
Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

RETRANSMIT

The MK45H0X can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (see Figure 6). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write

pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards. The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 6 : Retransmit.



AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) ($V_{CC} = +5.0\text{volts} \pm 10\%$)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Setup Time	25		30		30		45		100		ns	

SINGLE DEVICE CONFIGURATION

A single MK45H0X may be used when application requirements are for a depth of the device depth or less. The MK45H0X is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK45H0Xs. Any word width can be attained by adding additional

MK45H0Xs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and the read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation. See Figure 9.

Figure 7 : A Single MK45H0X FIFO Configuration.

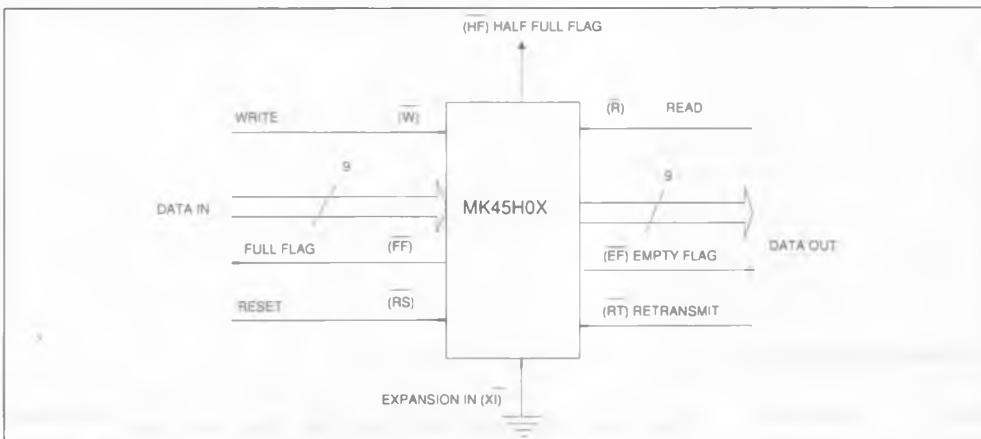
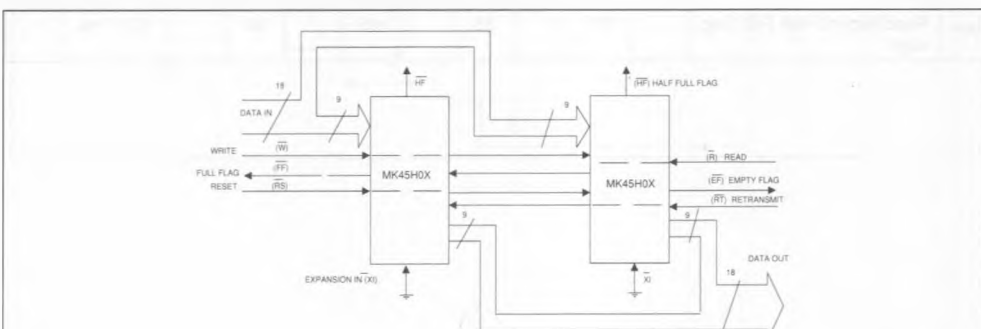


Figure 8 : MK45H0X Width Expansion FIFO Configuration.



Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

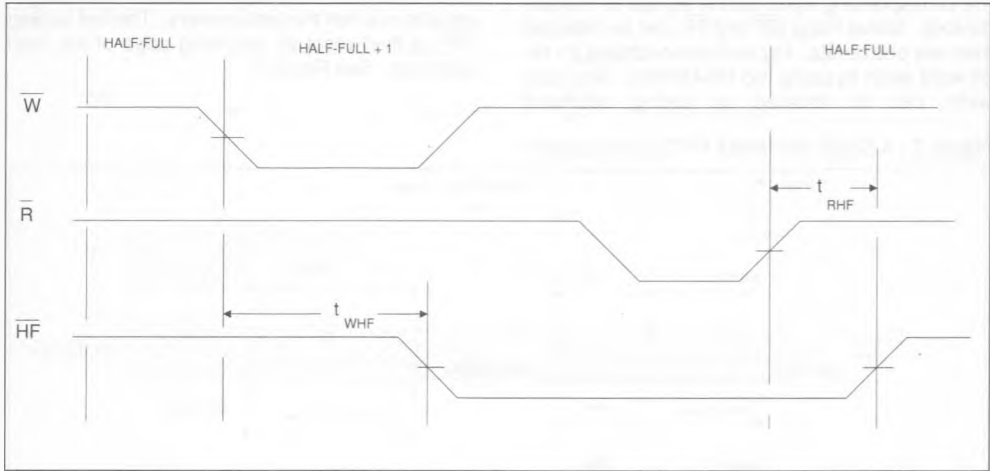
DEPTH EXPANSION (DAISY CHAIN)

The MK45H0X can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 10 demonstrates Depth Expansion using two MK45H0Xs. Any depth can be attained by adding additional MK45H0Xs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the EFs and the ORing of all the FFs (i.e., all must be set to generate the composite FF or EF).

The MK45H0X operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions:

Figure 9 : Half Full Flag Timing.



AC CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5volts ± 10%)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t _{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

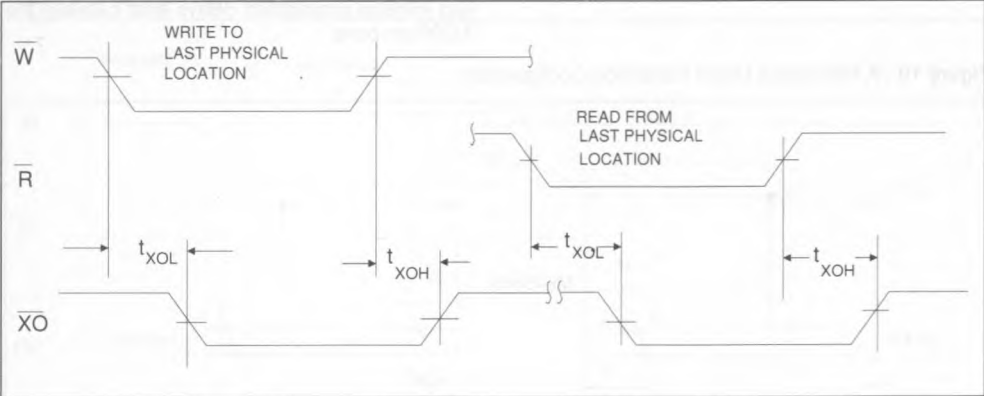
Figure 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In as much as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with the actual timing in the normal Depth Expanded application unless extreme propagation delays exist between the XO/XI pin pairs.

[illegible]

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH} . The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and

Empty Flags are activated, which is in response to writing and reading a last available location.
When in Depth Expansion mode, a given MK45H0X will begin writing and reading as soon as valid $\overline{A}WRITE$ and $\overline{A}READ$ signals begin, provided FL was grounded at RESET time.

Figure 11 : Expansion Out timing.



AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5.0\text{volts} \pm 10\%$)

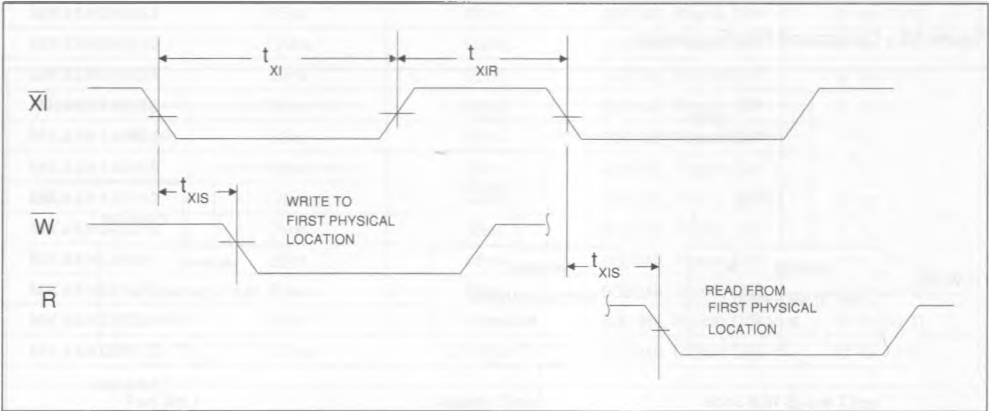
Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

A MK45H0X in Depth Expansion mode with $\overline{\text{FL}}$ high at RESET will not begin writing until after an expansion in pulse occurs.

It will not begin reading until a second Expansion In pulse and the Emph Flag has gone high. Expansion

In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI} , and recovery time, t_{XIR} , must be observed.

Figure 12 : Expansion In Timing.



AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) ($V_{\text{CC}} = +5.0\text{volts} \pm 10\%$)

Sym.	Parameter	- 25		- 35		- 50		- 65		- 120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion in Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion in Setup Time	15		15		15		15		15		ns	

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

Applications which require data buffering between two systems (each system capable of READ and

WRITE operations), can be achieved by pairing MK45H0Xs as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., FF is monitored on the device where W is used; EF is monitored on the device where R is used.) Both Depth Expansion and Width Expansion may be used in this mode.

Figure 13 : Compound Fifo Expansion.

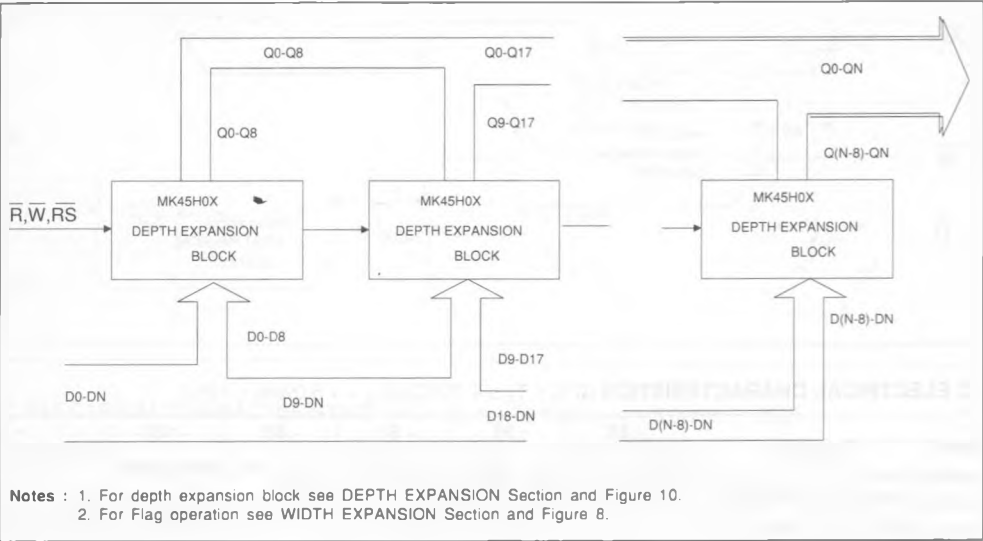
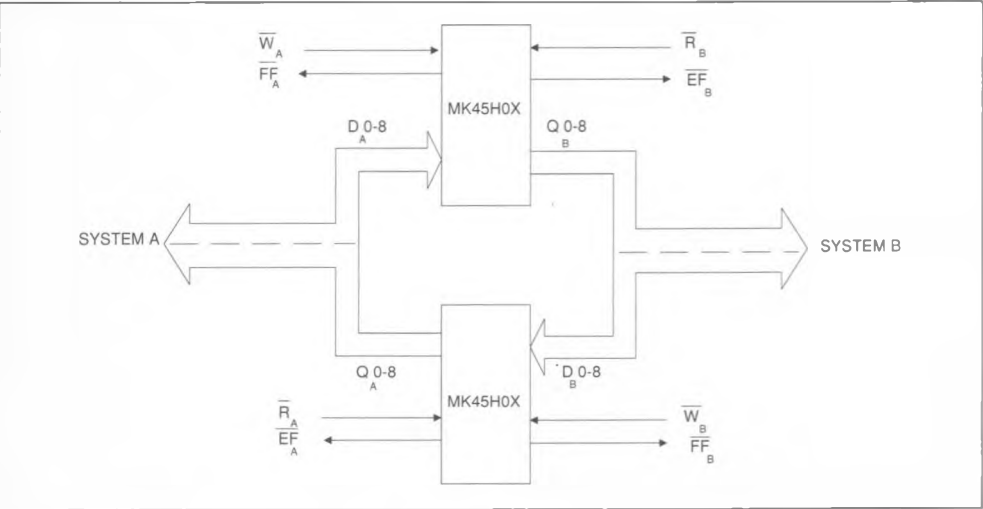


Figure 14 : Bidirectional Fifo Application.



ORDER CODES

Part No	Access Time	Cycle Time	Package Type	Temperature
MK45H04N25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H04N12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H14N12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H08N12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C

Part No	Access Time	R/W Cycle Time
MK45H04/08-25	25ns	35ns, 28.5MHz
MK45H04/08-35	35ns	45ns, 22.2MHz
MK45H04/08-50	55ns	65ns, 15.3MHz
MK45H04/08-65	65ns	80ns, 12.5MHz
MK45H04/08-12	120ns	140ns, 7.14MHz

PACKAGE MECHANICAL DATA

Figure 15 : MK45H04 28 Pin Plastic DIP (N) 600 MIL.

