SGS-THOMSON MICROELECTRONICS

MK45H01/02/03(N,K) -25/35/50/65/12

HIGH SPEED 512/1K/2K x 9 CMOS BiPORT™ FIFO

ADVANCE DATA

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS : MK45H01 (512 x 9), MK45H02 (1K x 9), MK45H03 (2K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE

N
DIP–28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

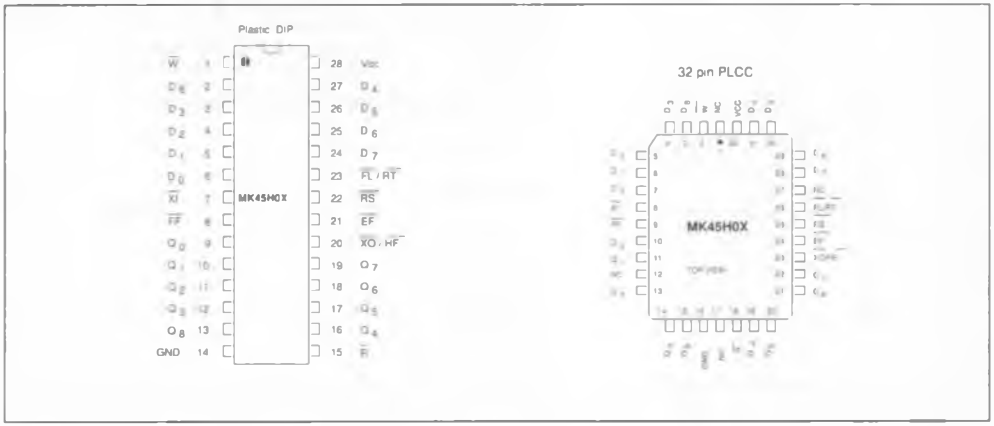
DESCRIPTION

The MK45H01, MK45H02, and MK45H03 are members of the BiPORT FIFO Family from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion In
$\overline{R}$	= Read	$\overline{XO}$	= Expansion Out
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL}/\overline{RT}$	= First Load/ Retransmit	$\overline{EF}$ $\overline{HF}$	= Empty Flag = Half-full Flag
$D_{0\text{-}8}$	= Data In	V_{CC}	Power, +5 V
$Q_{0\text{-}8}$	= Data Out	GND	= Ground

Figure 1 : Pin Connections.



DESCRIPTION (continued)

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of W (write), and R (read) input pins. Separate data in (D_0-D_8) and data out (Q_0-Q_8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

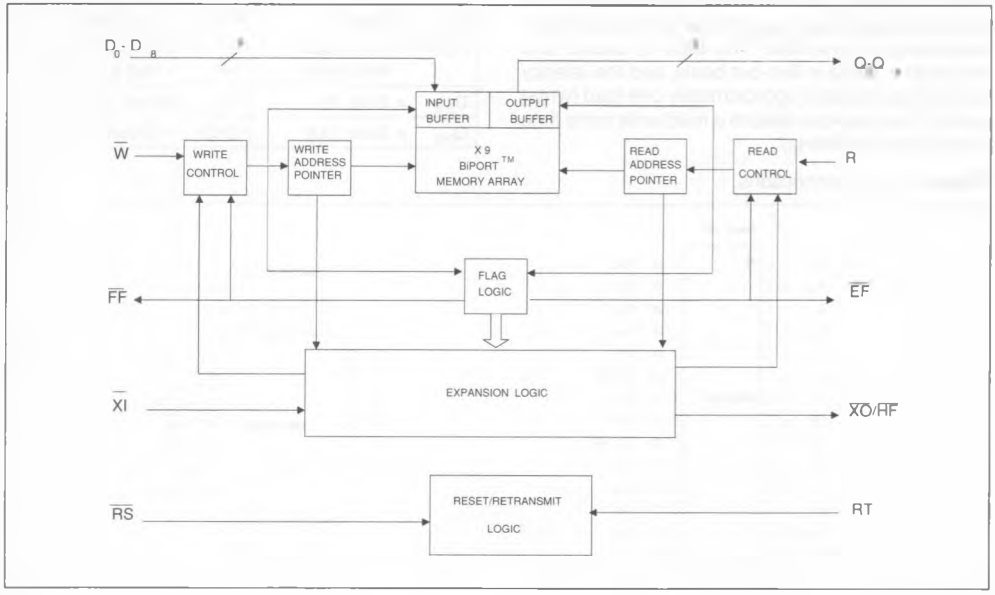
The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H01, MK45H02, and MK45H03 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit (RT) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words. The MK45H01, MK45H02, and MK45H03 continue our 28-pin industry standard pin-out assignment.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45H01, MK45H02, and MK45H03 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Figure 2 : MK45H0X Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to Ground	- 0.3 to + 7.0	V
Operating Temperature	0 to + 70	°C
Storage Temperature	- 55 to + 125	°C
Power Dissipation	1	Watt
Output Current	20	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5		5.5	V	3
GND	Ground	0		0	V	
V_{IH}	Logic "1" Voltage all Inputs	2.0		V_{CC} + 1.0	V	3
V_{IL}	Logic "0" Voltage all Inputs	- 0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average VCC Power Supply Current			120	mA	6
I_{CC2}	Average Standby Current (R = W = RS = FL/RT = VIH)			12	mA	6
I_{CC3}	Power Down Current (Inputs ≥ VCC – 0.2V)			2	mA	6
I_{IL}	Input Leakage Current (Any Input)	– 1.0		1.0	µA	4
I_{OL}	Output Leakage Current	– 10.0		10.0	µA	5
V_{OH}	Output Logic 1 Voltage (IOUT = – 4.0mA)	2.4			Volts	3
V_{OL}	Output Logic 0 Voltage (IOUT = 8.0mA)			0.4	Volts	3

Notes : 1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Circuit.
3. All voltages are referenced to ground.
4. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
5. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
6. I_{CC} measurements are made with outputs open.

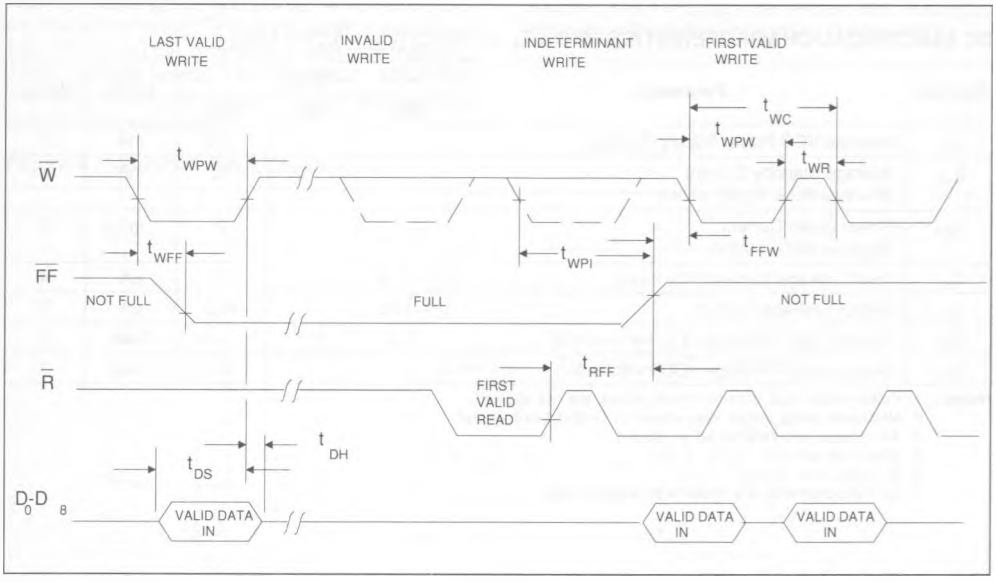
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45H01, MK45H02, and MK45H03 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows connecting the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45H0X initiates a Write Cycle (see figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of W. The data is stored sequentially and independent of any ongoing Read operations. FF is asserted during the last valid write as the MK45H0X becomes full. Write operations begun with FF low are inhibited. FF will go high t_{RFF} after completion of a valid READ operation. FF will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see figure 4A). Writes beginning t_{FFW} after FF goes high are valid. Writes beginning after FF goes low and more than t_{WPI} before FF goes high are invalid (ignored). Writes beginning less then t_{WPI} before FF goes high and less then t_{FFW} later may or may not occur (be valid), depending on internal flag status.

Figure 3A : Write and Full Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

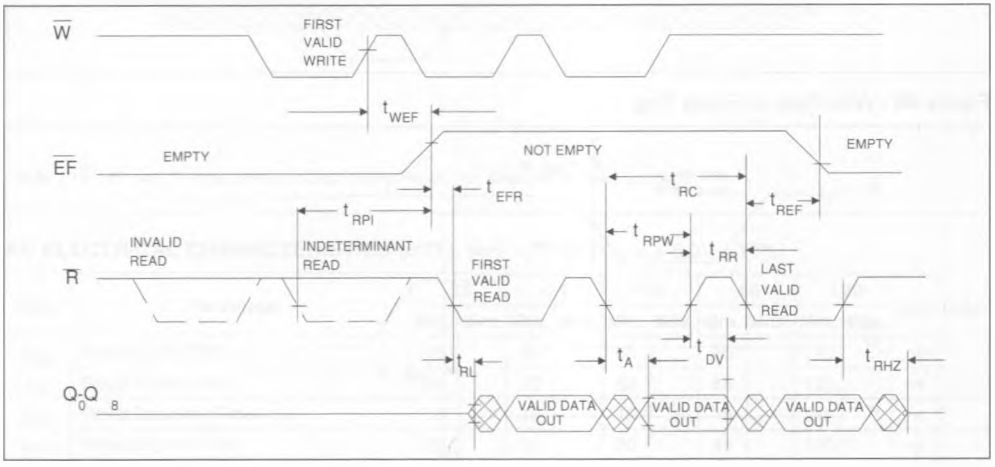
Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		30		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		30		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

READ MODE

The MK45H0X initiates a Read Cycle (see figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the read mode of operation, the MK45H0X provides a fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data inputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 3B : Read and Empty Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		30		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		30		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Figure 4A : Read/Write to Full Flag.

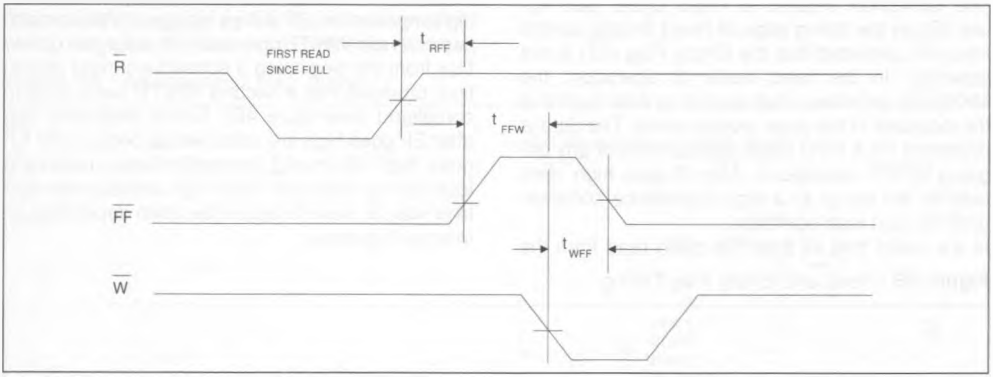
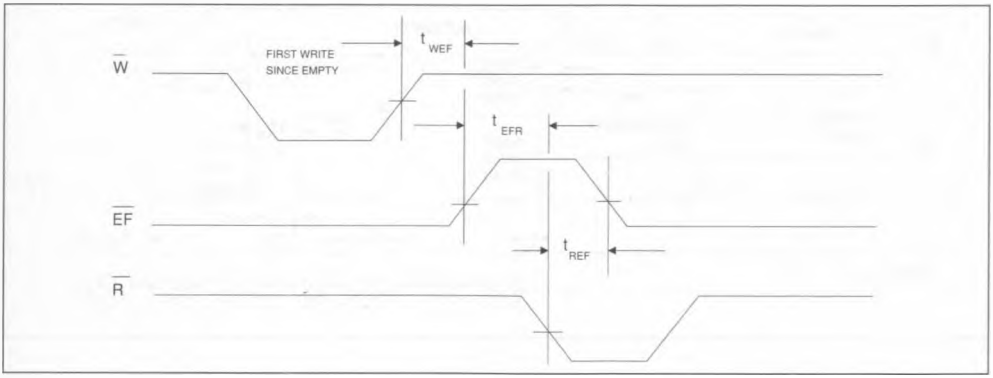


Figure 4B : Write/Read to Empty Flag.

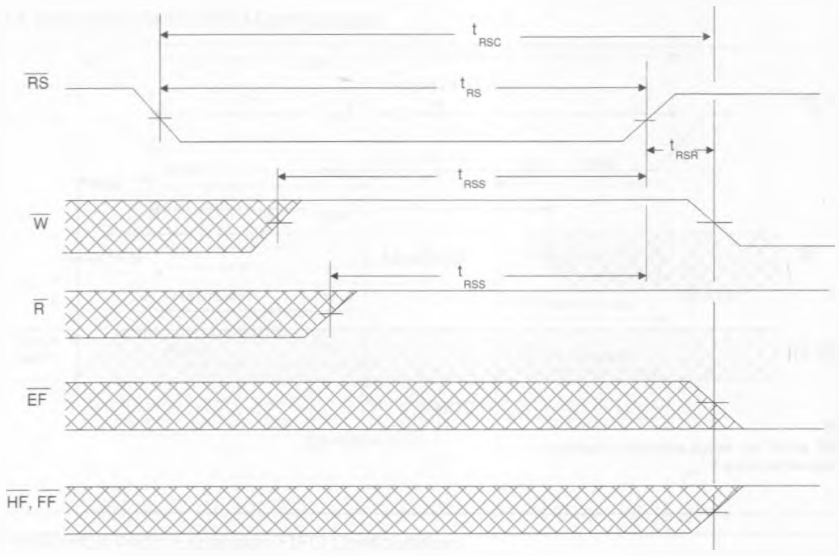


RESET

The MK45H0X is reset (see figure 5) whenever the Reset pin (RS) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both R and W must be high t_{RSS} before RS goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of FL/RT and XI during Reset.

Figure 5 : Reset.



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

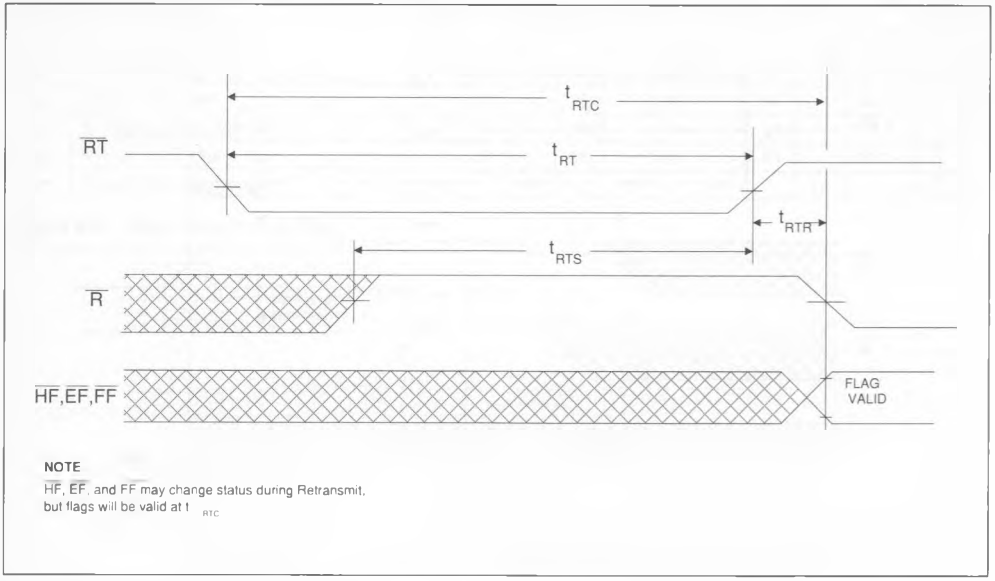
Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

RETRANSMIT

The MK45H0X can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See figure 6). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed bet-ween Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 6 : Retransmit.



AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5.0V ± 10%)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		10		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Setup Time	25		30		30		45		100		ns	

SINGLE DEVICE CONFIGURATION

A single MK45H0X may be used when application requirements are for a depth of the device depth or less. The MK45H0X is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin (XI) grounded (see figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags (EF and FF) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK45H0Xs. Any word width can be attained by adding additional MK45H0Xs. The half full flag (HF) operates the same as in single device configuration.

Figure 7 : A Single MK45H0X FIFO Configuration.

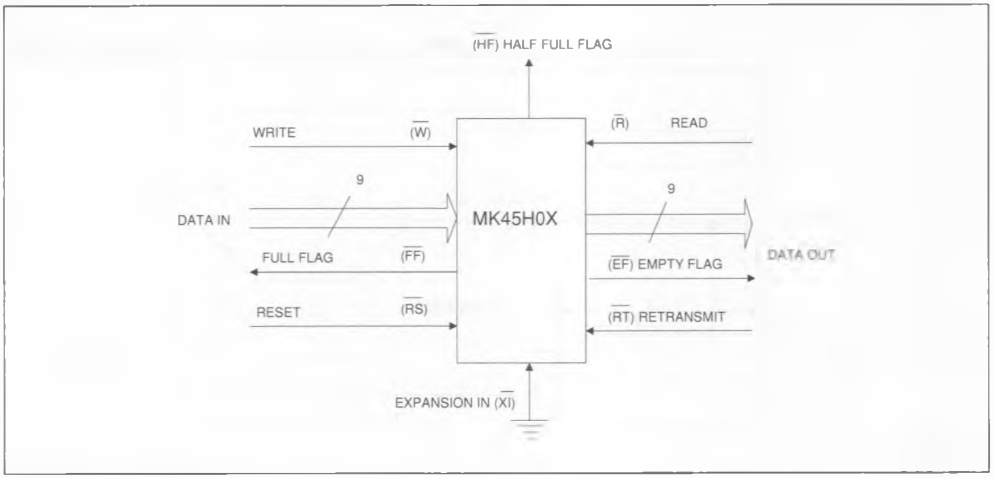
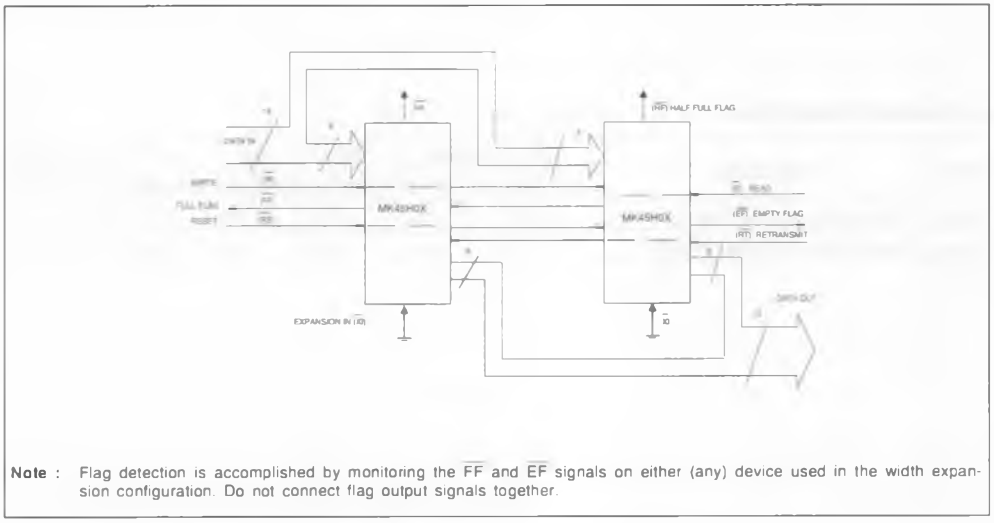


Figure 8 : MK45H0X Width Expansion FIFO Configuration.

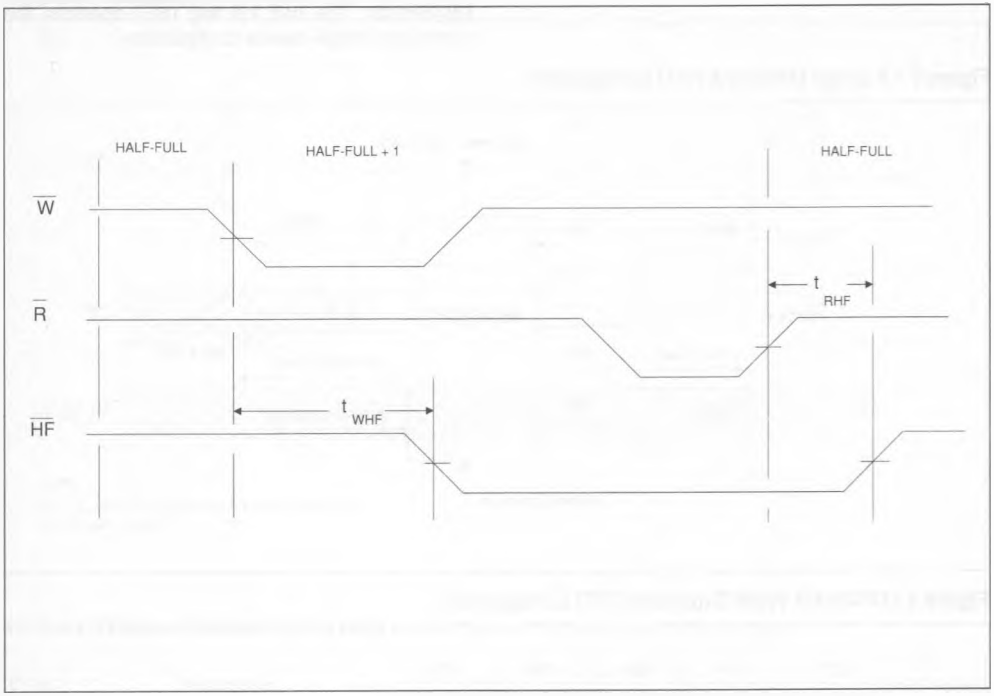


Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag (HF) is then reset by the rising edge of the read operation (see figure 9).

Figure 9 : Half Full Flag Timing.



AC CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

DEPTH EXPANSION (daisy chain)

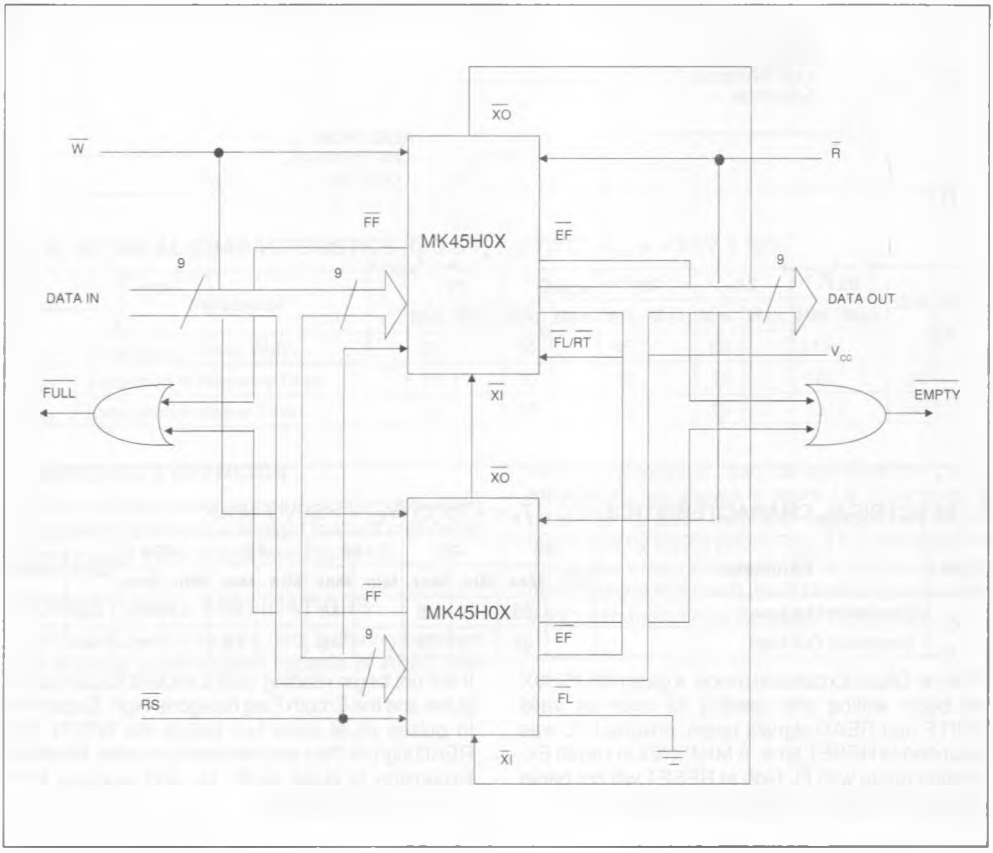
The MK45H0X can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 10 demonstrates Depth Expansion using two MK45H0Xs. Any depth can be attained by adding additional MK45H0Xs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the EFs and the ORing of all the FFs (i.e., all must be set to generate the composite FF or EF).

The MK45H0X operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

1. The first device must be designated by grounding the First Load pin (FL). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

Figure 10 : A Two Device Depth Expansion Configuration.

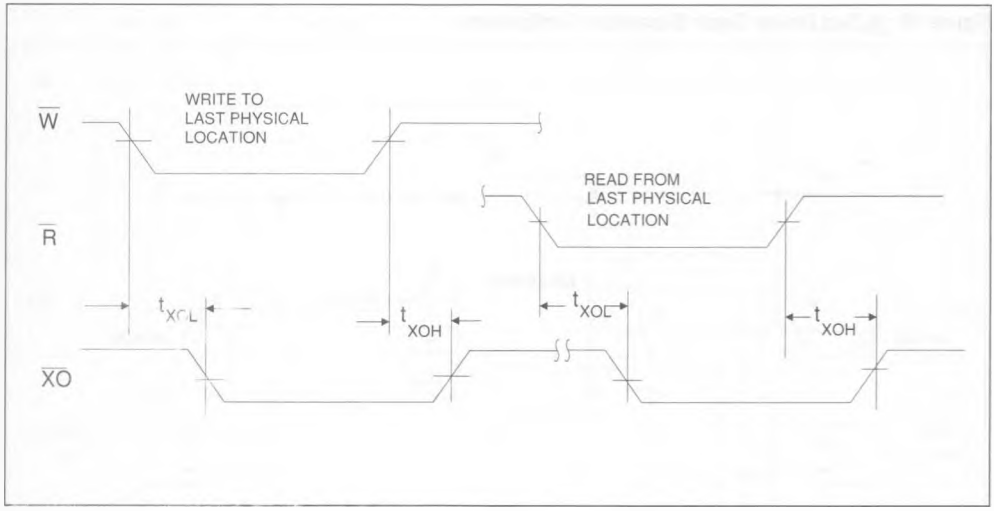


EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In asmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the XO/XI pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 11 : Expansion Out Timing.



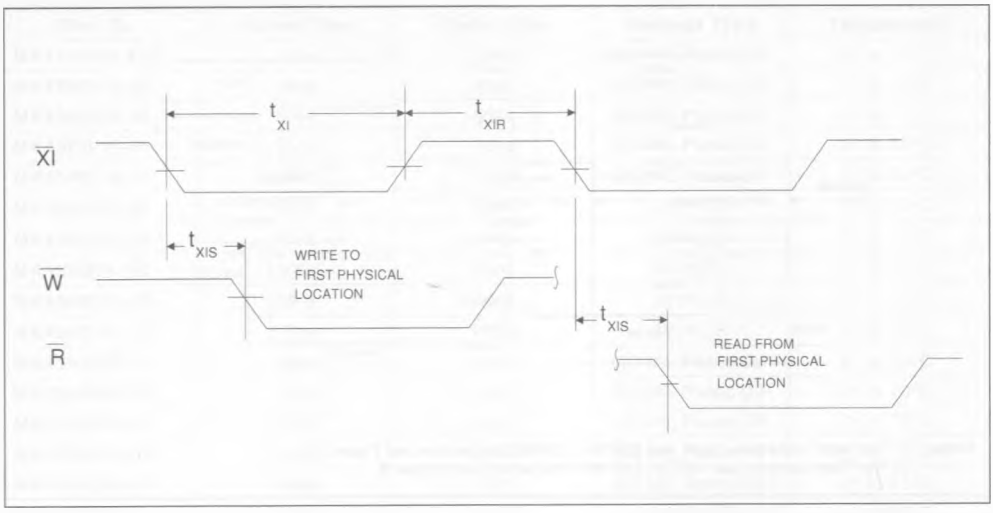
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

When in Depth Expansion mode, a given MK45H0X will begin writing and reading as soon as valid WRITE and READ signals begin, provided FL was grounded at RESET time. A MK45H0X in Depth Expansion mode with FL high at RESET will not begin writing until after an Expansion in pulse occurs.

It will not begin reading until a second Expansion In pulse and the Empth Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 12 : Expansion In Timing.



AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ + 70°C) (V_{CC} = + 5.0V ± 10%)

Sym.	Parameter	-25		-35		-50		-65		-120		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion in Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion in Setup Time	15		15		15		15		15		ns	

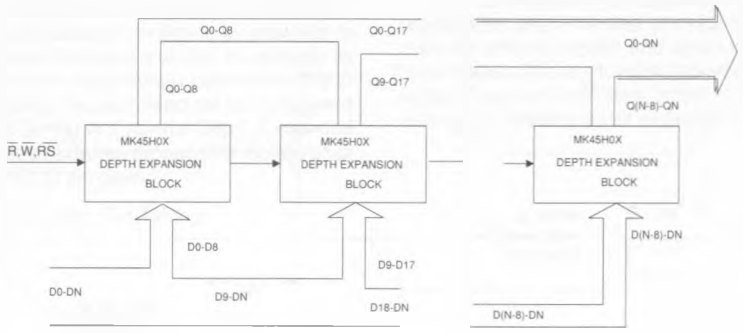
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see figure 13).

BIDIRECTIONAL APPLICATIONS

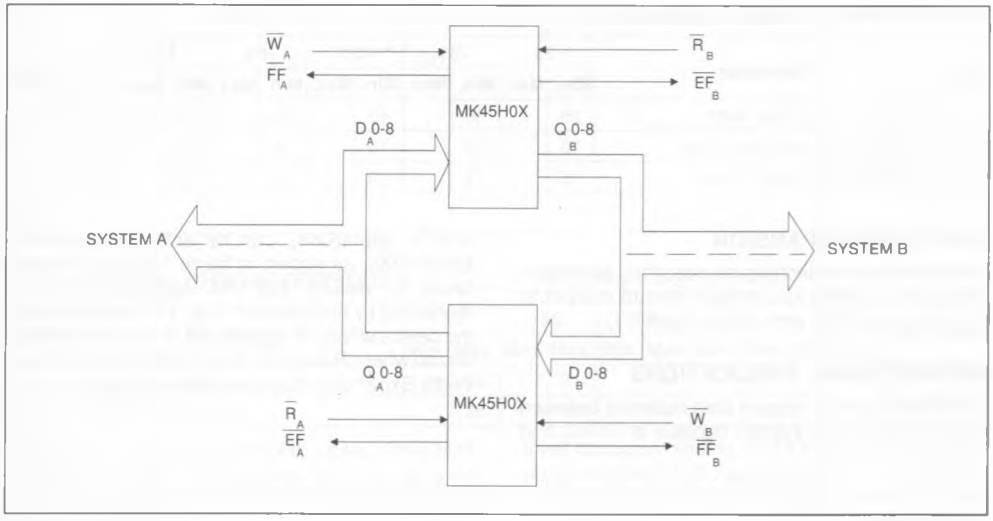
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45H0Xs, as shown in figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., FF is monitored on the device where W is used ; EF is monitored on the device where R is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 13 : Compound FIFO Expansion.



Notes : 1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

Figure 14 : Bidirectional FIFO Application.



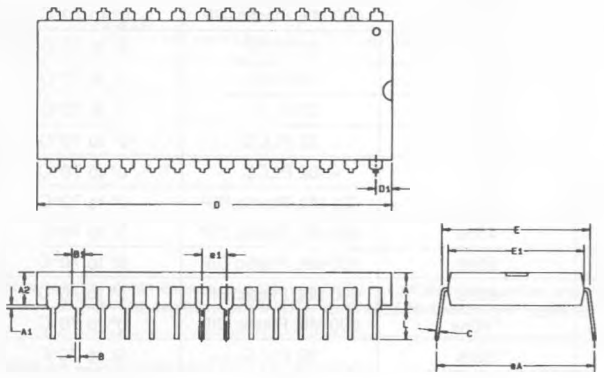
ORDER CODES

Part No	Access Time	Cycle Time	Package Type	Temperature
MK45H01N-25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H01N-12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H01K-25	25ns	35ns	32 PLCC	0° to 70°C
MK45H01K-35	35ns	45ns	32 PLCC	0° to 70°C
MK45H01K-50	50ns	65ns	32 PLCC	0° to 70°C
MK45H01K-65	65ns	80ns	32 PLCC	0° to 70°C
MK45H01K-12	120ns	140ns	32 PLCC	0° to 70°C
MK45H02N-25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H02N-12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H02K-25	25ns	35ns	32 PLCC	0° to 70°C
MK45H02K-35	35ns	45ns	32 PLCC	0° to 70°C
MK45H02K-50	50ns	65ns	32 PLCC	0° to 70°C
MK45H02K-65	65ns	80ns	32 PLCC	0° to 70°C
MK45H02K-12	120ns	140ns	32 PLCC	0° to 70°C
MK45H03N-25	25ns	35ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-35	35ns	45ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-50	50ns	65ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-65	65ns	80ns	600 MIL Plastic DIP	0° to 70°C
MK45H03N-12	120ns	140ns	600 MIL Plastic DIP	0° to 70°C
MK45H03K-25	25ns	35ns	32 PLCC	0° to 70°C
MK45H03K-35	35ns	45ns	32 PLCC	0° to 70°C
MK45H03K-50	50ns	65ns	32 PLCC	0° to 70°C
MK45H03K-65	65ns	80ns	32 PLCC	0° to 70°C
MK45H03K-12	120ns	140ns	32 PLCC	0° to 70°C
MK45H13N-25	25ns	35ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-35	35ns	45ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-50	50ns	65ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-65	65ns	80ns	300 MIL Plastic DIP	0° to 70°C
MK45H13N-12	120ns	140ns	300 MIL Plastic DIP	0° to 70°C

Part No	Access Time	R/W Cycle Time
MK45H01/2/3-25	25ns	35ns, 28.5MHz
MK45H01/2/3-35	35ns	45ns, 22.2MHz
MK45H01/2/3-50	50ns	65ns, 15.3MHz
MK45H01/2/3-65	65ns	80ns, 12.5MHz
MK45H01/2/3-12	120ns	140ns, 7.14MHz

PACKAGE DESCRIPTION

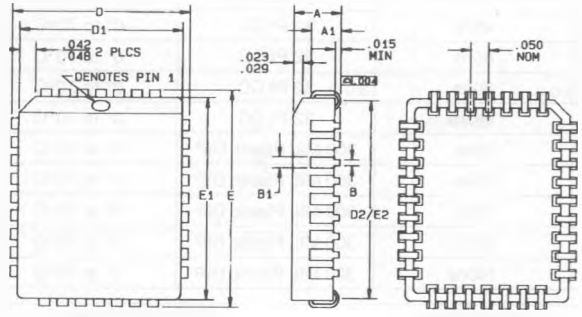
MK45H0X PLASTIC (N TYPE) DUAL–IN–LINE, 28 PINS



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		.210	2
A1	0.381		.015		2
A2	3.556	4.064	.140	.160	
B	0.381	0.534	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048		.120		

Notes : 1. Overall length includes .010 in flash on either end of the package.
2. Package standoff to be measured per jedec requirements.
3. The maximum limit shall be increased by .003 in when solder lead finish is specified.

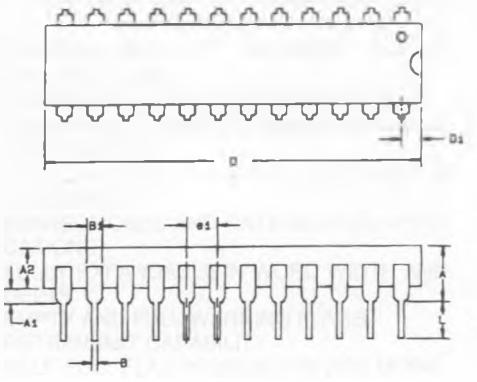
MK45H0X PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		Inches	
	Min.	Max.	Min.	Max.
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

PACKAGE DESCRIPTION

MK45H0X PLASTIC DIP (N), 28 PINS



Dim.	Inches	
	Min.	Max.
A		.210
A1	.015	
A2	.120	.140
B	.015	.021
B1	.045	.070
C	.008	.012
D		1.270
D1	.060	.090
E	.300	.325
E1	.240	.270
e1	.090	.110
eA	.300	.365
L	.125	