SGS-THOMSON MICROELECTRONICS

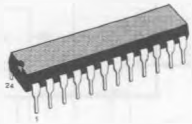
MK45264/45265(N) -55/70

(64 x 5) x 2 CMOS BIDERECTIONAL BiPORT FIFO/TRANSCEIVER

- DUAL 64 x 5 FIFOs PLUS A '245-TYPE TRANSCEIVER FUNCTION
- FULLY ASYNCHRONOUS DUAL PORT OPERATION
- EMPTY, FULL, ALMOST FULL AND ALMOST EMPTY STATUS FLAGS
- SPARE BITS FOR PARITY AND BEGINNING/END-OF-MESSAGE FLAGS
- ± 12mA OUTPUT DRIVE CAPABILITY
- DUAL V_{CC} AND V_{SS} FOR IMPROVED MARGIN AND DRIVE
- 300 MIL DIP PACKAGE
- APPLICATION : ARBITRATION-FREE µP-TO-µP MESSAGE PASSING

PIN NAMES

V_{CC}, V_{SS}	+ 5V, GND
DQ_{X0}-DQ_{X4}	X Port Data I/O
DQ_{Y0}-DQ_{Y4}	Y Port Data I/O
$\overline{W}_X$, $\overline{W}_Y$	X & Y Port Write Enables
$\overline{R}_X$/DIR	X Port Read Enable and Transceiver Direction Control
$\overline{G}$	Transceiver Enable
$\overline{R}_Y$	Y Port Read Enable
$\overline{RS}$	Master Reset
$\overline{EF}_X$, $\overline{FF}_Y$	Y-to-X FIFO Empty/full Flag
$\overline{EF}_Y$, $\overline{FF}_X$	X-to-Y FIFO Empty/full Flag
$\overline{AE}_Y$, $\overline{AF}_X$	X-to-Y FIFO Almost Empty/full
$\overline{AE}_X$, $\overline{AF}_Y$	Y-to-X FIFO Almost Empty/full



N
DIP-24
(Plastic Package)

Part No	Access Time	Cycle Time	Cycle Rate
MK45264N-55	55ns	75ns	13.3MHz
MK45265N-55	55ns	75ns	13.3MHz
MK45264N-70	70ns	95ns	10.5MHz
MK45265N-70	70ns	95ns	10.5MHz

Figure 1 : Pin Connections.

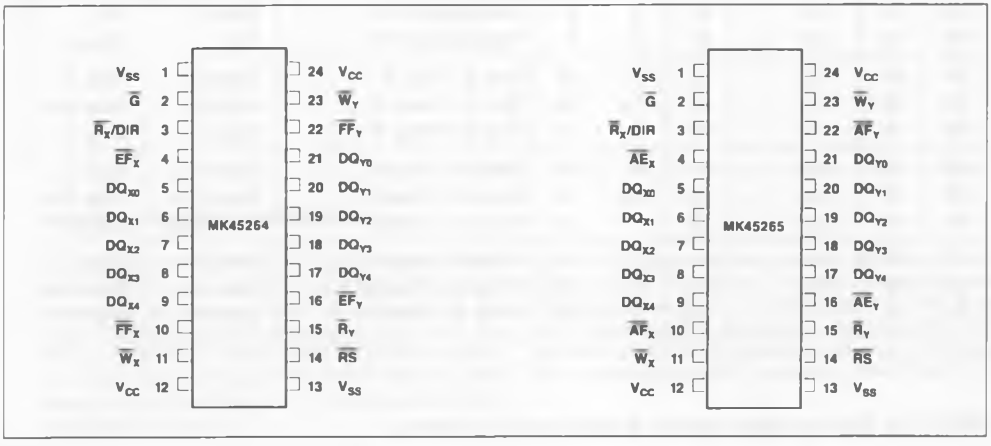
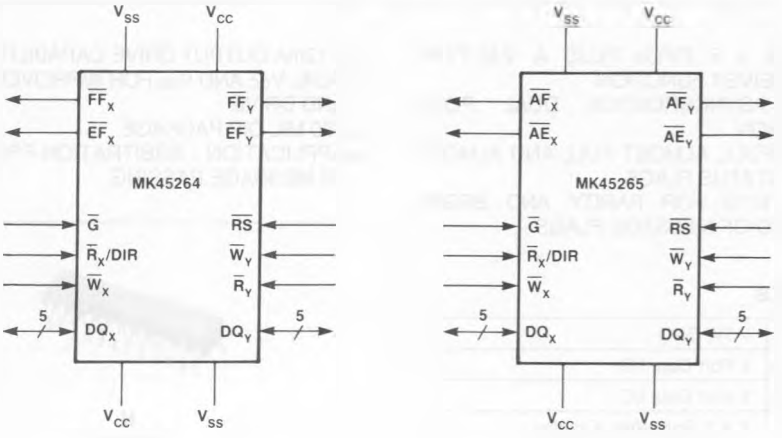


FIGURE 2. DEVICE LOGIC SYMBOL



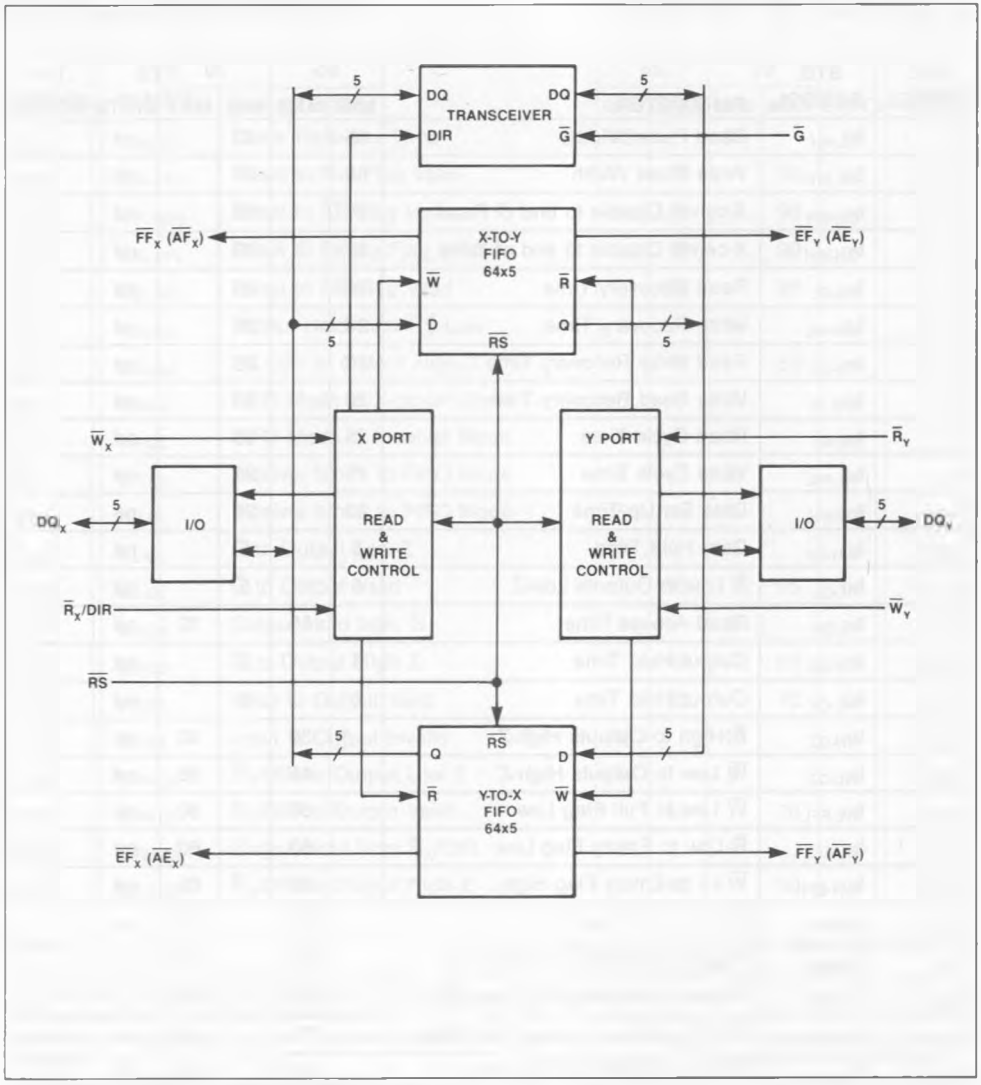
TRUTH TABLE

$\overline{RS}$	$\overline{G}$	$\overline{R}_X$/DIR	$\overline{W}_X$	$\overline{R}_Y$	$\overline{W}_Y$	MODE	DQ_X	DQ_Y
Lo	X	X	X	X	X	Master Reset	High Z	High Z
Hi	Lo	Hi	X	X	X	Transparent X-Y	Data In	DQ_X
Hi	Lo	Lo	X	X	X	Transparent Y-X	DQ_Y	Data In
Hi	Hi	Hi	Hi	Hi	Hi	Sby X / Sby Y	High Z	High Z
Hi	Hi	Hi	Hi	Lo	Hi	Sby X / Read Y	High Z	Data Out
Hi	Hi	Hi	Hi	X	Lo	Sby X / Write Y	High Z	Data In
Hi	Hi	Lo	Hi	Hi	Hi	Read X / Sby Y	Data Out	High Z
Hi	Hi	Lo	Hi	Lo	Hi	Read X / Read Y	Data Out	Data Out
Hi	Hi	Lo	Hi	X	Lo	Read X / Write Y	Data Out	Data In
Hi	Hi	X	Lo	Hi	Hi	Write X / Sby Y	Data In	High Z
Hi	Hi	X	Lo	Lo	Hi	Write X / Read Y	Data In	Data Out
Hi	Hi	X	Lo	X	Lo	Write X / Write Y	Data In	Data In

X = Don't Care

NOTE: Truth Table logic states presume all status flags to be inactive.

FIGURE 3. BLOCK DIAGRAM



DEVICE APPLICATION/FUNCTION

The MK45264/65 contains two independent single direction FIFOs, and a bidirectional transceiver, connected via two internal three state busses to I/O drive circuits. One FIFO is pointed X-to-Y, and the other pointed Y-to-X. Either port's FIFOs can be read or written asynchronous with FIFO read or write operations on the other port. The transceiver is activated with a low on $\overline{G}$.

Once the transceiver is activated, direction is controlled by the R_X/DIR pin. A high on R_X/DIR points the transceiver X-to-Y; a low points it Y-to-X. A low on $\overline{G}$ disables FIFO operations. Activating the Transceiver during FIFO operations may result in invalid or unpredictable FIFO operation.

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t_P	t_{RL-RH}	Read Pulse Width	55		70		ns	
t_P	t_{WL-WH}	Write Pulse Width	55		70		ns	
t_P	t_{GH-RH}	X-ceiver Disable to end of Read	55		70		ns	
t_P	t_{GH-WH}	X-ceiver Disable to end of Write	55		70		ns	
t_R	t_{RH-RL}	Read Recovery Time	20		25		ns	
t_R	t_{WH-WL}	Write Recovery Time	20		25		ns	
t_R	t_{RH-WL}	Read Write Recovery Time	20		25		ns	
t_R	t_{WH-RL}	Write Read Recovery Time	20		25		ns	
t_C	t_{RL-RL}	Read Cycle Time	75		95		ns	
t_C	t_{WL-WL}	Write Cycle Time	75		95		ns	
t_{DS}	t_{DV-WH}	Data Set Up Time	20		25		ns	
t_{DH}	t_{WH-DX}	Data Hold Time	5		5		ns	
t_{OL}	t_{RL-QL}	$\overline{R}$ Low to Outputs Low-Z	5		5		ns	2
t_A	t_{RL-QV}	Read Access Time		55		70	ns	3
t_{OH}	t_{RH-QX}	Output Hold Time	5		5		ns	3
t_{OH}	t_{WL-QX}	Output Hold Time	5		5		ns	3
t_{QZ}	t_{RH-QZ}	$\overline{R}$ High to Outputs High-Z		30		40	ns	2
t_{WQZ}	t_{WL-QZ}	$\overline{W}$ Low to Outputs High-Z		45		55	ns	2
t_{FL1}	t_{WL-FFL}	$\overline{W}$ Low to Full Flag Low		60		80	ns	4
t_{FL1}	t_{RL-EFL}	$\overline{R}$ Low to Empty Flag Low		60		80	ns	4
t_{FH1}	t_{WH-EFH}	$\overline{W}$ Hi to Empty Flag High		50		65	ns	4
t_{FH1}	t_{RH-FFH}	$\overline{R}$ Hi to Full Flag High		50		65	ns	4
t_{FL2}	t_{WL-AFL}	$\overline{W}$ Low to Almost Full Flag Low		60		80	ns	5
t_{FL2}	t_{RL-AEL}	$\overline{R}$ Low to Almost Empty Flag Low		60		80	ns	5
t_{FH2}	t_{WH-AEH}	$\overline{W}$ Hi to Almost Empty Flag High		75		95	ns	5
t_{FH2}	t_{RH-AFH}	$\overline{R}$ Hi to Almost Full Flag High		75		95	ns	5
t_I	t_{WL-FFH}	Write Protect Indeterminate		25		30	ns	6
t_I	t_{RL-EFH}	Read Protect Indeterminate		25		30	ns	7
t_{FR}	t_{FFH-WL}	Full Flag Recovery	0		0		ns	6
t_{FR}	t_{EFH-RL}	Empty Flag Recovery	0		0		ns	7
t_{RS}	$t_{RSL-RSH}$	Reset Pulse Width	55		70		ns	

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t_{RSR}	t_{RSH-WH}	Reset Recovery Time	75		95		ns	
t_{RFV}	$t_{RSL-FFH}$	Reset to Full Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL-AFH}$	Reset to $\overline{AF}$ Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL-EFL}$	Reset to Empty Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL-AEL}$	Reset to $\overline{AE}$ Flag Valid		70		90	ns	3
t_{RQX}	t_{RSL-QX}	Outout Hold from $\overline{RS}$ Low	0		0		ns	3
t_{RQZ}	t_{RSL-QZ}	RS Low to Output High Z		40		50	ns	2
t_{FG}	t_{WH-GL}	FIFO Mode to X-ceiver Mode	0		0		ns	
t_{FG}	t_{RH-GL}	FIFO Mode to X-ceiver Mode	0		0		ns	
t_{GF}	t_{GH-WL}	X-ceiver Mode to FIFO Mode	5		5		ns	
t_{GF}	t_{GH-RL}	X-ceiver Mode to FIFO Mode	5		5		ns	
t_{GQL}	t_{GL-QL}	$\overline{G}$ to Output Low Z	0		0		ns	2
t_{GQV}	t_{GL-QV}	$\overline{G}$ to Output Valid		75		95	ns	3
t_{GQX}	t_{GH-QX}	Output Hold from $\overline{G}$	0		0		ns	3
t_{GQZ}	t_{GH-QZ}	$\overline{G}$ to Output High Z		40		50	ns	2
t_{DVQV}	t_{DV-QV}	Input to Output Valid		55		70	ns	3
t_{DXQX}	t_{DX-QX}	Input to Output Invalid	10		10		ns	3
t_{DQL}	$t_{DIRV-QL}$	$\overline{R}_X$/DIR to Output Low Z	0		0		ns	2
t_{DQV}	$t_{DIRV-QV}$	$\overline{R}_X$/DIR to Output Valid		55		70	ns	3
t_{DQX}	$t_{DIRV-QX}$	Output Hold from $\overline{R}_X$/DIR	0		0		ns	3
t_{DQZ}	$t_{DIRV-QZ}$	$\overline{R}_X$/DIR to Output High Z		40		50	ns	2

NOTES

1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/5pf Output Load. See Equivalent Load Circuit B.
3. Measured w/30pf Output Load. See Equivalent Load Circuit A.
4. Applies to $\overline{EF}_X$, $\overline{FF}_X$, $\overline{FF}_Y$, $\overline{EF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
5. Applies to $\overline{AE}_X$, $\overline{AF}_X$, $\overline{AE}_Y$, $\overline{AF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
6. Writes beginning a) more than t_I (max) before $\overline{FF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{FF}$ goes high may be performed. c) t_{FR} (min) after $\overline{FF}$ goes high will be performed.
7. Reads beginning a) more than t_I (max) before $\overline{EF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{EF}$ goes high may be performed. c) t_{FR} (min) after $\overline{EF}$ goes high will be performed.

Read/Write

The FIFOs utilize separate Read and Write enable inputs to control port activity and direction. A low on a Read Enable reads a port's receive FIFO. A high on a Read Enable or a low on a Write Enable disables a port's data outputs to a high impedance state. A low on a Write Enable initiates a write to a port's transmit FIFO, regardless of the state of Read Enable. Input data is latched into the FIFO on the rising edge of a Write Enable.

Full/Empty Flags

An active Full Flag indicates that a port's transmit FIFO is full and will accept no more data. Writes done to a FIFO while full are blocked. Once a read has occurred on a full FIFO, clearing a location in the FIFO, the Full Flag will go inactive, allowing another write to begin on the next falling edge of Write Enable.

An active Empty Flag indicates a port's receive FIFO is empty and can send no more data. Any reads done on a FIFO while empty are blocked. Once a write to an empty FIFO has occurred, the Empty Flag will go inactive, allowing another read to begin on the next falling edge of Read Enable.

Almost Flags

An inactive Almost Full flag indicates a port's transmit FIFO has room for at least four (4) more bytes, which is to say the flag will go active during the fourth write from full and stay active until after the fourth location from full has been vacated (read). An inactive Almost Empty flag indicates a port's receive FIFO has at least four (4) bytes of data in memory, ready to be read, which is to say that the flag will go active while reading the fourth remaining byte and remain active until after the fourth byte has been stored (written).

Reset

Reset is initiated by a low on the Master Reset ($\overline{RS}$) input. A reset returns all data outputs to a high impedance state, taking precedence over the read strobes ($\overline{R}_X$/DIR and $\overline{R}_Y$) and $\overline{G}$. The states of the FIFO control inputs ($\overline{R}_X$/DIR, $\overline{W}_X$, $\overline{R}_Y$ and $\overline{W}_Y$) are a Don't Care throughout reset. The read strobes are a Don't Care at the end of reset because the Empty Flag becomes active (goes low) during reset, blocking any attempted reads. The write strobes ($\overline{W}_X$ and $\overline{W}_Y$) may fall any time during or after reset, but must not go high until t_{RSR} after $\overline{RS}$ goes high.

FIGURE 4. WRITE TIMING

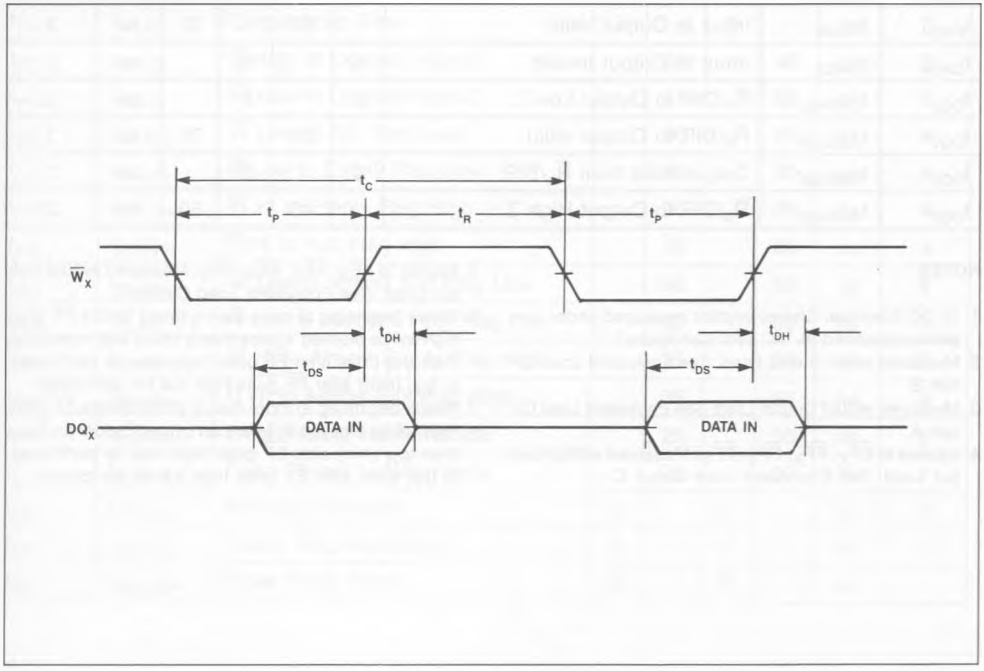


FIGURE 5. READ TIMING

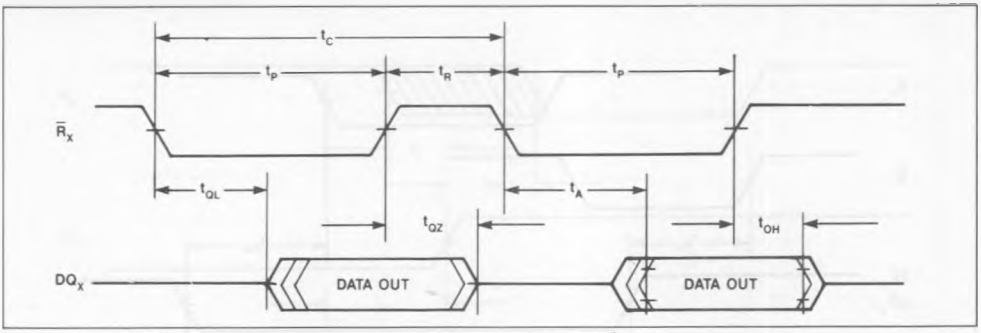


FIGURE 6. WRITE/READ TIMING

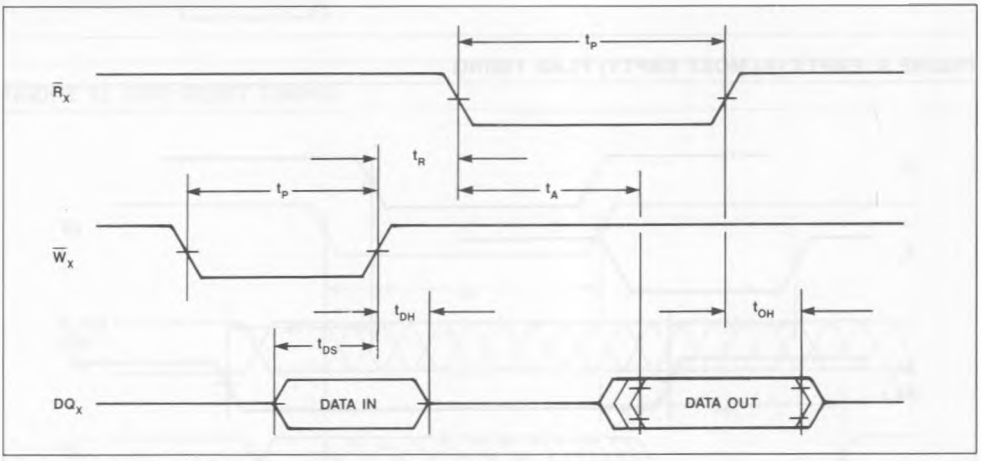


FIGURE 7. READ/WRITE TIMING

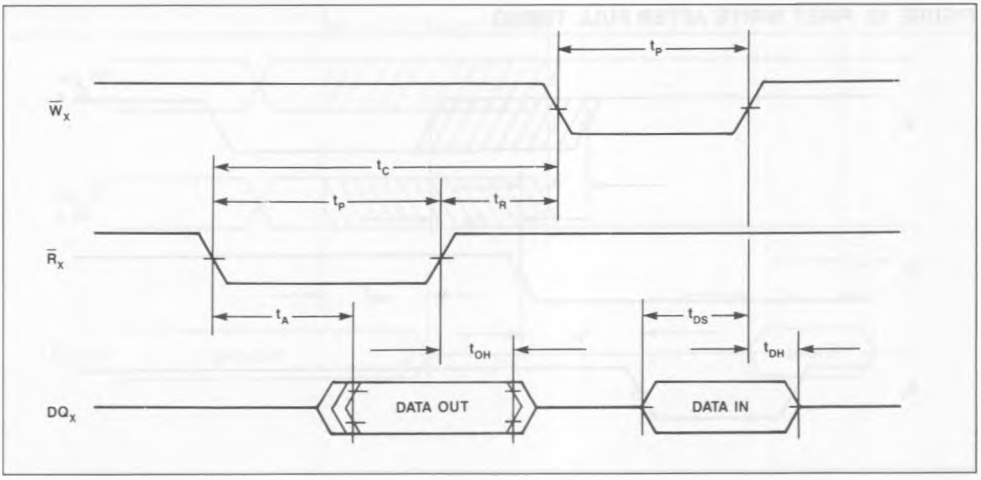


FIGURE 8. FULL (ALMOST FULL) FLAG TIMING

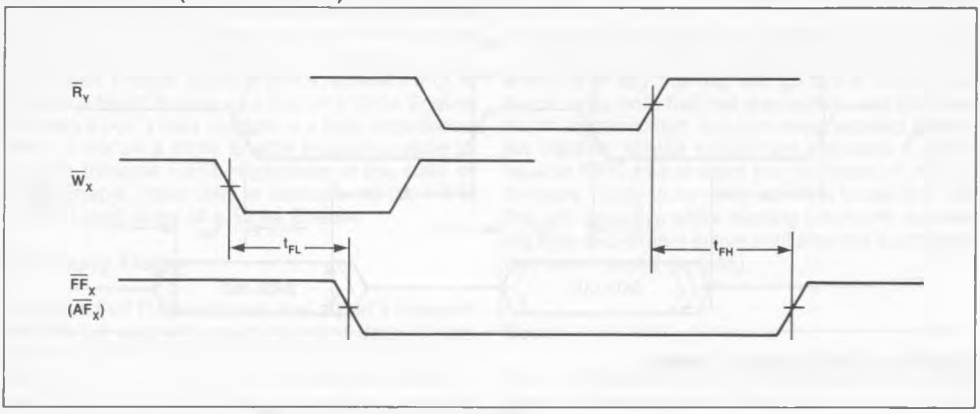


FIGURE 9. EMPTY (ALMOST EMPTY) FLAG TIMING

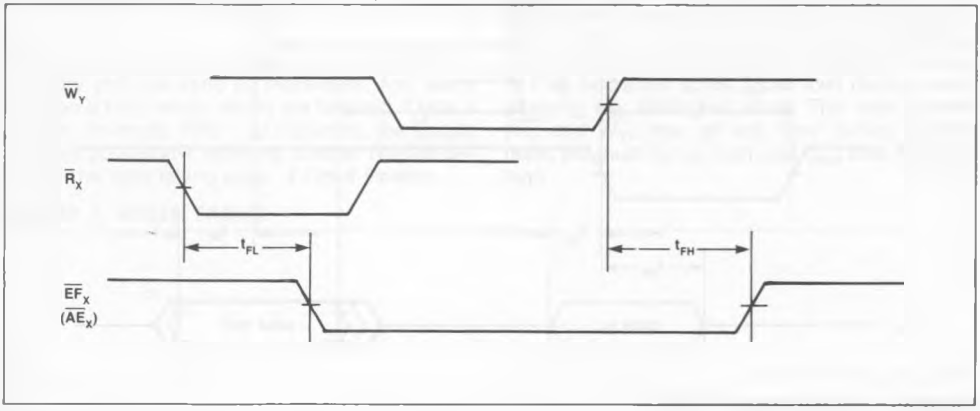


FIGURE 10. FIRST WRITE AFTER FULL TIMING

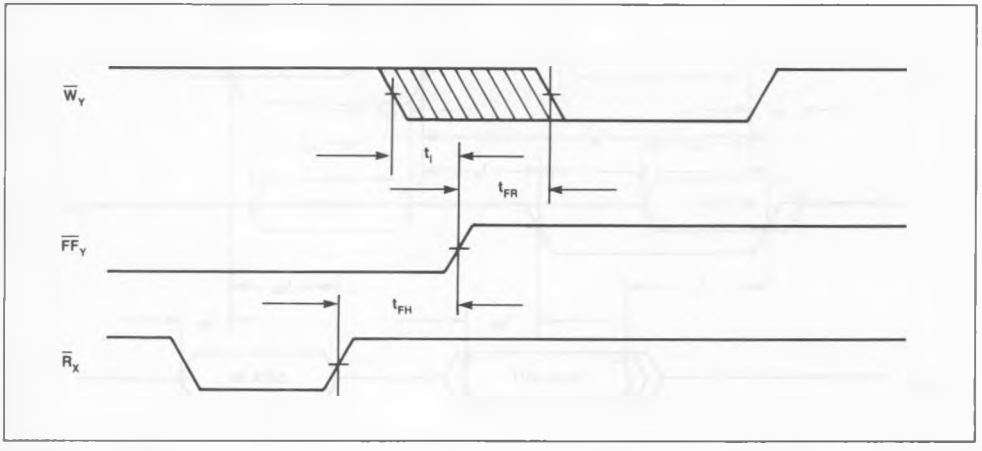


FIGURE 11. FIRST READ AFTER EMPTY TIMING

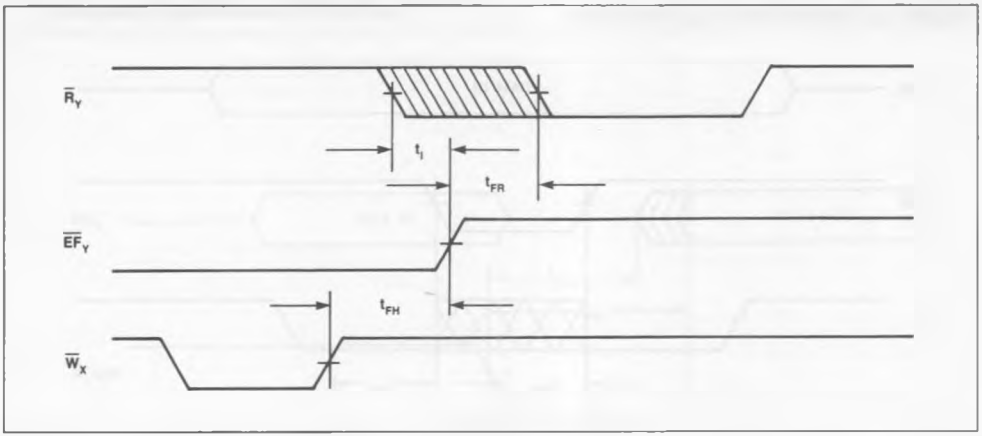


FIGURE 12. FIFO RESET TIMING

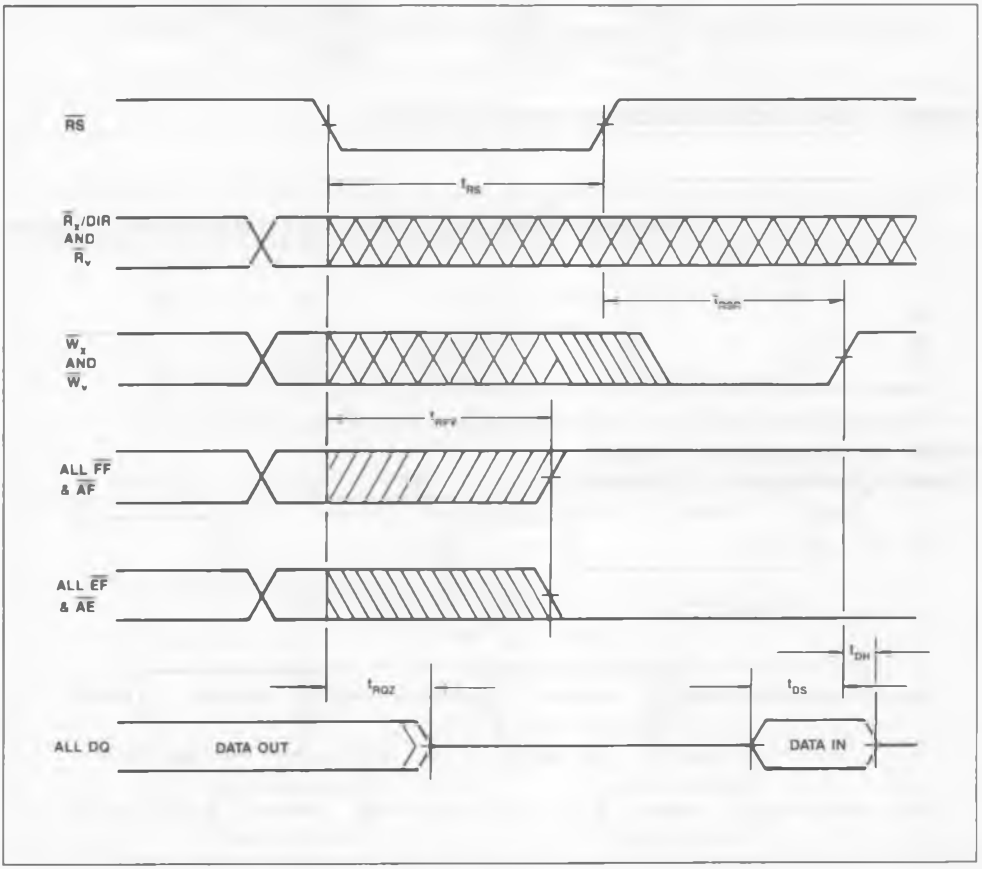


FIGURE 13. TRANSCEIVER RESET TIMING (EXAMPLE SHOWN WITH $\overline{R}_X$/DIR HIGH)

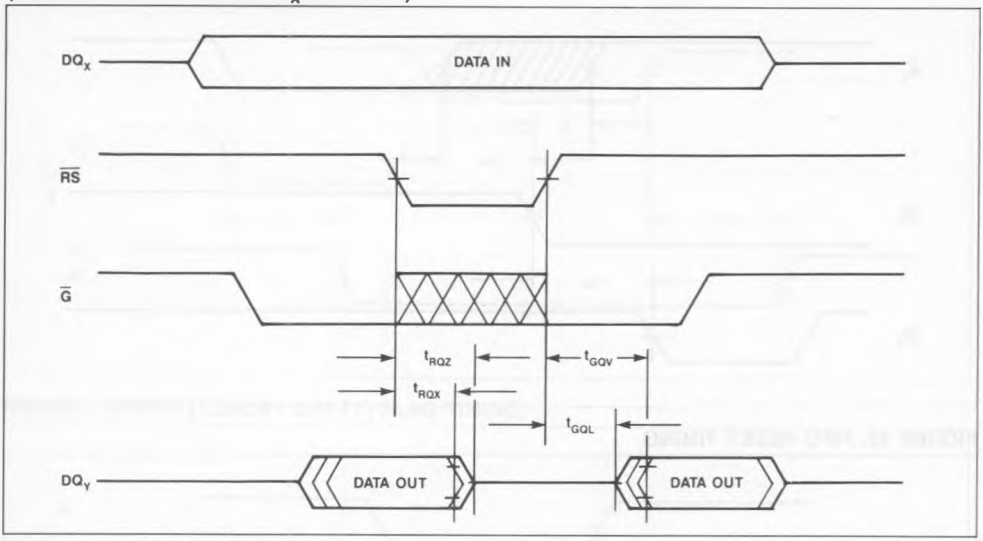


FIGURE 14. FIFO MODE/TRANSCEIVER MODE TRANSITION

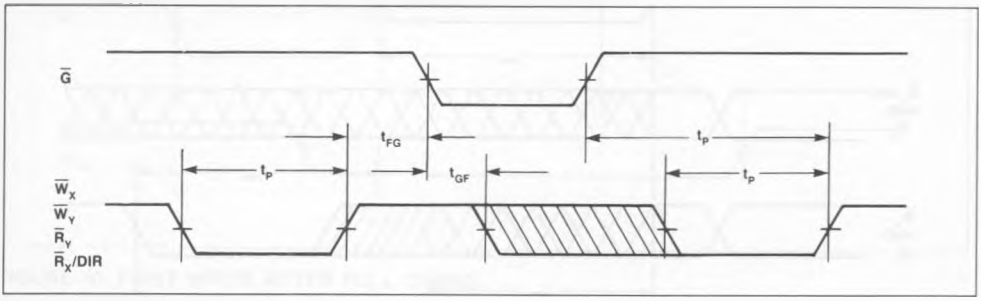


FIGURE 15. TRANSCEIVER $\overline{G}$ TIMING (EXAMPLE SHOWN WITH $\overline{R}_X$/DIR HIGH)

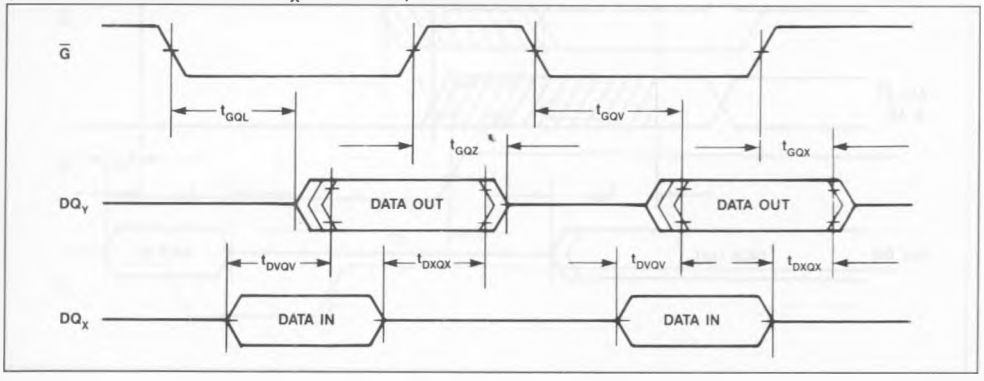


FIGURE 16. TRANSCEIVER $\overline{R}_X$/DIR TIMING
(EXAMPLE SHOWN WITH $\overline{G}$ LOW)

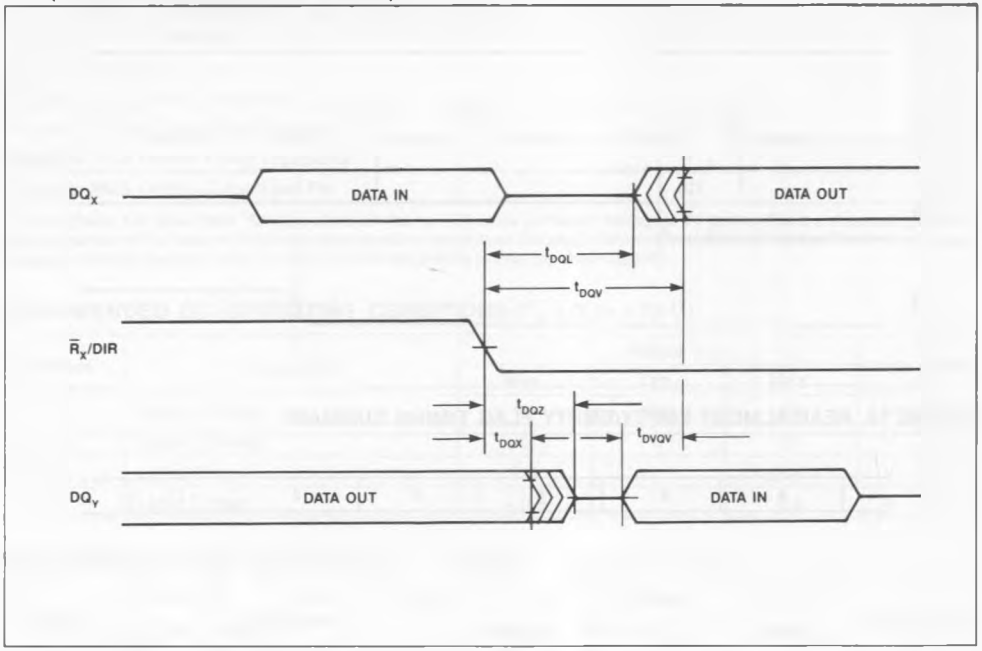


FIGURE 17. WRITE/ALMOST FULL/FULL FLAG TIMING SUMMARY

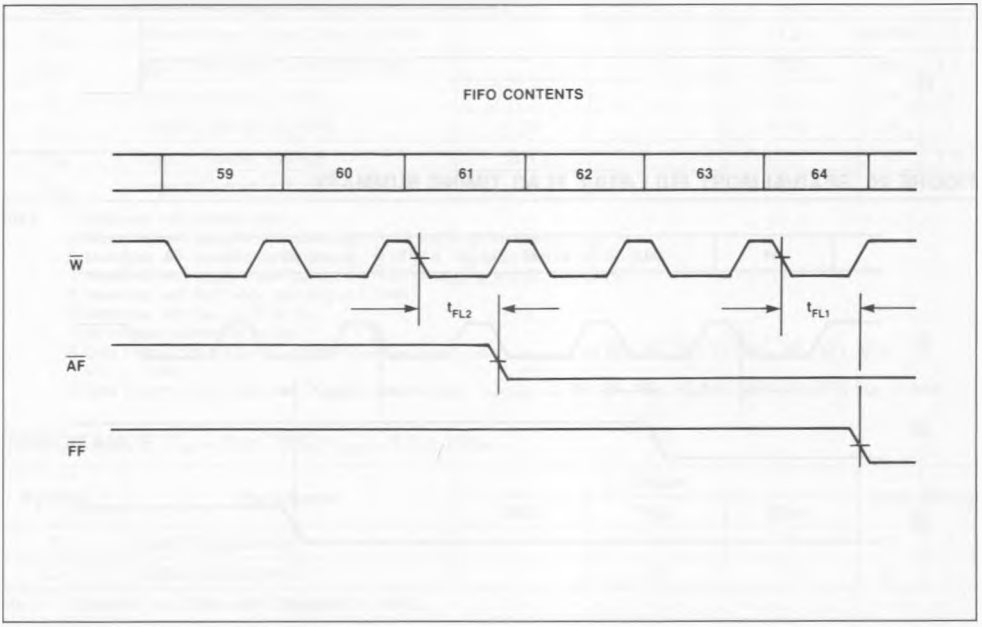


FIGURE 18. WRITE/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

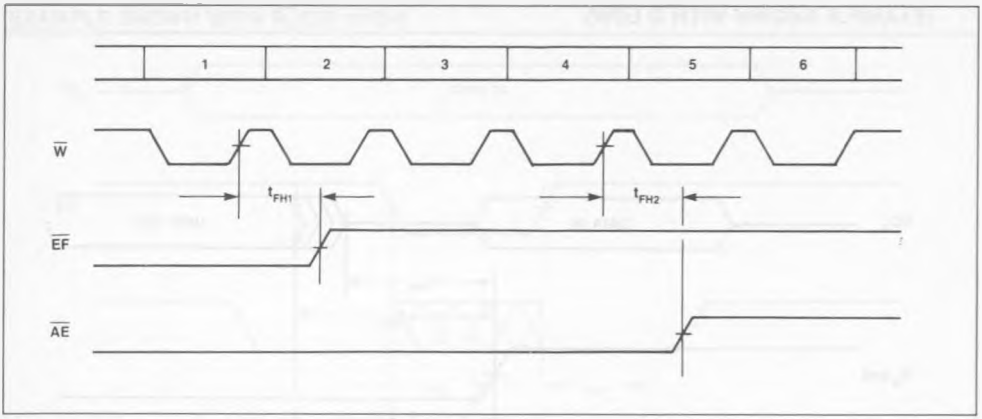


FIGURE 19. READ/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

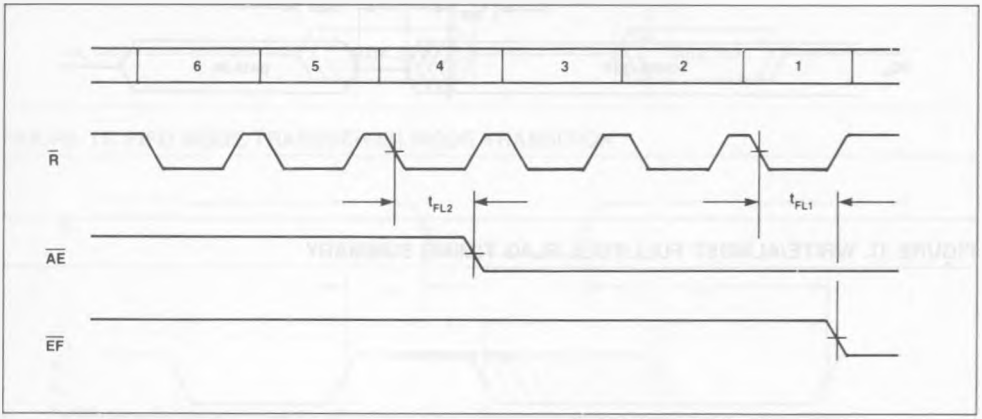
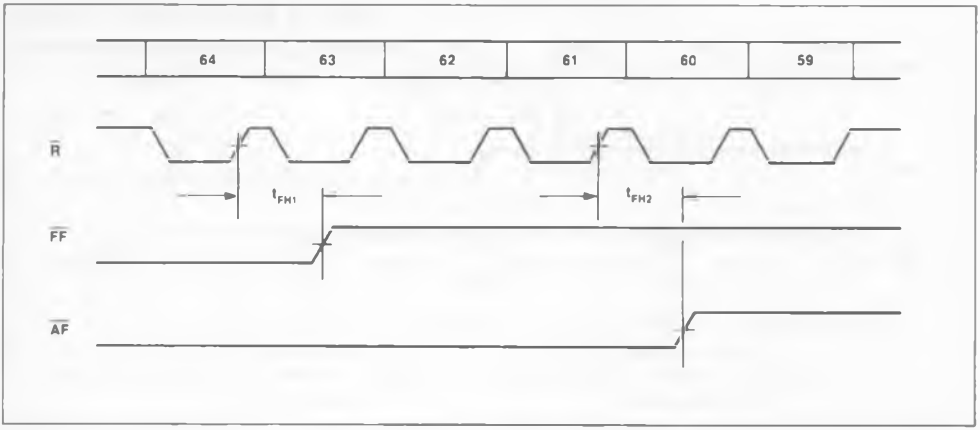


FIGURE 20. READ/ALMOST FULL/FULL FLAG TIMING SUMMARY



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to V_{SS}	– 1.5 to + 7.0	V
Ambient Operating Temperature (T_A)	0 to + 70	°C
Ambient Temperature under Bias	– 55 to + 125	°C
Ambient Storage Temperature (plastic)	– 55 to + 125	°C
Allowable Total Device Power Dissipation	1	W
Allowable RMS Output Current per Pin	80	mA

* Stresses greater than those listed "Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0° to + 70°C)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC} + 0.3	V	1
V_{IL}	Logic 0 Input	– 0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CCQ}	Quiescent Power Supply Current, per Port			25	mA	1,2
I_{CCA}	Active Power Supply Current, per Port			40	mA	1,3
I_{CCD}	Dynamic Power Supply Current, per Port			1.2	mA/MHz	1,4
I_{CCT}	Total Power Supply Current, both Ports			100	mA	1,5
I_{IL}	Input Leakage Current	– 1		+ 1	µA	6
I_{OL}	Output Leakage Current	– 10		+ 10	µA	7
V_{OH}	Logic 1 Output Voltage	2.4			V	7,8
V_{OL}	Logic 0 Output Voltage			0.4	V	7,9

Notes :
1. Measured with outputs open.
2. Measured with opposite port quiescent ; $\overline{R}$, $\overline{W}$ and $\overline{G}$ ≥ V_{IH} (Min).
3. Measured with opposite port quiescent ; $\overline{R}$ or $\overline{W}$ ≤ V_{IL} (Max) and $\overline{G}$ ≥ V_{IH} (Min).
4. Measured with opposite port quiescent ; $\overline{R}$ or $\overline{W}$ toggling and G ≥ V_{IH} (Min).
5. Measured with both ports operating at t_C (min.).
6. Measured with V_{IN} = 0.0V to V_{CC}.
7. All voltages referenced to V_{SS}.
8. Data Output Pins (DQ_{X0}-DQ_{X4} and DQ_{Y0}-DQ_{Y4}) I_{OUT} = – 12mA ; Flag Output Pins $\overline{EF_X}$ $\overline{EF_Y}$ $\overline{FF_X}$ $\overline{FF_Y}$ $\overline{AE_X}$ $\overline{AE_Y}$ $\overline{AF_X}$ $\overline{AF_Y}$) I_{OUT} = –1mA.
9. Data Outputs (DQ_{X0}-DQ_{X4} and DQ_{Y0}-DQ_{Y4}) I_{OUT} = 12mA ; Flag Output Pins $\overline{EF_X}$, $\overline{EF_Y}$, $\overline{FF_X}$ $\overline{FF_Y}$, $\overline{AE_X}$ $\overline{AE_Y}$ $\overline{AF_X}$ $\overline{AF_Y}$) I_{OUT} = 4mA.

CAPACITANCE (T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_I	Input Capacitance		4	5	pF	1
C_O	Output Capacitance		8	10	pF	1

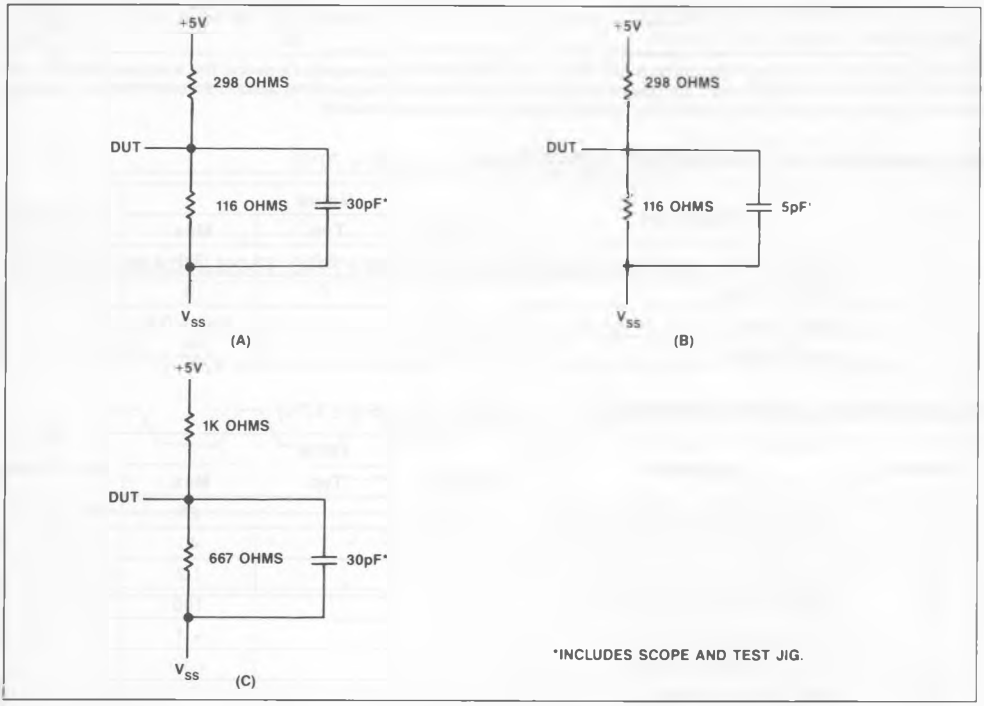
Note : 1. Sampled, not 100% tested. Measured at 1 MKz.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0° to 70°C

V_{CC} = 5.0 Volts ± 10%

FIGURE 21. EQUIVALENT OUTPUT LOAD CIRCUIT



APPLICATION ISSUES

Width Expansion

The MK45264/65 is designed to be used in sets of two or more, as shown below. The MK45264/65 is supplied in two configurations, MK45264 and MK45265; the MK45264 having Empty and Full Flags, the MK45265 having Almost Empty and Almost Full Flags. This scheme allows a pair of devices to be connected in such a way as to assure that the PAIR present a full complement of status flags in BOTH directions, that is, both to the left and to the right.

The resulting 10 bit wide configuration allows both parity AND beginning or end of message flag bits to be carried along with an 8 bit byte of data. The 20 bit wide configuration allows carrying 2 bits of parity AND separate message start and stop bits in 16 bit applications.

The MK45264/65 was designed as a 5 bit wide device in order to allow the use of a 300 mil DIP package; allowing the MK45264/65 to: a) achieve the highest function/board space ratio possible for a fully featured bidirectional BiPORT FIFO, b) provide higher performance with improved noise margins than would be possible in higher pin count packages, and c) provide greater flexibility to users of various bus widths.

FIGURE 22. (64x10)x2 WIDTH EXPANSION

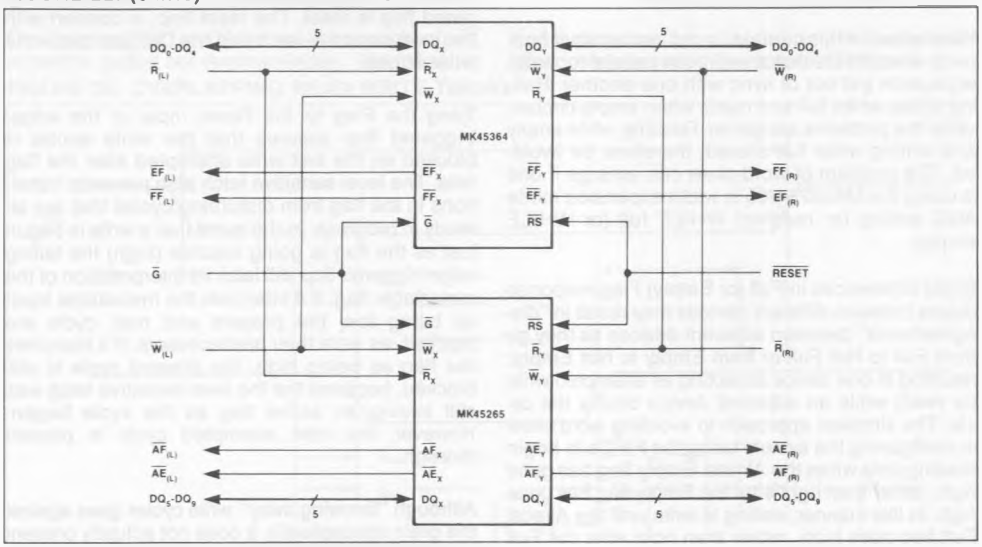
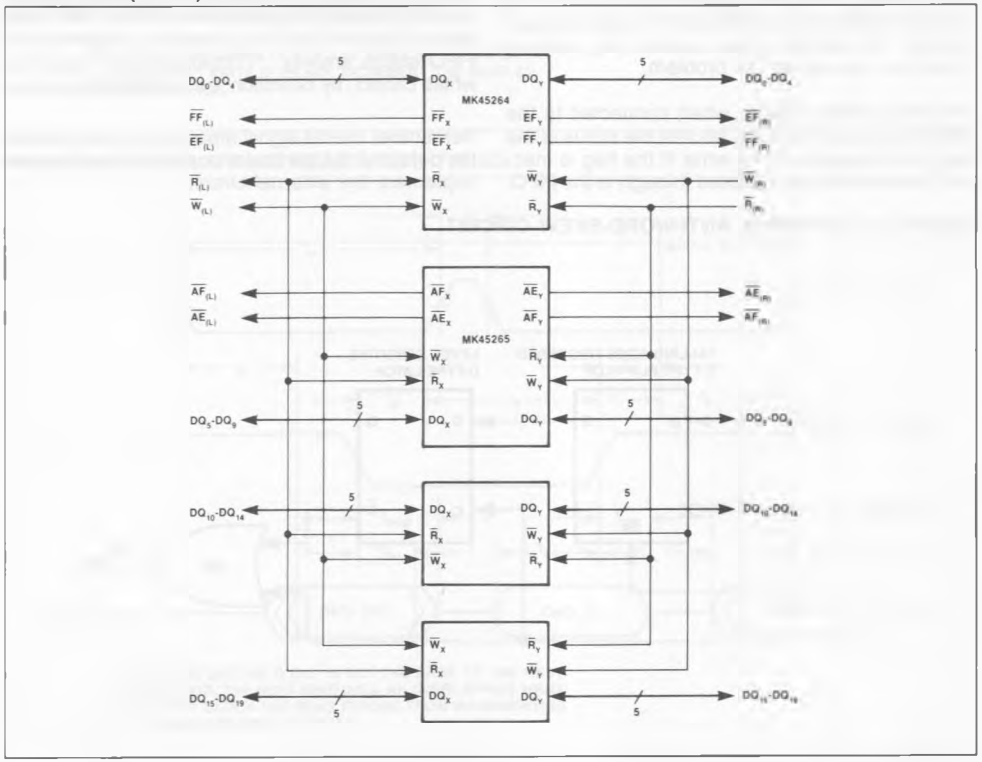


FIGURE 23. (64x20)x2 WIDTH EXPANSION



Width Expansion and Word-Skew

Word-skew, in this context, is defined as what happens when FIFOs that are wired in parallel for width expansion get out of sync with one another. Halting writes when full and reads when empty circumvents the problems altogether. Reading while empty and writing while full should, therefore, be avoided. The problem of word-skew can emerge if one is using the MK45264/65 in width expansion mode AND writing (or reading) WHILE full (or WHILE empty).

Slight differences in Full (or Empty) Flag response delays between different devices may result in "disagreements" between adjacent devices as they go from Full to Not Full or from Empty to Not Empty; resulting in one device accepting an attempted write (or read) while an adjacent device blocks the cycle. The simplest approach to avoiding word skew is configuring the system using the FIFOs to begin reading only when the Almost Empty flag has gone high, rather than right after the Empty flag has gone high. In like manner, waiting to write until the Almost Full flag goes high, rather than right after the Full flag goes high will prevent the problem, which is why the Almost flags are provided. However, should such a scheme prove unworkable in a particular appication, the addition of an external flag latching circuit can also solve the problem.

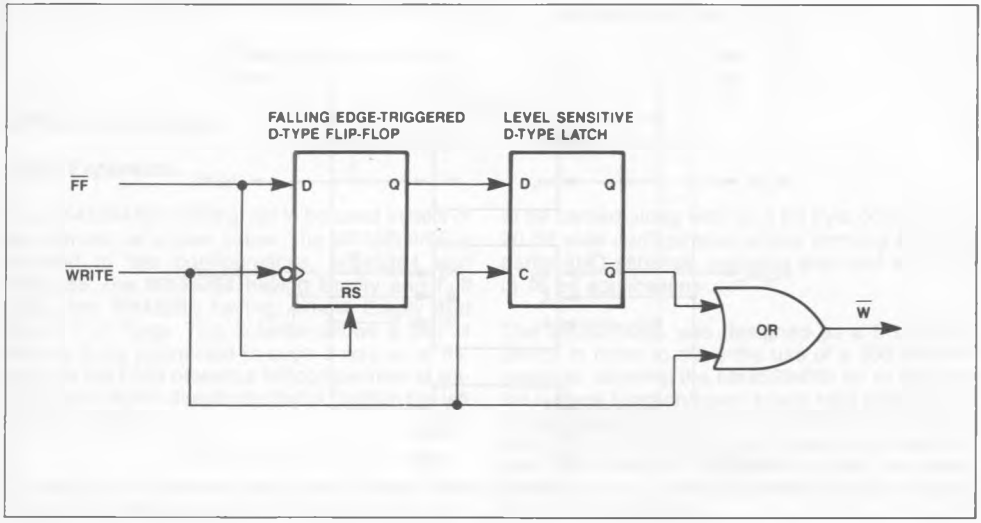
The circuit shown below, when connected to the Write strobe and Full Flag, latches the status of the flag at the beginning of a write. If the flag is inactive, the Write strobe is passed through to the FIFO. When the flag goes active (low) the falling-edge triggered flop is reset. The reset flop, in concert with the level-sensitive latch and the OR gate block the write strobe.

Tying the Flag to the Reset input of the edge-triggered flop assures that the Write strobe is blocked on the first write attempted after the flag falls. The level sensitive latch also prevents transitions in the flag from disturbing cycles that are already in progress. In the event that a write is begun just as the flag is going inactive (high) the falling edge-triggered flop will latch its interpretation of the metastable flag. If it interprets the metastable input as being low, the present and next cycle are blocked, as were their predecessors. If it interprets the flag as being high, the present cycle is still blocked, because the the level sensitive latch was still seeing an active flag as the cycle began. However, the next attempted cycle is passed through.

Although "throwing away" write cycles goes against the grain conceptually, it does not actually present a problem in this situation. It must be assumed that Writing while Full or Reading while Empty would only be allowed in applications where the write and/or read strobes are proceeding regardless of FIFO status anyway. "Throwing away" reads or writes cannot, by definition, be considered an error.

Remember, overall signal timing must comprehend the delays of the particular components chosen to implement the external circuit.

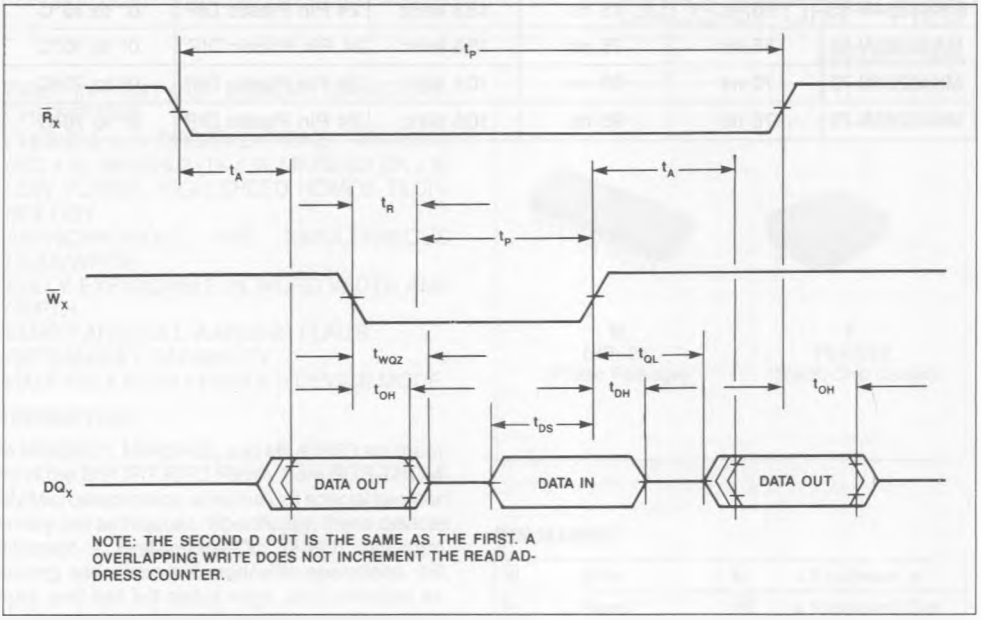
FIGURE 24. EXTERNAL ANTI-WORD-SKEW CIRCUIT



Overlapping Read and Write Strobes

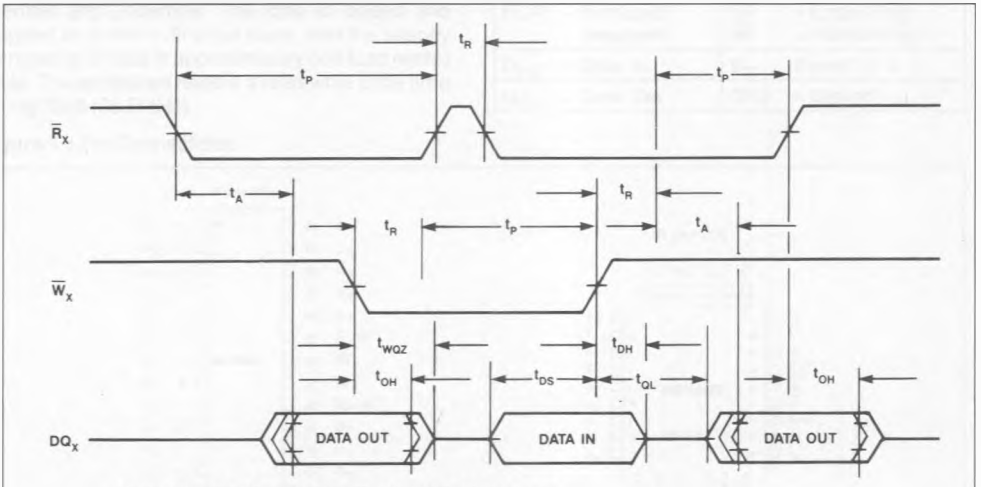
Overlapping Read and Write strobes on a given port is neither tested nor recommended. The following timing diagrams are provided only to illustrate the relationship between the control functions.

FIGURE 25. OVERLAPPING READ/WRITE TIMING



NOTE: THE SECOND D OUT IS THE SAME AS THE FIRST. A OVERLAPPING WRITE DOES NOT INCREMENT THE READ ADDRESS COUNTER.

FIGURE 26. OVERLAPPING READ/WRITE TIMING



NOTE: THE SECOND D OUT IS NOT THE SAME AS THE FIRST. IT IS, IN FACT, THE NEXT READ DATA. AN OVERLAPPING WRITE DOES NOT BLOCK THE READ STROBE FROM INCREMENTING THE READ ADDRESS COUNTER.

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK45264N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45264N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C