MOSTEK

4096 x1-BIT STATIC RAM

MK4104(J/N/E) Series

FEATURES

- ☐ Combination static storage cells and dynamic control circuitry for truly high performance

PART NUMBER	ACCESS TIME	CYCLE TIME
MK4104-3/-33	200ns	310ns
MK4104-4/-34	250ns	385ns
MK4104-5/-35	300ns	460ns
MK4104-6	350ns	535ns

- ☐ Low Active Power Dissipation: 150mW (Max)
- ☐ Battery backup mode (3V/10mW on -33, -34 and -35)
- ☐ Standby Power Dissipation less than 28 mW (at V_{CC} = 5.5V)
- ☐ Single +5V Power Supply (± 10% tolerance)
- ☐ Fully TTL Compatible
  Fanout: 2 – Standard TTL
  2 – Schottky TTL
  12 – Low Power Schottky TTL
- ☐ Standard 18-pin DIP
- ☐ MKB version screened to MIL-STD-883

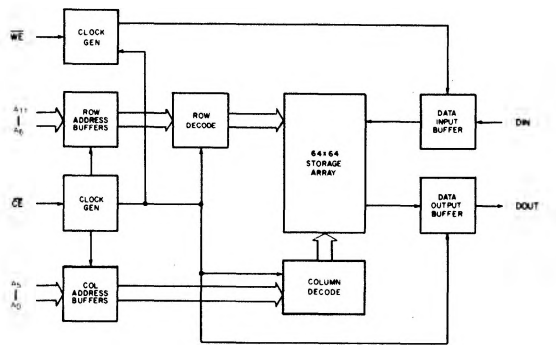
DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

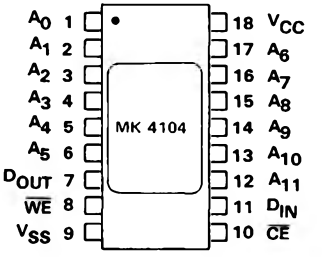
All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL compatible with a one level of 2.2 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 200mV of noise margin when driven by standard TTL and a minimum of 500mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{11}	Address Inputs	V_{SS}	Ground
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −1.0V to +7.0V
Operating Temperature T_A (Ambient) ..... 0° C to + 70° C
Storage Temperature (Ambient) (Ceramic) ..... −65° C to +150° C
Storage Temperature (Ambient) (Plastic) ..... −55° C to +125° C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0° C ≤ T_A ≤ + 70° C)

	PARAMETER	MK4104 Series			UNITS	NOTES
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	-1.0		.8	Volts	1

DC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		5	mA	3
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	4
I_{OL}	Output Leakage Current	−10	10	μA	3, 5
V_{OH}	Output Logic "1" Voltage I_{OUT}=−500μA	2.4		Volts	
V_{OL}	Output Logic "0" Voltage I_{OUT}= 5mA		0.4	Volts	

AC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = + 5.0 volts ± 10%)

	PARAMETER	TYP	MAX	NOTES
C_I	Input Capacitance	4pF	6pF	14
C_O	Output Capacitance	6pF	7pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by:
   I_{CC1} [ma] = $(5t_p + 15(t_C - t_p) + 4720) \div t_C$
   where t_p and t_C are expressed in nanoseconds. Equation is referenced to the -3 device, other devices derate to the same curve. Data outputs open.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at 0 ≤ V_{IN} ≤ 5.5 volts. (V_{CC} = 5V)
5. 0V ≤ V_{OUT} ≤ + 5.5V. (V_{CC} = 5V)
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
8. If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.
9. Determined by user. Total cycle time cannot exceed t_{CE} max.
10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.
11. AC measurements assume t_T = 5ns. Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
12. $t_C = t_{CE} + t_p + 2t_T$.
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with Δ V equal to 3V and V_{CC} nominal.
15. $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3t_T + t_{MOD}$

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6,11]

($0°C \leq T_A \leq +70°C$) (V_{CC} = + 5.0 volts ± 10%)[1]

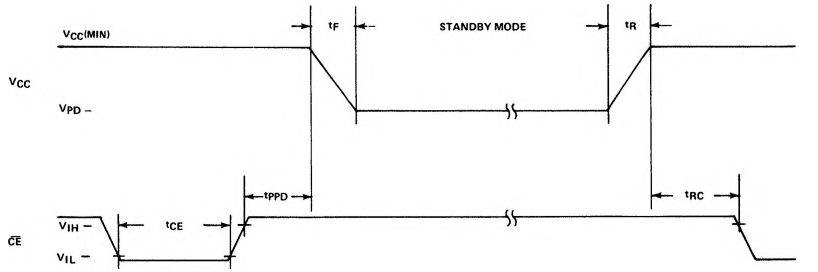
SYMBOL	PARAMETER	MK4104-3/33		MK4104-4/34		MK4104-5/35		MK4104-6		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time	310		385		460		535		ns	12
t_{AC}	Random Access		200		250		300		350		7
t_{CE}	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	350	10,000		
t_P	Chip Enable Precharge Time	100		125		150		175			
t_{AH}	Address Hold Time	110		135		165		190			
t_{AS}	Address Set-Up Time	0		0		0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	65	0	75	0	100		13
t_{RS}	Read Command Set-Up Time	0		0		0		0			8
t_{WS}	Write Enable Set-Up Time	-20		-20		-20		-20			8
t_{DHC}	Data Input Hold Time Referenced to $\overline{CE}$	170		210		250		285			
t_{DHW}	Data Input Hold Time Referenced to $\overline{WE}$	70		90		105		125			
t_{WW}	Write Enabled Pulse Width	60		75		90		105			
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	0	10,000		9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	70		85		105		120			
t_{DS}	Data Input Set-Up Time	0		0		0		0			10
t_{WH}	Write Enable Hold Time	150		185		225		260			
t_T	Transition Time	5	50	5	50	5	50	5	50		
t_{RMW}	Read-Modify-Write Cycle Time	385		475		570		660			16

STANDBY CHARACTERISTICS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MK4104-33		MK4104-34		MK4104-35		UNITS	
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{PD}	V_{CC} In Standby	3.0		3.0		3.0		Volts	
I_{PD}	Standby Current		3.3		3.3		3.3	mA	
t_F	Power Supply Fall Time	100		100		100		µsec	
t_R	Power Supply Rise Time	100		100		100		µsec	
t_{CE}	Chip Enable Pulse Width	200		250		300		µsec	
t_{PPD}	Chip Enable Precharge To Power Down Time	100		125		150		nsec	
V_{IH}	Min CE High "I" Level	2.2		2.2		2.2		Volts	
t_{RC}	Standby Recovery Time	500		500		500		µsec	

POWER DOWN WAVEFORM



DESCRIPTION (Cont'd)

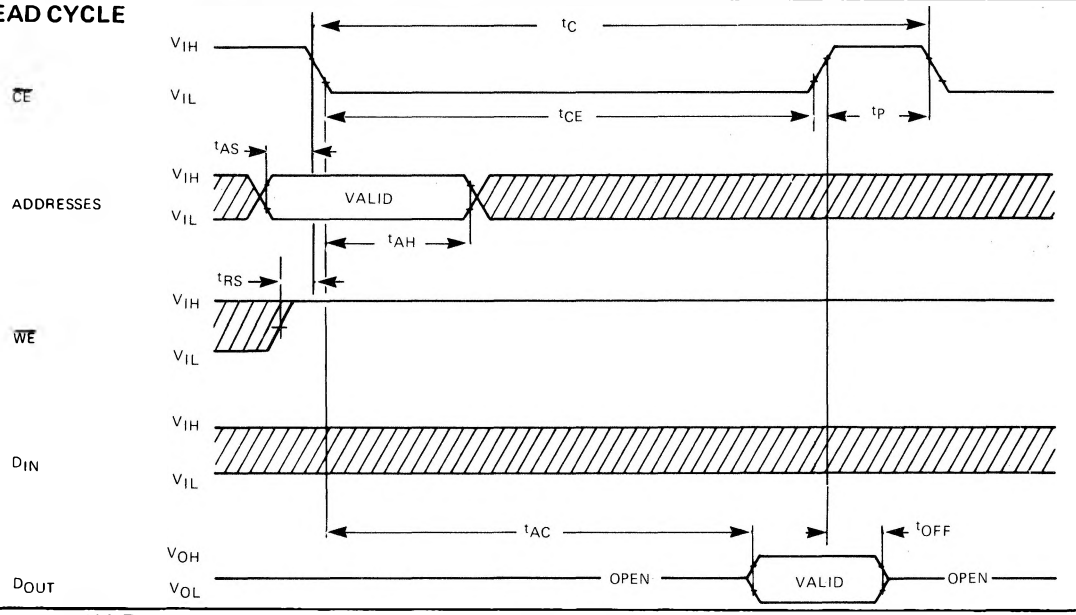
to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirements of +5V ± 10% tolerance combined with TTL compatability on all I/0 pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/0 makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's MK3880 (Z80). The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/0 operation, needed for Z80 interfacing, without external circuitry.

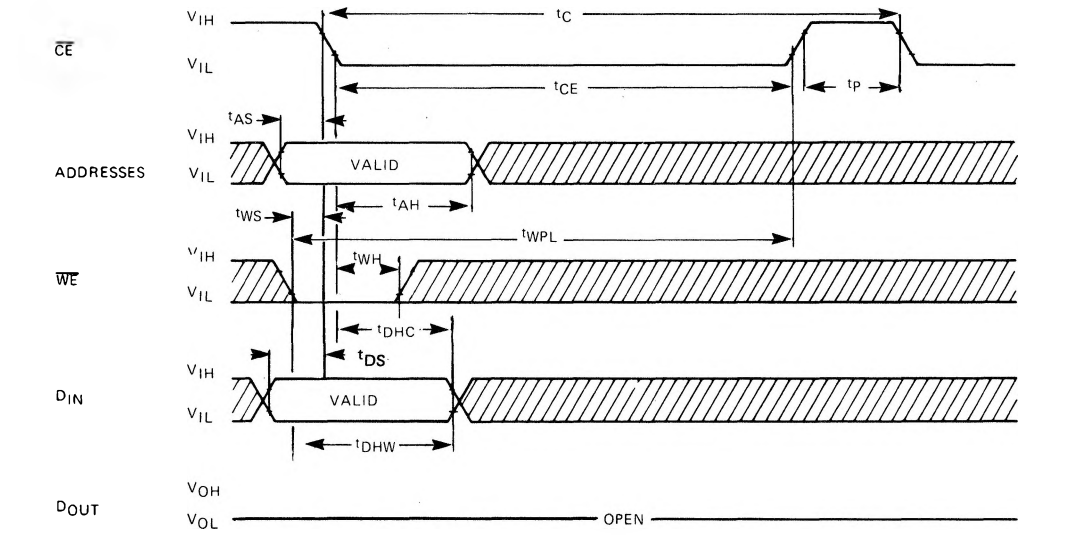
The MK4104-3X series has the added capability of retaining data in a reduced power mode. V_{CC} maybe lowered to 3V with a guaranteed power dissipation of only 10mW maximum. This makes the MK4104 ideal for those applications requiring data retention at the lowest possible power as in battery operation.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only at 8°C at 1.86 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

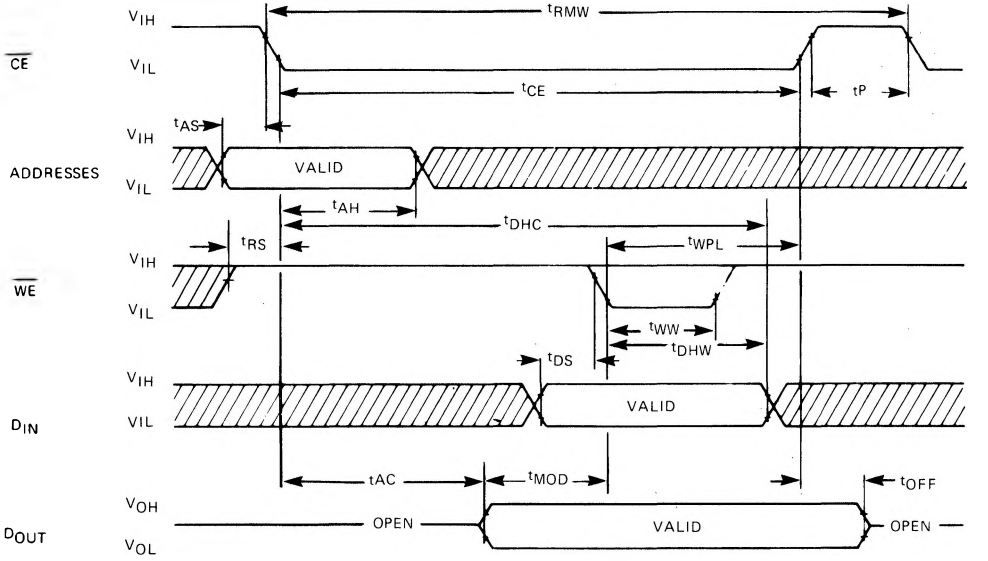
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATION

READ CYCLE

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ($\overline{CE}$) clock. A read cycle is accomplished by holding the 'write enable' ($\overline{WE}$) input at a high level (V_{IH}) while clocking the $\overline{CE}$ input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of $\overline{CE}$ and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when $\overline{CE}$ goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of $\overline{CE}$ or $\overline{WE}$. If the negative transition of $\overline{WE}$ occurs prior to the leading edge of $\overline{CE}$ as in an "early" write cycle then the $\overline{CE}$ input serves as the strobe for data-in. If $\overline{CE}$ leading edge occurs prior to the leading edge of $\overline{WE}$ as in a read-modify-write cycle then data-in is strobed by the $\overline{WE}$ input. Due to the internal timing generator, two independent timing parameters must be satisfied for DI hold time, these are, t_{DHW} and t_{DHC}. For a R/W or RMW cycle t_{DHC} is automatically satisfied making t_{DHW} the more restrictive parameter. For a write only cycle either parameter can be more restrictive depending on the position of $\overline{WE}$ relative to $\overline{CE}$. In any event both parameters must be satisfied.

In an early' write cycle the output will remain in an open or high impedance state. In a read-modify write operation the output will go active through the modify and write period until $\overline{CE}$ goes to precharge. If the cycle is such that $\overline{WE}$ goes active after $\overline{CE}$ but before valid data appears on the output (prior to t_{AC}) then the output may not remain open. However, if data-in is valid on the leading edge of $\overline{WE}$, and $\overline{WE}$ occurs prior to the positive transition of $\overline{CE}$ by the minimum lead time t_{WPL}, then valid data will be written into the selected cell. The Data in hold time parameters t_{DHW} and t_{DHC} must be satisfied.

READ-MODIFY-WRITE CYCLE

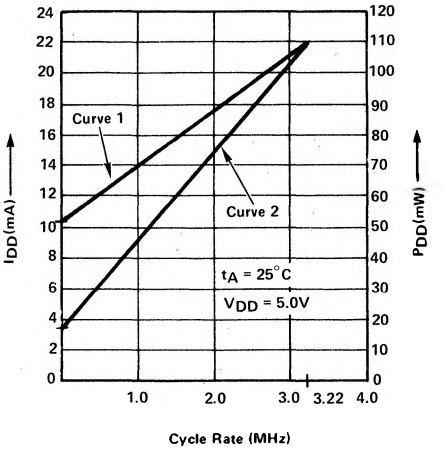
The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between $\overline{WE}$ active (low) and the rising edge of $\overline{CE}$ (t_{WPL}). Data out will remain valid until the rising edge of $\overline{CE}$. A minimum RMW cycle time can be approximated by the following equation (t_{RMW} = RMW cycle time and t_P = $\overline{CE}$ precharge time).

$$t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3t_T$$

POWER DOWN MODE

In power down data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leq$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

OPERATING POWER VS CYCLE TIME



Characterization data plot of frequency vs power dissipation for a typical MK4104 device.

Curve 1 - Clock on time (low level) is bottom scale minus 100 NSEC

Curve 2 - Clock off time (high level) is bottom scale minus 200 NSEC