PRELIMINARY

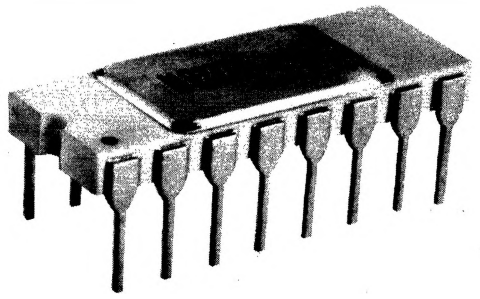
MK 4102P-6

1024x1 BIT STATIC
MOS Random Access Memory

MOSTEK

FEATURES:

- ☐ Direct TTL compatibility – all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time: 275 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required



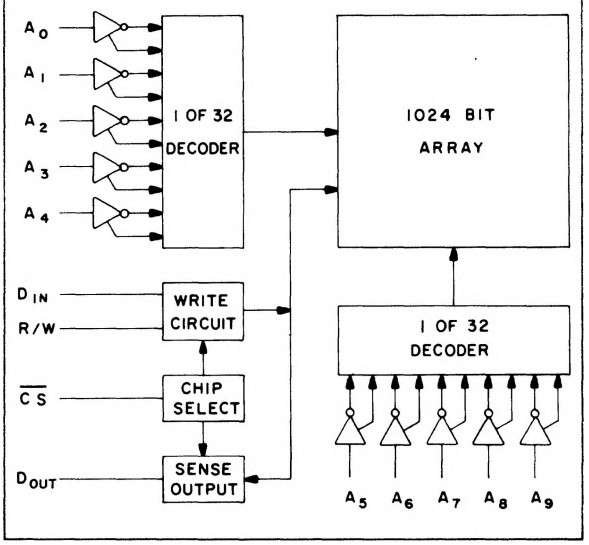
DESCRIPTION:

The MOSTEK MK 4102-6 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

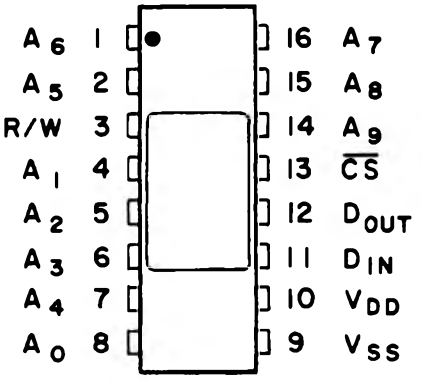
All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select (CS) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK 4102-6 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102-6 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... −0.5V to 7V

Operating Temperature (Ambient) ..... 0°C to 70°C

Storage Temperature (Ambient) ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle	275		nsec	
t_{WC}	Write Cycle	275		nsec	
t_{WP}	Write Pulse Width	200		nsec	
t_{AW}	Address to Write Pulse Delay	0		nsec	
t_{DS}	Data Set-Up Time	175		nsec	
t_{DH}	Data Hold Time	50		nsec	
t_{CW}	Chip Select Pulse Width	175		nsec	
t_{WA}	Write Pulse To Address Delay	50	50	nsec	Write Cycle
t_{ACR}	Address to Chip Select Delay		125	nsec	Read Cycle
t_{OH}	Output Hold Time	50		nsec	Chip Must Remain Selected
t_{ACW}	Address to Chip Select Delay		50	nsec	Write Cycle

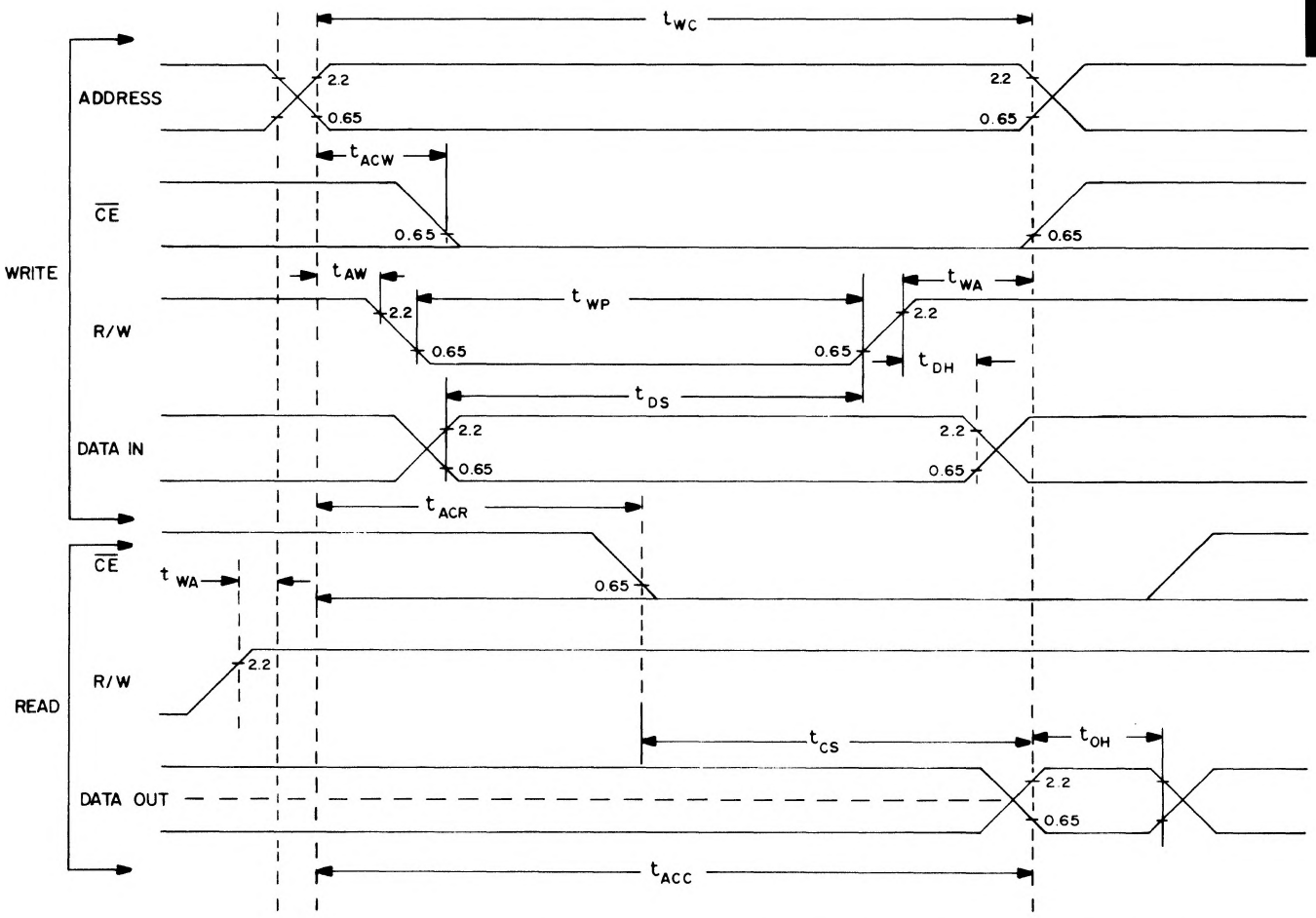
DC ELECTRICAL CHARACTERISTICS (V_{DD}= +5V ± 5%, V_{SS} = 0V, $0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD}	Supply Current		80	mA	output open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 0V to 5.25 V
I_{LO}	Output Leakage Current		10	µA	V_O = 0.4V to 5.25V
V_{OH}	Output Voltage, Logic 1	2.2		volts	I_{OH}= -100 µA
V_{OL}	Output Voltage, Logic 0		.40	volts	I_{OL} = +3.2 mA

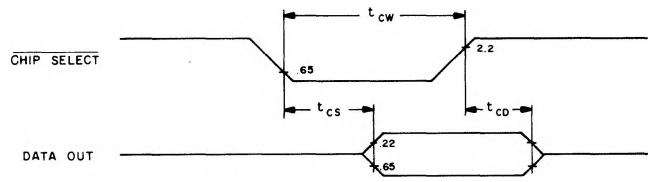
AC ELECTRICAL CHARACTERISTICS (V_{DD}= +5V ± 5%, V_{SS} = 0V, 0°C < T_A < 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Access Time		275	nsec	
t_{CS}	Chip Select Time		150	nsec	Address stable for T_{ARC}
t_{CD}	Chip Deselect Time		100	nsec	
C_I	Input Capacitance (Any Input)		5	pF	f = 1MHz V_I = 0V@25°C
C_O	Output Capacitance		10	pF	f = 1MHz V_I =0V@25°C

TIMING



CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to $\overline{\text{Chip Select}}$.

PACKAGE (16-lead ceramic dual-in-line hermetic package)