PRELIMINARY

MOSTEK®

MICROCOMPUTER COMPONENTS

CMOS MICROCOMPUTER CLOCK/RAM

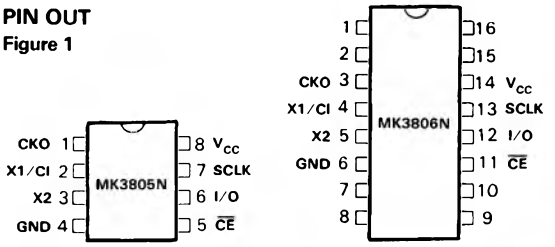
MK3805N/MK3806N

FEATURES

- Real-time clock counts seconds, minutes, hours, date of the month, day of the week, month, and year. Every 4th year, February has 29 days.
- Serial I/O for minimum pin count (8 pins)
- 24 x 8 RAM for scratchpad data storage
- Simple Microcomputer interface
- High speed shift clock independent of crystal oscillator frequency
- Single byte or multiple byte (Burst Mode) data transfer capability for read or write of clock or RAM data.
- TTL Compatible (V_{CC} = 5V)
- Low-power CMOS
- $I_{CC} \leq 2mA$ (V_{CC} = 5 V)
- $+3V \leq V_{CC} \leq 9.5V$

PIN OUT

Figure 1



PIN DESCRIPTION

Table 1

PIN 3805N	PIN 3806N	NAME	DESCRIPTION
1	3	CKO	Buffered Sytem Clock Output
2	4	X1/C1	Crystal or External Clock Input
3	5	X2	Crystal Input
4	6	GND	Power Supply Pin
5	11	$\overline{CE}$	Chip Enable for Serial I/O Transfer
6	12	I/O	Data Input/Output Pin
7	13	SCLK	Shift Clock for Serial I/O Transfer
8	14	V_{CC}	Power Supply Pin

GENERAL DESCRIPTION

Many microprocessor applications require a real-time clock and/or memory that can be battery powered with very low power drain. The MK3805N/MK3806N are specifically designed for these applications. The device contains a real-time clock/calendar, 24 bytes of static RAM, an on-chip oscillator, and it communicates with the microprocessor via a simple serial interface. The MK3805N/MK3806N are fabricated using CMOS technology, thus insuring very low power consumption.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information to the microprocessor. The end of the month date is automatically adjusted for months with less than 31 days, including correction for leap year every 4 years. The clock operates in either the 24 hour or 12 hour format with an AM/PM indicator.

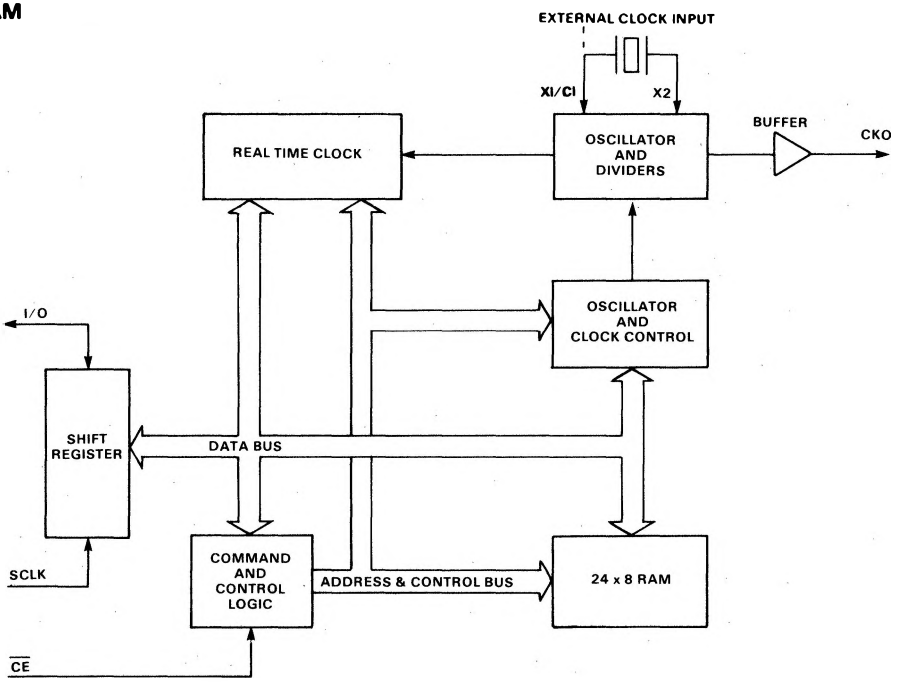
The on-chip oscillator provides a real-time clock source for the clock/calendar. It incorporates a programmable divider so that a wide variety of crystal frequencies can be accommodated. The oscillator also has an output available that can be connected to the microprocessor clock input. A separately programmable divider provides several different output frequencies for any given crystal frequency. This feature can eliminate having to use a separate crystal or external oscillator for the microprocessor, thereby reducing system cost.

Interfacing the CLOCK/RAM with a microprocessor is greatly simplified using synchronous serial communication. Only 3 lines are required to communicate with the CLOCK/RAM: (1) $\overline{CE}$ (chip enable), (2) I/O (data line) and (3) SCLK (shift register clock). Data can be transferred to and from the CLOCK/RAM one byte at a time or in a burst of up to 24 bytes.

TECHNICAL DESCRIPTION

Figure 2 is a block diagram of the CLOCK/RAM chip. Its main elements are the oscillator and divider circuit, oscillator and clock control, the real-time clock/calendar, static RAM, the serial shift register, and the command and control logic.

BLOCK DIAGRAM
Figure 2



The shift register is used to communicate with the outside world. Data on the I/O line is either input or output on each shift register clock pulse when the chip is enabled. If the chip is in the input mode, the data on the I/O line is input to the shift register on the rising edge of SCLK. If in the output mode, data is shifted out onto the I/O line on the falling edge of SCLK.

The command and control logic receives the first byte input by the shift register after $\overline{CE}$ goes active. This byte must be the command byte and will direct further operations within the CLOCK/RAM. The command specifies whether subsequent transfers will be data input or data output, and which register or RAM location will be involved.

A control register provides programmable control of the divider for the internal clock signal, the external clock signal, the crystal type and mode, and the write protect function.

The real-time clock/calendar is accessed via seven registers. These registers control seconds, minutes, hours, day, date, month, and year. Certain bits within these registers also control a run/stop function, 12/24 hour format, and indicate AM or PM (12 hour mode only). These registers can be accessed sequentially in Burst Mode, or randomly in a single byte transfer.

The static RAM is organized as 24 bytes of 8-bits each. They can be accessed either sequentially in burst mode, or randomly in a single byte transfer.

POWER UP

A clock signal is necessary for correct power up, and it should be noted that a delay exists between power up and the correct power up state of the clock and control registers.

DATA TRANSFER

Data Transfer is accomplished under control of the $\overline{CE}$ and SCLK inputs by an external microcomputer. Each transfer consists of a single byte ADDRESS/COMMAND input followed by a single byte or multiple byte (if Burst Mode is specified) data input or output, as specified by the ADDRESS/COMMAND byte. The serial data transfer occurs with LSB first, MSB last format.

ADDRESS/COMMAND BYTE

The ADDRESS/COMMAND Byte is shown below:

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A4	A3	A2	A1	A0	Rd / $\overline{W}$

As defined, the MSB (bit 7) must be a logical 1; bit 6 specifies a Clock/Calendar/Control register if logical 0 or a RAM register if logical 1; bits 1-5 specify the designated

register(s) to be input or output; and the LSB (bit 0) specifies a WRITE operation (input) if logical 0 or READ operation (output) if logical 1.

BURST MODE

Burst Mode may be specified for either the Clock/Calendar/Control registers or for the RAM registers by addressing location 31 Decimal (ADDRESS/COMMAND bits 1-5 = logical 1). As before, bit 6 specifies Clock or RAM and bit 0 specifies read or write.

There is no data storage capability at location 31 in either the Clock/Calendar/Control registers or the RAM registers.

SCLK and $\overline{CE}$ CONTROL

All data transfers are initiated by $\overline{CE}$ going low. After $\overline{CE}$ goes low, the next 8 SCLK cycles input an ADDRESS/COMMAND byte of the proper format. A SCLK cycle is the sequence of a positive edge followed by a negative edge. For data inputs, the data must be valid during the SCLK cycle. If bit 7 is not a logical 1, indicating a valid CLOCK/RAM ADDRESS/COMMAND, the ADDRESS/COMMAND byte is ignored as are all SCLK cycles until $\overline{CE}$ goes high and returns low to initiate a new ADDRESS/COMMAND transfer. See Figure 3.

ADDRESS/COMMAND bits and DATA bits are input on the rising edge of SCLK, and DATA bits are output on the falling edge of SCLK.

A data transfer terminates if $\overline{CE}$ goes high, and the transfer must be reinitiated by the proper ADDRESS/ COMMAND when $\overline{CE}$ again goes low. The data I/O pin is high impedance when $\overline{CE}$ is high.

DATA INPUT

Following the 8 SCLK cycles that input the WRITE Mode ADDRESS/COMMAND byte (bit 0 = logical 0), a DATA byte is input on the rising edge of the next 8 SCLK cycles (per byte, if Burst Mode is specified). Additional SCLK cycles are ignored should they inadvertently occur.

DATA OUTPUT

Following the 8 SCLK cycles that input the READ Mode ADDRESS/COMMAND byte (bit 0 = logical 1), a DATA byte is output on the falling edge of the next 8 SCLK cycles (per byte, if Burst Mode is specified). Additional SCLK cycles retransmit the data byte(s) should they inadvertently occur, so long as $\overline{CE}$ remains low. This operation permits continuous Burst Read Mode capability.

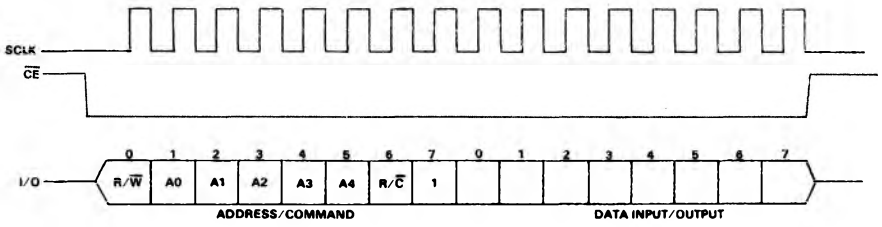
DATA TRANSFER SUMMARY

A data transfer summary is shown in Figure 3.

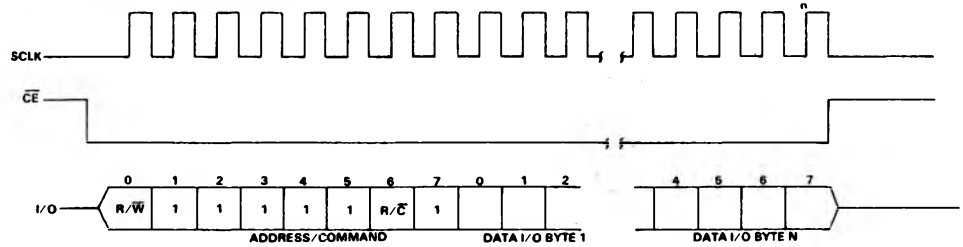
DATA TRANSFER SUMMARY

Figure 3

I. SINGLE BYTE TRANSFER



II. BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

NOTES

1) Data input sampled on rising edge of clock
2) Data output changes on falling edge of clock
3) Rising edge of $\overline{CE}$ terminates operation and resets address/command

REGISTER DEFINITION

CLOCK/CALENDAR

The Clock/Calendar is contained in 7 addressable/writeable/readable registers, as defined below.

Address	Function	Range (BCD)
0	Seconds+Clock Halt Flag	00-59
1	Minutes	00-59
2	Hours/AM-PM/12-24 Mode	00-23 or 01-12
3	Date	01-28,29, 30,31
4	Month	01-12
5	Day	01-07
6	Year	00-99

Data contained in the Clock/Calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the Seconds Register is defined as the Clock Halt Flag. Bit 7 = logical 1 inhibits the 1 Hz input to the Clock/Calendar. Bit 7 is set to logical 1 on power-up to prevent counting, and it may be set high or low by writing to the seconds register under normal operation of the device.

AM-PM/12-24 MODE

Bit 7 of the Hours Register is defined as the 12 or 24 hour mode select bit. When high, the 12 hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

TEST MODE BITS

Bit 7 of the Date Register and Bit 7 of the Day Register are Test Mode Bits utilized in testing the MK3805N/MK3806N. These bits should be logic 0 for normal operation.

CONTROL REGISTER

The Control Register specifies the crystal mode/frequency to be used, the system clock output frequency, and the WRITE PROTECT Mode for data protection. The Control Register is located at address 7 in the Clock/Calendar/Control address space.

7	6	5	4	3	2	1	0
WP	C1	C0	X4	X3	X2	X1	X0

CRYSTAL DIVIDER MODE

X4 and X3 specify the Crystal frequency divider mode selected.

X4	X3	Xtal Mode	Primary Frequencies
0	0	Binary	2^{22}, 2^{21}, 2^{20} Hz
0	1	Microprocessor	8, 5, 4, 2.5, 2, 1.25, 1 MHz
1	0	Baud Rate	7.3728, 3.6864, 1.8432 MHz
1	1	Color Burst	3.5795 MHz

CRYSTAL DIVIDER PRESCALER

X2, X1, and X0 specify a particular prescaler divider selection necessary to generate a 1 Hz frequency for the Clock/Calendar. Refer to Table 2 for complete definition.

SYSTEM CLOCK OUTPUT

C1 and C0 designate the system clock output frequency selected. The options are X, X/2, X/4, and ~2 kHz. When in the Binary Mode and C1, C0 = '1', the output frequency is 2048 Hz. In any other mode, the output frequency is ~2048 Hz. Refer to Table 3 for complete definition.

WRITE PROTECT

Bit 7 of the Control Register is the WRITE PROTECT Flag. Bit 7 is set to logical 1 on power-up, and it may be set high or low by writing to the Control Register. When high, the WRITE PROTECT Flag prevents a write operation to any internal register, including the other bits of the Control Register. Further, logic is included such that the WRITE PROTECT bit may be reset to a logic 0 by a Write operation without altering the other bits of the Control Register.

CLOCK/CALENDAR/CONTROL BURST MODE

Address 31 Decimal of the Clock/Calendar/Control Address space specifies Burst Mode operation. In this mode, the 7 Clock/Calendar Registers and the Control Register may be consecutively read or written. Addresses above address 7 (Control Register) are non-existent; only addresses 0-7 are accessible.

RAM

The static RAM is contained in 24 addressable/writeable/readable registers, addressed consecutively in the RAM address space beginning at location 0.

RAM BURST MODE

Address 31 Decimal of the RAM address space specifies Burst Mode operation. In this mode, the 24 RAM registers may be consecutively read or written. Addresses above the maximum RAM address location are non-existent and are not accessible.

REGISTER SUMMARY

A Register, Data Format summary is shown in Figure 4.

MICROCOMPUTER CLOCK/RAM ADDRESS/COMMAND, REGISTER, DATA FORMAT SUMMARY

Figure 4

I. ADDRESS/COMMAND FORMAT

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A_4	A_3	A_2	A_1	A_0	RD / $\overline{W}$

II. REGISTER ADDRESS

A. CLOCK

	7	6	5	4	3	2	1	0	REGISTER DEFINITION	7	4	3	0	POWER ON RESET
SEC	1	0	0	0	0	0	0	RD / $\overline{W}$	00-59	CH	10 SEC		SEC	80
MIN	1	0	0	0	0	0	1	RD / $\overline{W}$	00-59	0	10 MIN		MIN	00
HR	1	0	0	0	0	1	0	RD / $\overline{W}$	01-12 00-23	12/24	0	10 / A/P	HR	00
DATE	1	0	0	0	0	1	1	RD / $\overline{W}$	01-28/29 01-30 01-31	T_1	0	10 DATE	DATE	01
MONTH	1	0	0	0	1	0	0	RD / $\overline{W}$	01-12	0	0	0	10 M / MONTH	01
DAY	1	0	0	0	1	0	1	RD / $\overline{W}$	01-07	T_2	0	0	0 / 0 / DAY	01
YEAR	1	0	0	0	1	1	0	RD / $\overline{W}$	0-99	10 YEAR			YEAR	00
CONTROL	1	0	0	0	1	1	1	RD / $\overline{W}$		WP	C_1	C_0	X_4 / X_3 / X_2 / X_1 / X_0	A0
CLOCK BURST	1	0	1	1	1	1	1	RD / $\overline{W}$						

B. RAM

RAM 0	1	1	0	0	0	0	0	RD / $\overline{W}$	RAM DATA 0										XX
RAM 23	1	1	1	0	1	1	1	RD / $\overline{W}$	RAM DATA 23										XX
RAM BURST	1	1	1	1	1	1	1	RD / $\overline{W}$											

CRYSTAL FREQUENCY SELECTION

Table 2

X4	X3	X2	X1	X0	f_{XTAL} (MHz) Crystal Frequency	Comments
0	0	0	0	0	8.388608	Power on condition
0	0	0	0	1	8.388608	
0	0	0	1	0	4.194304	
0	0	0	1	1	4.194304	
0	0	1	0	0	2.097152	
0	0	1	0	1	2.097152	
0	0	1	1	0	1.048576	
0	0	1	1	1	0.032768	
0	1	0	0	0	8.000000	
0	1	0	0	1	5.000000	
0	1	0	1	0	4.000000	
0	1	0	1	1	2.500000	
0	1	1	0	0	2.000000	
0	1	1	0	1	1.250000	
0	1	1	1	0	1.000000	
0	1	1	1	1	0.031250	
1	0	0	0	0	7.372800	
1	0	0	0	1	7.372800	
1	0	0	1	0	3.686400	
1	0	0	1	1	3.686400	
1	0	1	0	0	1.843200	
1	0	1	0	1	1.843200	
1	0	1	1	0	0.921600	
1	0	1	1	1	0.028800	
1	1	0	0	0	7.159040	
1	1	0	0	1	7.159040	
1	1	0	1	0	3.579520	
1	1	0	1	1	3.579520	
1	1	1	0	0	1.789760	
1	1	1	0	1	1.789760	
1	1	1	1	0	0.894880	
1	1	1	1	1	0.027965	

CLOCK OUTPUT SELECTION

Table 3

C1	C0	CKO Output Frequency	Comments
0	0	f_{XTAL}	
0	1	$f_{XTAL} \div 2$	Power on condition
1	0	$f_{XTAL} \div 4$	
1	1	2048 Hz	Binary mode

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} relative to GND ..... -0.5 V to + 12.0 V
Voltage on any pin ..... -0.5 V to + V_{CC} + .5
Temperature under bias ..... -50°C + 95°C
Storage Temperature ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

$-40°C \leq T_A \leq +85°C$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	3.0	5.0	9.5	V	1

DC ELECTRICAL CHARACTERISTICS

$-40°C \leq T_A \leq +85°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
I_{CC1}	Power Supply Current			2.0	mA	2
I_{CC2}	Power Supply Current			0.1	mA	3
I_{LI}	Input Leakage Current, SCLK and CE	-1.0		1.0	μA	4
I_{LO}	Output Leakage Current, I/O Pin	-10.0		10.0	μA	4
V_{IH}	Logic "1" Voltage, All Inputs except X1	2.0			V	1, 5
V_{IL}	Logic "0" Voltage, All Inputs			0.8	V	1
V_{IHX2}	Logic "1" Voltage, X_2 Input		3.5			
$V_{I/OH}$	Output Logic "1" Voltage, I/O pin	2.4			V	1(I_{OH}=-100μA)
$V_{I/OL}$	Output Logic "0" Voltage, I/O pin			0.4	V	1(I_{OL}= 1.8 mA)
V_{CKH}	Output Logic "1" Voltage, CKO pin	2.4			V	1(I_{OH} = -400μA)
V_{CKL}	Output Logic "0" Voltage, CKO pin			0.4	V	1(I_{OL} = 4.0 mA)

NOTES:
1. All voltages referenced to GND.
2. Crystal/Clock Input frequency = 8.4 MHz, outputs open.
3. Crystal/Clock Input frequency = 32.768 Hz, outputs open.
4. Measured with $V_{CC} = 5.0V$, $0 \leq V_I \leq 5.0V$, outputs in high impedance state.
5. When X_1 is driven by an external signal, a pull-up resistor is required.

AC ELECTRICAL CHARACTERISTICS

$-40°C \leq T_A \leq +85°C$, V_{CC} 5 V ± 10%

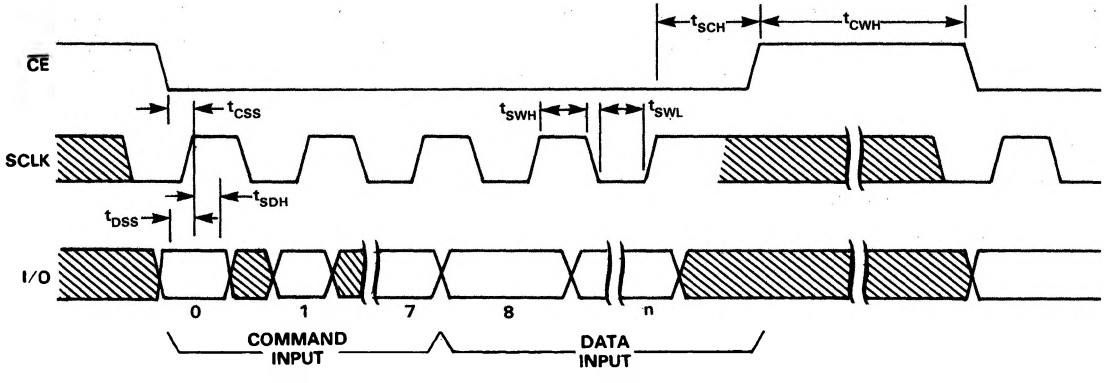
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
C_I	Capacitance on Input pin		6	10	pF	6
$C_{I/O}$	Capacitance on I/O pin		7	12	pF	6
C_X	Capacitance on XI/CI and X2		7	12	pF	6
f_X	Crystal frequency	27		8400	kHz	
t_{CSS}	$\overline{CE}$ to SCLK↑ set up time	1.0			μs	1,7
t_{SCH}	SCLK↑ to $\overline{CE}$↑ hold time	1.0			μs	1,7,12
t_{DSS}	Input Data to SCLK↑ set up time	1.0			μs	1,7
t_{SDH}	Input Data from SCLK↑ hold time	100			ns	1,7
t_{SDD}	Output Data from SCLK↓ delay time	300		1000	ns	1,7,8,9
t_{CDZ}	$\overline{CE}$↑ to I/O high impedance			500	ns	1,7,8,9
t_{SWL}	SCLK low time	1.95		∞	μs	
t_{SWH}	SCLK high time	1.95		∞	μs	
f_{SCLK}	SCLK frequency	DC		250	kHz	
t_{SR}, t_{SF}	SCLK Rise and Fall Time			1	μs	10
t_{CR}, t_{CF}	CKO Rise and Fall Time			50	ns	9,10
t_{CWH}	$\overline{CE}$ high time	2.0			μs	
t_{INIT}	Delay from power up till power up states valid — XTAL=27 kHz			500	ms	11
	XTAL=1 MHz			150	ms	11

NOTES:

6. Measured as $C = \frac{I \Delta t}{\Delta V}$ with ΔV = 3V, and unmeasured pins grounded.
7. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 50 ns rise and fall times on inputs.
8. Measured at V_{OH} = 2.4V and V_{OL} = 0.4V.
9. Load Capacitance = 100 pF
10. t_r and t_f measured from 0.8V to 2.0V
11. t_{INIT} is measured from the time V_{CC} = 4.5 V and XTAL input is valid until the power up states of the CLOCK/RAM registers are valid.
12. t_{SCH} must follow the last rising edge of S_{CLK} during a write cycle in order to allow time to complete a write to the internal register.

I/O TIMING DIAGRAM

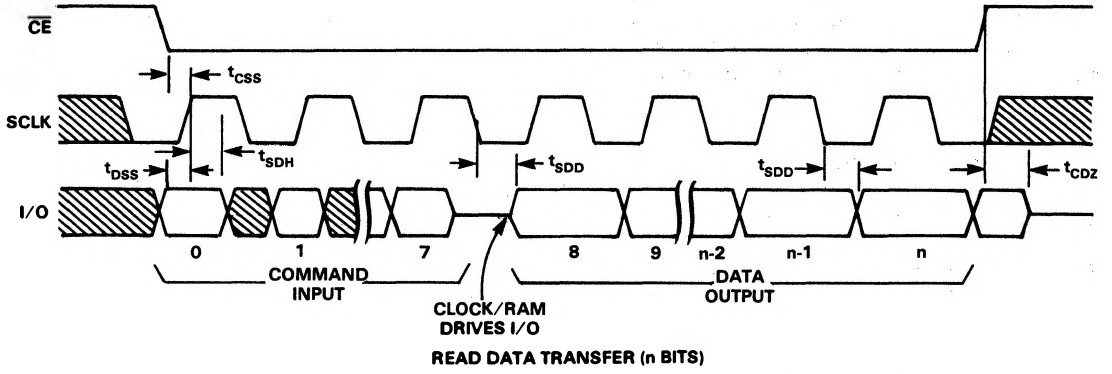
Figure 5



WRITE DATA TRANSFER (n BITS)

I/O TIMING DIAGRAM (Cont.)

Figure 5

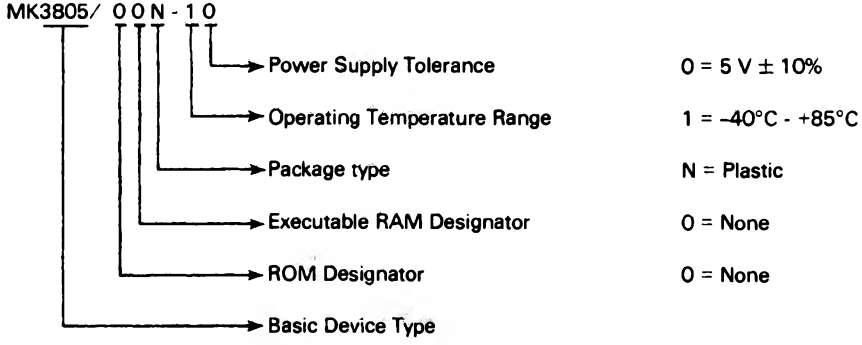


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and executable RAM, the desired package type, temperature range and power supply tolerence. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information describes in the generic part number to define a customer/code specific device order number.

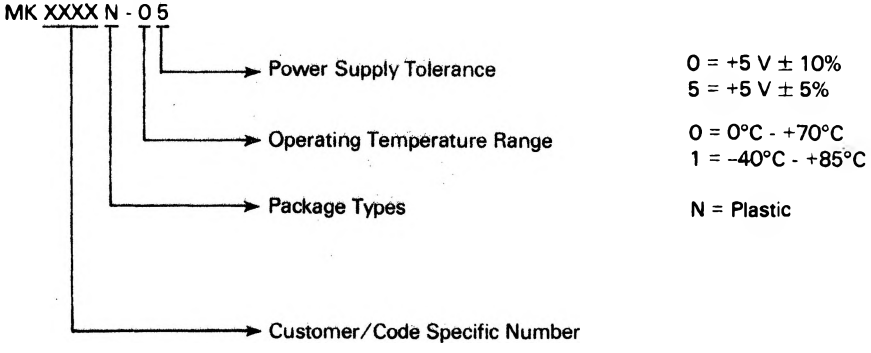
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The customer/code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirement of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.