MOSTEK®

64K-BIT MOS READ-ONLY MEMORY

MK37000(P/J/N) Series

FEATURES

- Organization: 8K x 8 Bit ROM - JEDEC Pinout
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Access Time/Cycle Time

P/N	ACCESS	CYCLE
MK37000-5	300 ns	450 ns
MK37000-4	250 ns	375 ns

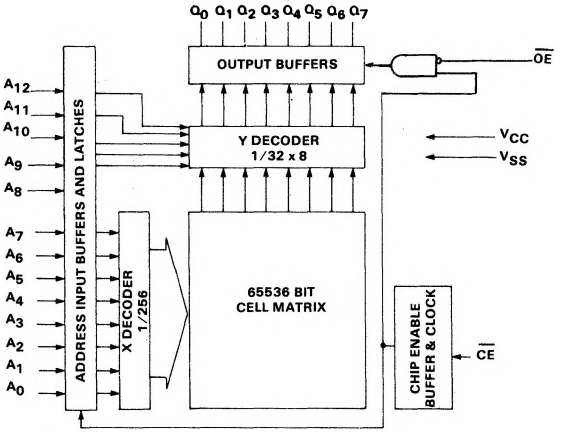
- Mask ROM replacement for 2764 EPROM
- No Connections allow easy upgrade to future generation higher density ROMs
- Low power dissipation: 220mW max active, 45mW max standby
- $\overline{CE}$ and $\overline{OE}$ functions facilitate Bus control
- MKB version screened to MIL-STD-883

DESCRIPTION

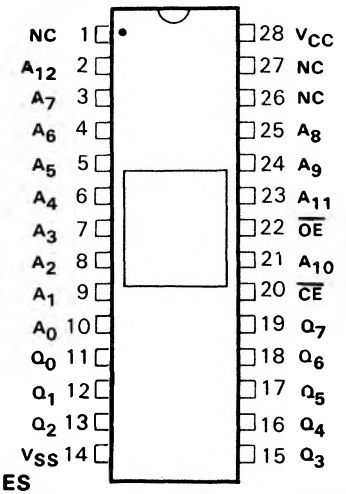
The MK37000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK37000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The MK37000 is to be used as a pin/function compatible mask programmable alternative to the 2764 8K x 8 bit EPROM. As a member of the Mostek BYTEWYDE Memory Family, the MK37000 brings to the memory market a new era of ROM, PROM and EPROM compatibility previously unavailable.

Use of clocked control periphery and a standard static ROM cell makes the MK37000 the lowest power 64K ROM available. Active power is a mere 220mW while standby ($\overline{CE}$ high) is only 45mW. To provide greater system flexibility an output enable ($\overline{OE}$) function has been added using one of the extra pins available on the

FUNCTIONAL DIAGRAM (MK37000)



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

X = Don't Care

PIN NAMES

A0 - A12-Address
$\overline{CE}$ - Chip Enable
Q_0 - Q_7 - Outputs

NC - No Connection
$\overline{OE}$ - Output Enable
V_{CC} - +5V supply
V_{SS} - Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS [6]

($V_{CC} = 5V \pm 10\%$) ($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ $I_{OUT} = 3.3mA$			0.4	V	
V_{OH}	Output Logic "1" Voltage @ $I_{OUT} = -220\mu A$	2.4			V	

AC ELECTRICAL CHARACTERISTICS[6]

($V_{CC} = 5V \pm 10\%$) ($0°C \leq T_A \leq +70°C$)

		-4		-5			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10,000	300	10,000	ns	4
t_{CEA}	$\overline{CE}$ Access Time		250		300	ns	4
t_{CEZ}	Chip Enable Data Off Time		60		75	ns	
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_P	$\overline{CE}$ Precharge Time	125		150		ns	
t_{OEA}	Output Enable Access Time		80		100	ns	
t_{OEZ}	Output Enable Data Off Time		60		75	ns	

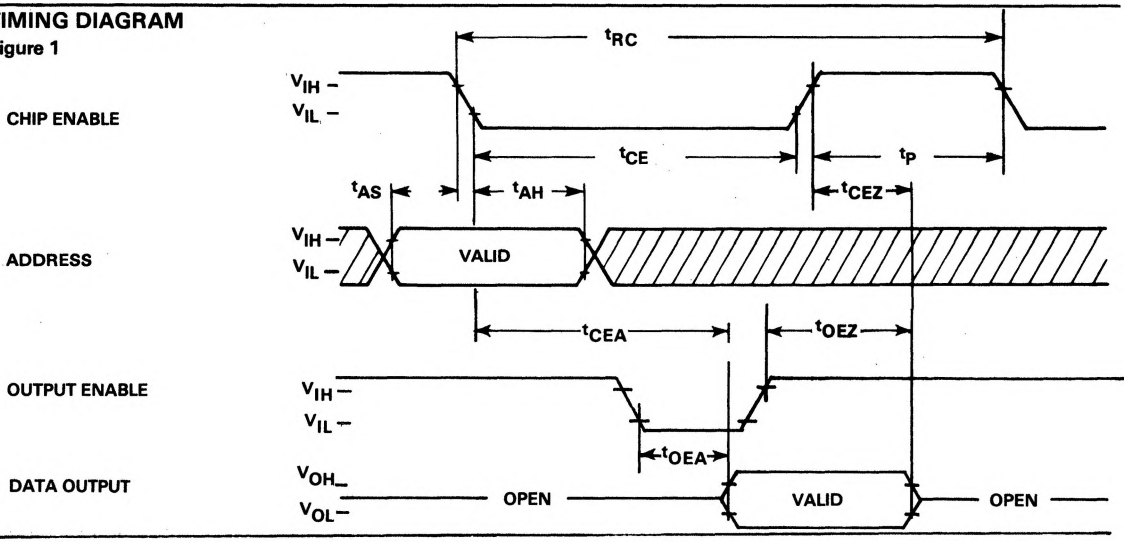
CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM

Figure 1



NOTES:

1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high

DESCRIPTION (Continued)

28 pin DIP. This function matches that found on all of the new BYTEWYDE family of memories available from Mostek.

The use of clocked $\overline{CE}$ mode of operation provides an automatic power down mode of operation. The MK37000 features on chip address latches controlled by the $\overline{CE}$ input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by $\overline{CE}$. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiple devices.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MK37000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MK37000 is packaged in the industry standard 28 pin DIP. Pin 1 and 26 are not connected to allow easy upward compatibility with next generation higher density ROM which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK37000. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK37000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A negative going edge at the $\overline{CE}$ input will activate the device and latch the addresses into the on chip address registers. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access

time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met. The on chip address register allows addresses to be changed after the specified hold time (t_{AH}) in preparation for the next cycle. The outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the inactive state. After chip deselect time (t_{CEZ}) the output buffers will go to a high impedance state. The $\overline{CE}$ input must remain inactive (high) between subsequent cycles for time t_P to allow for precharging the nodes of the internal circuitry.

MK37000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 07FF for a 2K x 8 device. EPROM #2 would then start at address space 0800 and so on. A total of (4) 2K x 8 devices would be required to totally describe the address space of the 8K x 8 MK37000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be excepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

Acceptable EPROMs for Code Data

Table 1

EPROM	# REQUIRED
2716/2516	4
2732	2
2764	1