

MOS Read-Only Memory Character Generators

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} +0.3V to -20V
 Operating temperature range..... 0°C to +75°C
 Storage temperature range..... -55°C to +150°C

RECOMMENDED OPERATING CONDITIONS (0°C ≤ T_A ≤ 75°C)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V _{SS}	Supply voltage	+4.75	+5.0	+5.25	V	See note 1
	V _{DD}	Supply voltage	—	0.0	—	V	
	V _{GG}	Supply voltage	-12.6	-12.0	-11.4	V	
INPUTS	V _{in(o)}	Input voltage, logic "0"	V _{SS} - 1.5	-12.0 +5.0	+0.6	V	See note 2
	V _{in(i)}	Input voltage, logic "1"				V	Count control input should be returned to V _{GG} for ÷ 6 operation, or V _{SS} for ÷ 7 operation
	V _{in(cc)}	Count Control input voltage, ÷ 6 ÷ 7			-11.4	V	
COUNTER TIMING	f _{clk}	Counter Clock input frequency	0		200	kHz	See timing diagrams
	t _{clk(o)}	Clock time at logic "0"	2			μs	
	t _{clk(i)}	Clock time at logic "1"	2			μs	
	t _{r(clk)}	Clock rise time			0.1	μs	
	t _{f(clk)}	Clock fall time			0.1	μs	
	t _{rp}	Reset pulse width	1.0			μs	
	t _{crd}	Clock-to-reset pulse delay	0.4			μs	See note 4

ELECTRICAL CHARACTERISTICS (V_{SS} = +5.0V ±0.25V, V_{GG} = -12.0V ±0.6V, 0°C ≤ T_A ≤ +75°C, unless noted otherwise)

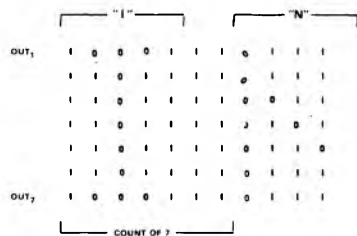
	PARAMETER		MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I _{SS}	Supply current (V _{SS})		20	40	mA	Outputs unconnected
	I _{GG}	Supply current (V _{GG})		20	40	mA	f _{clk} = 200 kHz
INPUTS	C _{in}	Input capacitance			10	pF	V _{in} = V _{SS} , f _{meas} = 1MHz
	I _{in}	Input leakage current			10	μA	V _{in} = V _{SS} - 6V, T _A = 25°C
OUTPUTS	V _{out(o)}	Output voltage, logical "0"	2.4	0.2	0.4	V	I _{out} = 2.0 mA (into output)
	V _{out(i)}	Output voltage, logical "1"				V	I _{out} = 0.6 mA (out of output)
	I _{out}	Data Output leakage current				μA	V _{SS} - 6V ≤ V _{out} ≤ V _{SS} T _A = 25°C (outputs disabled)
DYNAMIC CHARACTERISTICS	t _{AC}	Address-to-output delay time			1	μs	Rise and fall times included in delay times See timing diagrams R _L = 4 kΩ to V _{SS} C _L = 15 pF to V _{DD} T _A = 25°C
	t _{CO}	Clock-to-output delay time			1	μs	
	t _{CCO}	Clock-to-counter output delay time			1	μs	
	t _{BO}	Blanking/unblanking delay time			1	μs	
	t _{OEO}	Output enable/disable delay time			1	μs	
	t _{CRO}	Counter reset delay time			1	μs	
	t _{CRCO}	Reset-to-counter output delay time			1	μs	
	t _F	Output fall time			0.3	μs	
	t _R	Output rise time			0.3	μs	

*Typical values apply at V_{SS} = +5.0V, V_{GG} = -12.0V, T_A = 25°C

- NOTES:**
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = 0V, V_{DD} = -5V, V_{GG} = -17V. Input voltages would also need to be adjusted accordingly.
 2. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
 3. These parameters apply to both the data outputs and counter output.
 4. The counter clock must not make a negative transition within the period t_{crd}, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

TIMING

Timing diagram (1) shows the time relationships between character address, data output, counter clock, and counter output during typical operation of an MK 2300 P Series character generator. An output sequence from the MK 2302 P is shown to help clarify operation. This sequence can be seen from the top rows (OUT₁) of the characters "I" and "N".



All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

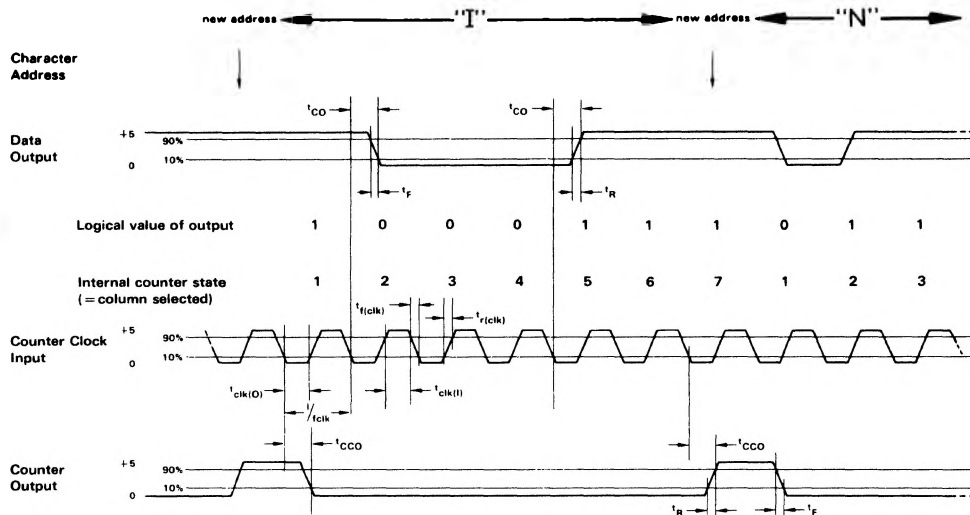
Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control, +5V
Counter Reset, +5V
Blanking Input, +5V
Output Enable, +5V

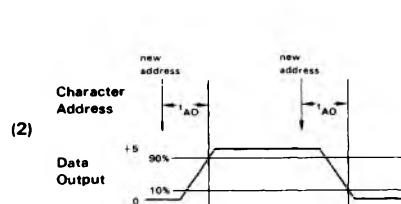
Had the Count Control input been at -12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

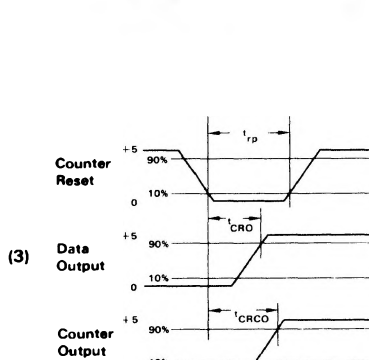
Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.



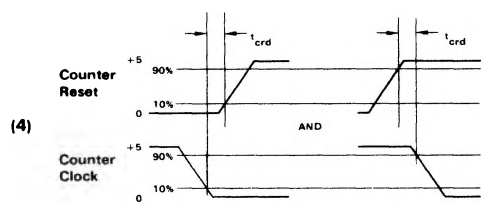
(1)



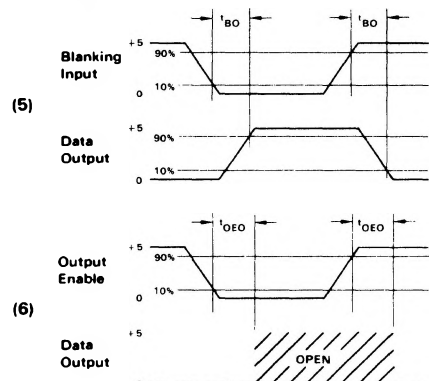
(2)



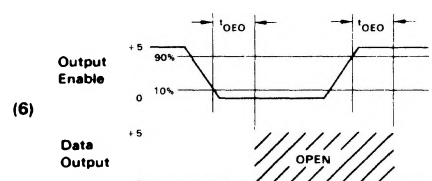
(3)



(4)



(5)



(6)

OPERATING NOTES

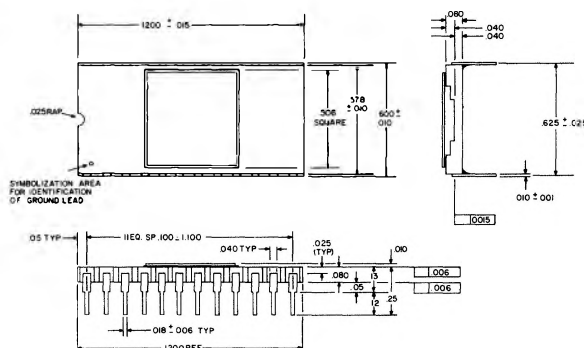
The following table summarizes the MK 2300 P Series input control states and corresponding drive levels:

Count Control	
÷6	-12V
÷7	+5V
Counter Reset	
operate	+5V
reset	0V
Blanking Input	
unblank	+5V
blank*	0V
Output Enable	
enable	+5V
disable**	0V

*All data outputs high (+5V)

**All data outputs open-circuited

PHYSICAL DESCRIPTION (24 lead ceramic dual-in-line hermetic package)



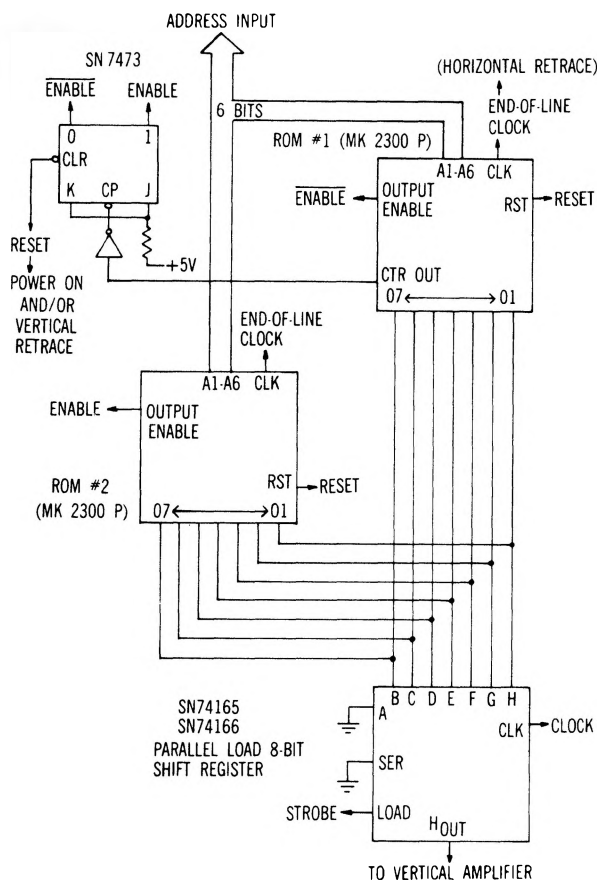
Read Only
Memories

APPLICATION: 7x10 CHARACTER GENERATOR

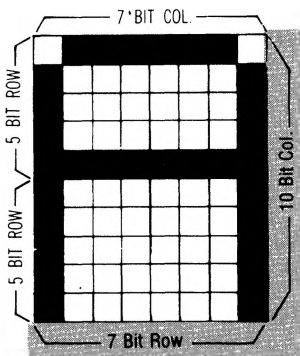
ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 1/2 lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 1/2 lines.



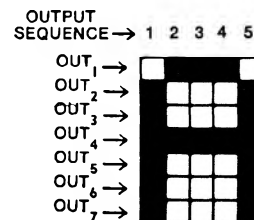
Combining two 5x7 column-output ROMs provides a 7x10 row output.



MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



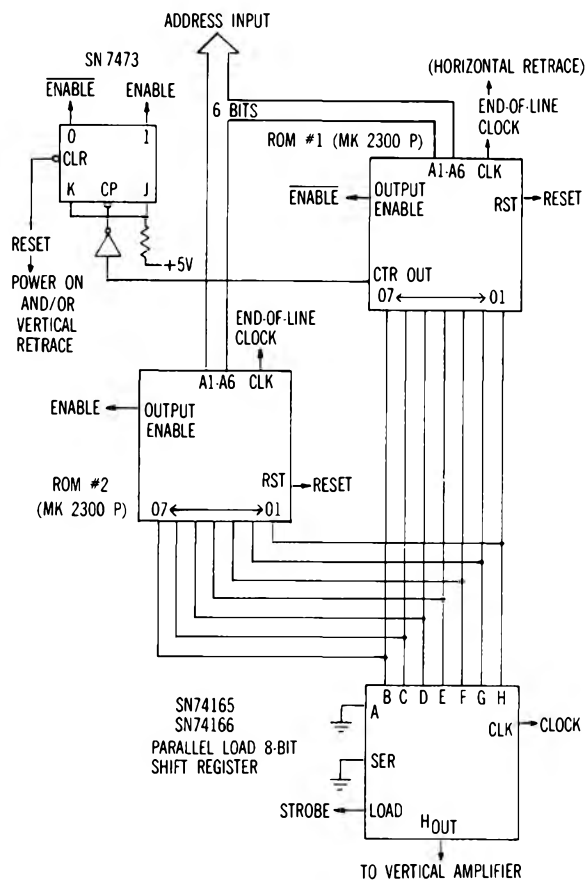
				OUTPUT SEQUENCE → 1 2 3 4 5				
				A ₆	1	1	0	0
A ₄	A ₃	A ₂	A ₁	A ₅	0	1	0	1
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

APPLICATION: 7x10 CHARACTER GENERATOR

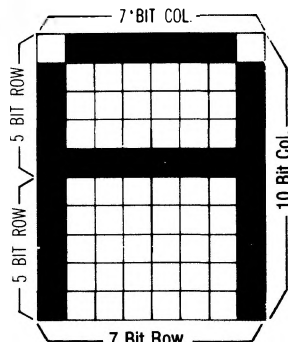
ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 1/2 lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 1/2 lines.



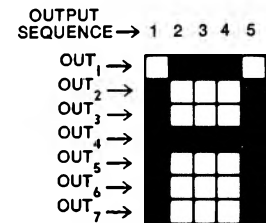
Combining two 5x7 column-output ROMs provides a 7x10 row output.



MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



A ₄	A ₃	A ₂	A ₁	A ₆	1	1	0	0
				A ₅	0	1	0	1
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Read Only
Memories

MOSTEK ROM PUNCHED-CARD CODING FORMAT¹

MK 2300 P

Cols. Information Field

First Card

1-30 Customer
31-50 Customer Part Number
60-72 Mostek Part Number²

Second Card

1-30 Engineer at Customer Site
31-50 Direct Phone Number for Engineer

Third Card

1-5 Mostek Part Number¹
10-15 Organization²

Fourth Card

1-6 Data Format³— "MOSTEK"
15-28 Logic⁴— "Positive Logic" or
35-57 Verification Code⁵

Data Cards⁴

1-6 Binary Address
8-12 First row of character
14-18 Second row of character
20-24 Third row of character
26-30 Fourth row of character
32-36 Fifth row of character
38-42 Sixth row of character
44-48 Seventh row of character

Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

2. Punched as 64x5x7.

3. "MOSTEK" format only is accepted on this part.

4. A dot "ON" should be coded as a "1".

5. Punched as: (a) VERIFICATION HOLD — i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
(b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
(c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.