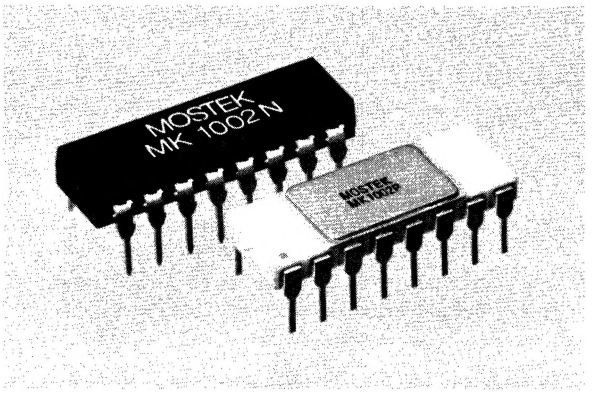
MK 1002 P
MK 1002 N

DUAL 128-BIT
MOS Static Shift Register

MOSTEK



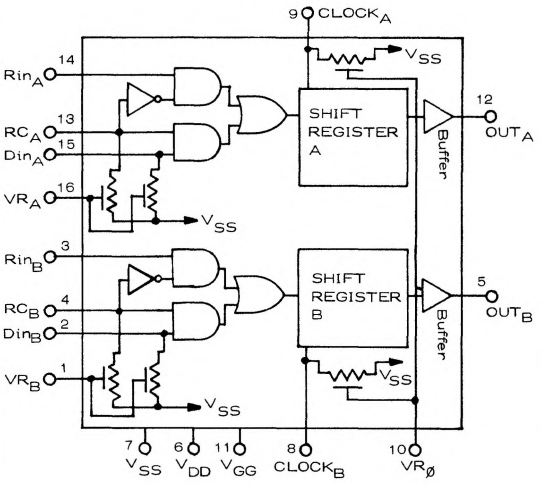
FEATURES:

- ☐ Ion-implanted for full TTL/DTL compatibility — no interface circuitry required
- ☐ Single-phase, TTL/DTL compatible clocks
- ☐ Dual 128-bit static shift registers — 256 bits total
- ☐ Dual sections have independent clocks
- ☐ Recirculate logic built in
- ☐ DC to 1 MHz clock rates
- ☐ Low power dissipation — 130 mW
- ☐ 16-pin dual-in-line package

APPLICATIONS

- ☐ Delay lines
- ☐ Buffer data storage
- ☐ Recycling test data sequencer
- ☐ Digital filtering

FUNCTIONAL DIAGRAM



DESCRIPTION

The MK 1002 is a P-channel MOS static shift register utilizing low threshold-voltage processing and ion-implantation to achieve full TTL/DTL compatibility. Each of the two independent 128 bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL-level external input. In addition, each section has input logic for loading or recirculating data within the register. (See Functional Diagram.) The positive-logic Boolean expression for this action is:

$$\text{OUT (delayed 128 bits)} = (R_C)(D_{in}) + (\overline{R_C})(R_{in})$$

The Data, Recirculate Control, and Clock inputs are provided with internal pull-up resistors to V_{SS} (+5V) for use when driving from TTL. These resistors can be disabled when driving from circuitry with larger output-voltage swings, such as DTL. Enabling of pull-up resistors is accomplished by connecting the appropriate terminal to V_{GG}; disabling by connecting to V_{SS}. The Recirculate inputs are not provided with pull-up resistors since they are generally driven from MOS.

Shifting data into the register is accomplished while the Clock input is low. Output data appears following the positive-going Clock edge. Data in each register can be held indefinitely by maintaining the Clock input high.

OPERATING NOTES

R_C	R_{in}	D_{in}	DATA ENTERED
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

"1" = V_{SS} = +5V
"0" = V_{DD} = Grd
X = No Effect
Output Logic: See Description.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . V_{SS} — 10.0 V
Supply Voltage, V_{GG} . . . . . V_{SS} — 20.0 V
Voltage at any Input or Output . . . . . V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range . . . . . 0°C to +75°C
Storage Temperature Range . . . . . —55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0	V_{ss}	V	
INPUT TIMING	f	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	
	t_{rld}	Recirculate Control Leadtime	100			ns	
	t_{flg}	Recirculate Control Lagtime	300			ns	

ELECTRICAL CHARACTERISTICS

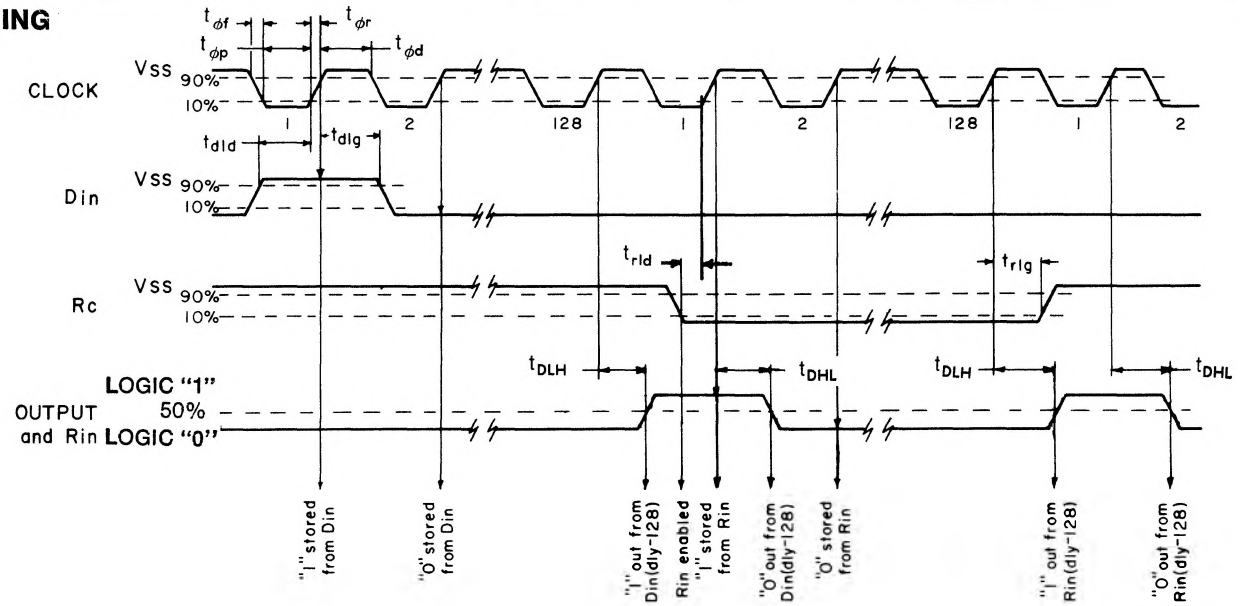
($V_{SS} = +5 \pm 0.25V, V_{GG} = -12 \pm 0.6V, V_{DD} = 0V, T_A = 0°C$ to $+75°C$, using test circuit shown, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		3	10	pF	$V_I = V_{SS}$, f = 1 MHz $T_A = 25°C$
	I_{IL}	Input Current, Logic 0: Resistors Disabled[2]			−40	μA	$V_I = V_{SS} - 5V$
		Resistors Enabled[2]	−0.3		−1.6	mA	$V_I = +0.4V$
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$VR_A, VR_B, VR\phi = V_{SS}$ $V_I = V_{SS}$
	$I_{IR(on)}$	Input Current at Recirculate Inputs[2]			−40	μA	$VR_A, VR_B, VR\phi = V_{GG}$ $V_I = V_{SS} - 5V$
OUTPUTS	V_{OL}	Output Voltage, Logic 0 (3)			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1 (3)	$V_{SS} - 1$			V	$I_L = +100\ \mu$A
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High (3)			450	ns	See Timing Diagram and Test Circuit
	t_{DHL}	Output Delay, High to Low (3)			450	ns	
	t_{VOR}	Output Voltage Rise Time (3)		100	150	ns	
	t_{VOF}	Output Voltage Fall Time (3)		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0V$, $V_{DD} = -5 \pm 0.25V$, $V_{GG} = -17 \pm 0.85V$.
2. MOS pull-up resistors to +5V are provided internally. These MOS resistors are enabled by connecting VR_A, VR_B and $VR\phi$ to V_{GG}, and disabled by connecting VR_A, VR_B and $VR\phi$ to V_{SS}. Pull-up resistors not provided at recirculate inputs.
3. At $T_A = 25°C$.

TIMING



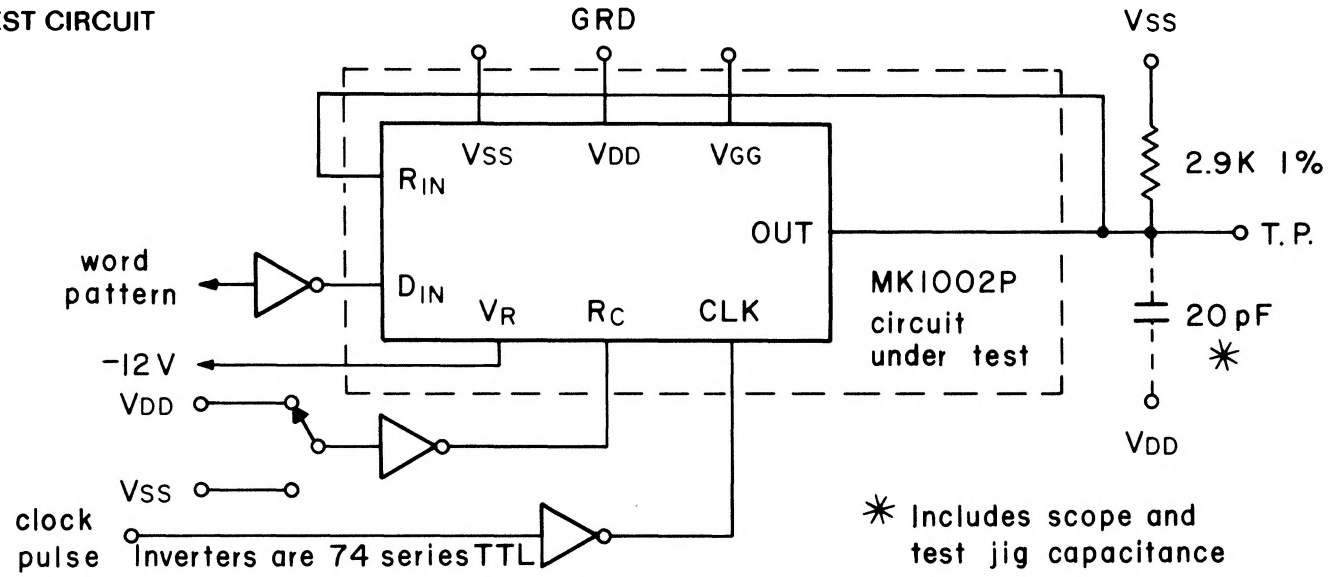
The timing diagram applies to either section of the dual shift register. The test conditions for these waveforms are illustrated below. A logic "1" is defined as +5 V and a logic "0" is defined as 0V

As long as R_C is at a "1", R_{in} is disabled and D_{in} is enabled. The data that is present at D_{in} while the clock is at "0" is shifted in and will be stored as the clock goes to a "1" This data must have been present t_{dld} time prior to the clock "1" edge. The data must also remain in that same state for t_{dlg} time after that edge. These times are necessary to insure proper data storage in the first register-cell.

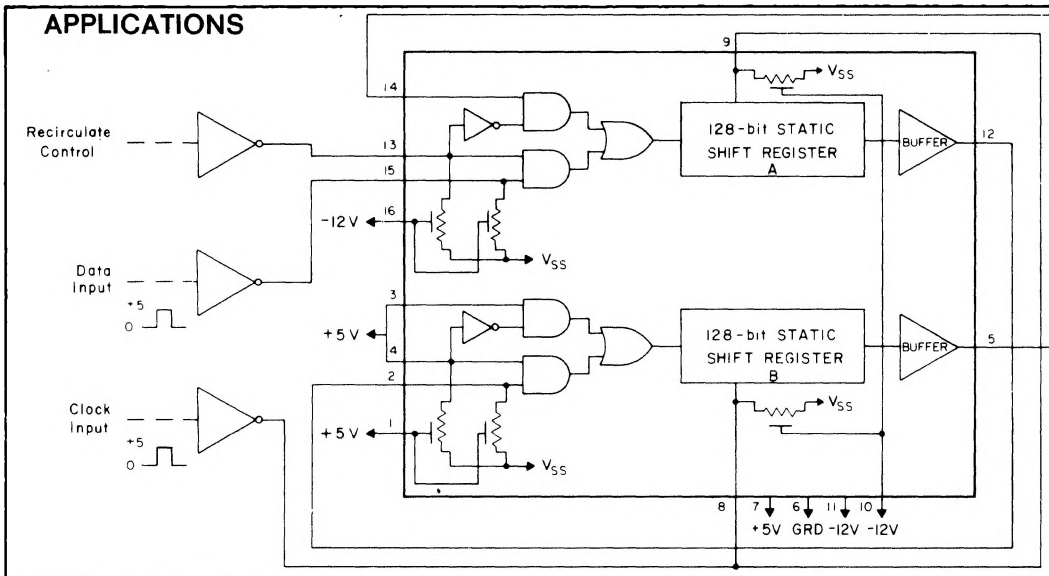
On the clock "1" edge, data is shifted through the register causing bit 127 to be shifted to position 128. This cell's output is buffered and appears at the output in the same logic polarity that appeared at the input 128 clocks prior. This data appears within t_{pd} time of the clock "1" edge.

R_{in} may be hardwired to the data output. When R_C is at a "0", R_{in} is enabled and D_{in} is disabled. Therefore, the output data will appear at the input of the first cell. When R_{in} is tied to the data output, the output delay will insure t_{dlg} and t_{dld} times. R_C "0" time must lead the clock "1" edge by t_{rld} time and must lag that edge by t_{rlg} time to insure proper data storage when recirculate storage is desired.

TEST CIRCUIT



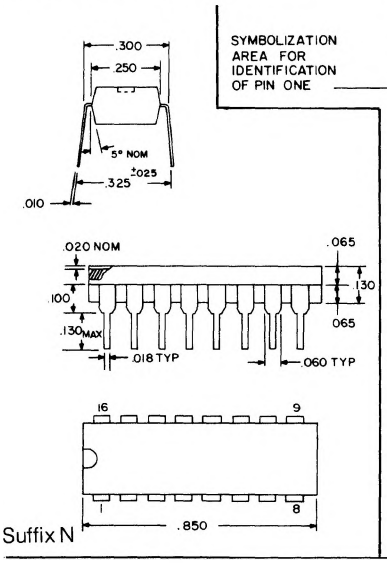
APPLICATIONS



This shows the MK 1002 P connected to operate as a single, 256-bit, static shift register. Pull-up resistors are enabled at TTL driven inputs and disabled at MOS or DTL driven inputs. Any similar TTL/DTL device may be used in place of the inverters shown.

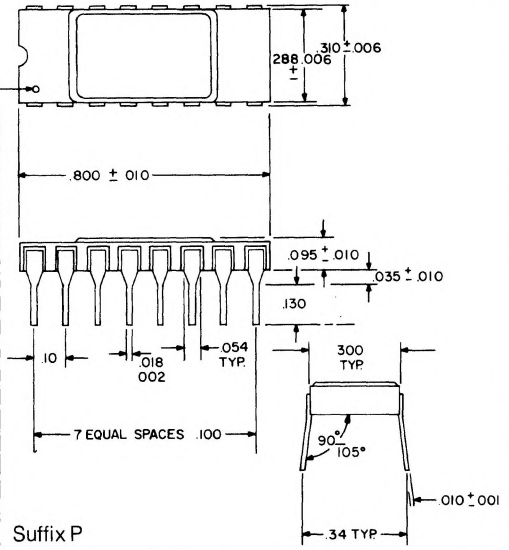
Inverters are 74-series TTL

PACKAGE 16-pin plastic dual-in-line



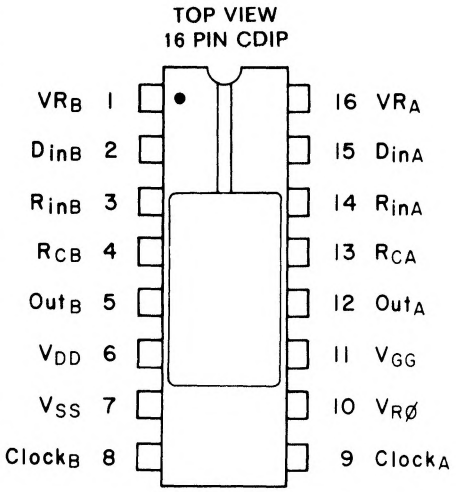
Suffix N

PACKAGE 16-pin ceramic dual-in-line



Suffix P

PIN CONNECTIONS



TYPICAL PERFORMANCE