MK 1002 L

DUAL 128 BIT
MOS Static Shift Register

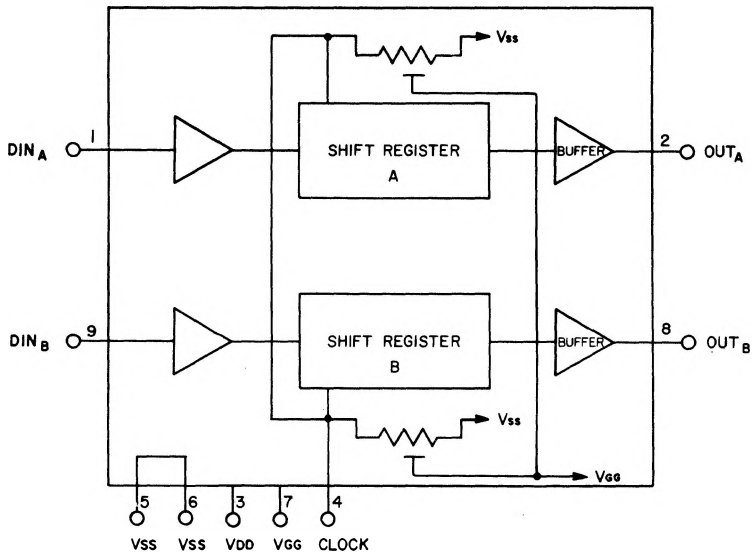
MOSTEK

DESCRIPTION

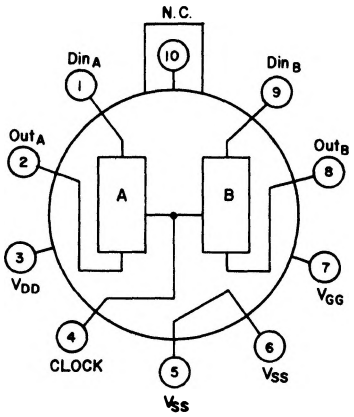
The MK 1002 is a P-channel MOS static shift register utilizing ion implant, low-threshold voltage processing to achieve full TTL/DTL compatibility. Each of the two independent 128-bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL level external input.

Shifting data into the register is accomplished while the clock input is low. Output data appears following the positive-going clock edge. Data in each register can be held indefinitely by maintaining the clock input high.

FUNCTIONAL DIAGRAM



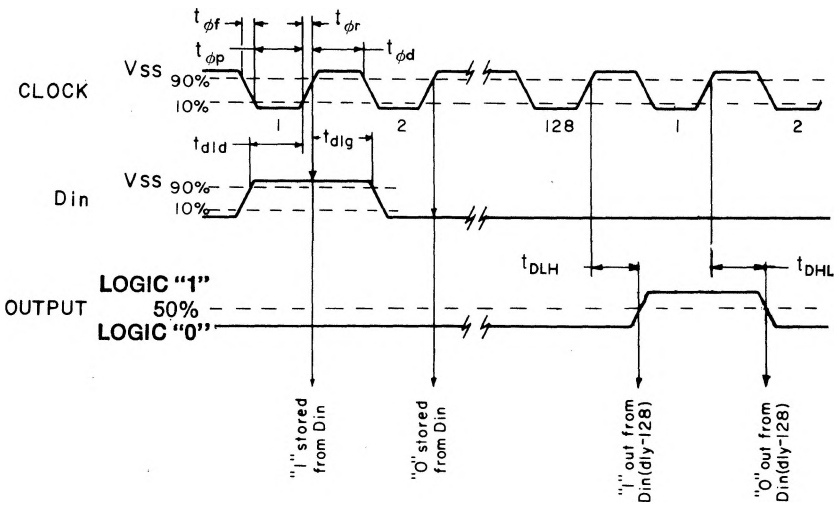
PIN CONNECTIONS



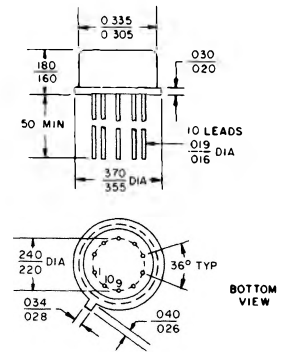
TOP VIEW

N.C. = no connection

TIMING



PACKAGE



NOTES

A ALL DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED

B ALL LEADS WELDABLE AND SOLDERABLE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	V_{SS} — 10.0 V
Supply Voltage, V_{GG}	V_{SS} — 20.0 V
Voltage at any Input or Output	V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range	0°C to +75°C
Storage Temperature Range	—55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0	V_{ss}	V	
INPUT TIMING	f_ϕ	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5 ±0.25V, V_{GG} = −12 ±0.6V, V_{DD} = 0V, T_A = 0°C to +75°C, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	f_ϕ = 1 MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		6	10	pF	$V_I = V_{SS}$, f = 1 MHz
		Clock		12	20	pF	T_A = 25°C
	I_{IL}	Input Current, Logic 0,					
		Data			−40	μA	$V_I = V_{SS}$ —5V
		Clock	-0.6		−3.2	mA	V_I = +0.4V
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$V_I = V_{SS}$
OUTPUTS	V_{OL}	Output Voltage, Logic 0[3]			0.4	V	I_L = −1.6 mA
	V_{OH}	Output Voltage, Logic 1[3]	V_{SS} − 1			V	I_L = +100 μA
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High[3]			450	ns	
	t_{DHL}	Output Delay, High to Low[3]			450	ns	See Timing
	t_{VOR}	Output Voltage Rise Time[3]		100	150	ns	Diagram
	t_{VOF}	Output Voltage Fall Time[3]		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS} = OV, V_{DD} = −5±0.25V, V_{GG} = −17±0.85V.
2. Pull-up resistances to +5V are provided internally at Clock Input.
3. At T_A = 25°C.