DOCUMENT NUMBER
9S12B128DGV1/D

MC9S12B128
Device User Guide
V01.04

Covers also MC9S12B64P

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Semiconductor Products Sector
Motorola, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	20 NOV 2002	20 NOV 2002		Initial version based on MC9S12DGJ64-1.10 Version.
V01.01	27 JAN 2003	01 FEB 2003		updated Table 0-1; added submodule configuration in Section 6 & Section 11. Updated memory map $0118-$011B
V01.02	24 FEB 2003	24 FEB 2003		updated Table 0-1; updated section 2.2.28; Updated memory map $0101.
V01.03	18MAR 2003	18 MAR 2003		added the IIC to the document; added for B64P more details in the preface and the according “Memory Map out of Reset”
V01.04	05MAY 2003	05 MAY 2003		updated bus frequency in **Table A-4**; updated numbers in **A.3.1.2** and **A.3.1.3**

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Derivative Differences and Document References

The **Device User Guide** provides information about the particular system made up of the MC9S12B128.

Derivative Differences

Table 0-1 shows the availability of peripheral modules on the various derivatives. For details about using the HCS12 D family as a development platform for the HCS12B family refer also to engineering bulletin EB388.

Table 0-1 Derivative Differences

Generic device	MC9S12B128	MC9S12B64P
Packages	112LQFP, 80QFP	112LQFP, 80QFP
Mask Set	L80R	L80R
Temp Options	M, V, C	M, V, C
Package Codes	PV, FU	PV, FU
Bus Speed Options	25MHz, 16MHz	25MHz, 16MHz
Note	An errata exists contact Sales office	An errata exists contact Sales office

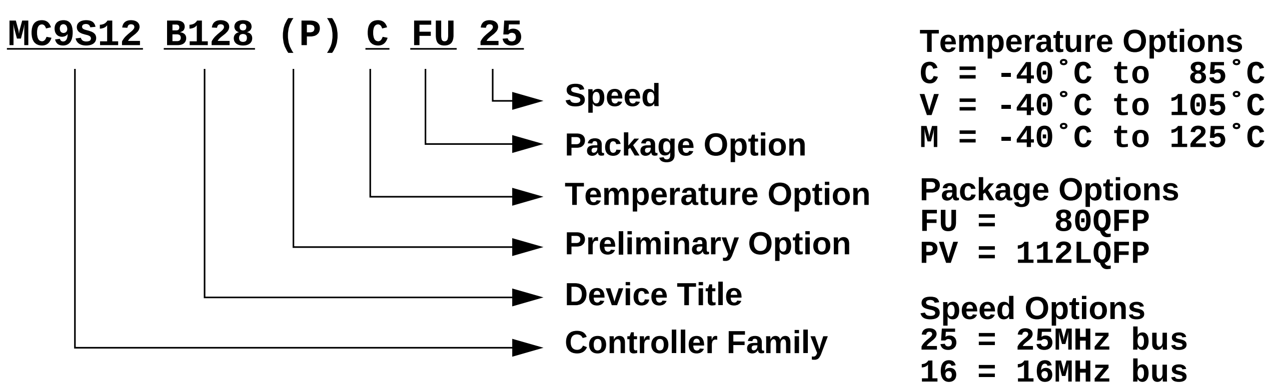


Figure 0-1 Order Partnumber Example

The following items should be considered when using a derivative.

- **Preliminary Option**
  - **Preliminary B64 using B128 die**

    The B128 is tested only for B64 functionality. For the preliminary B64 the upper 2K Bytes RAM of the B128 are reserved and should not be used. Also the pages $38-$3B of Flash are reserved and should not be used.

- **Pins not available in 80 pin QFP package**

– **Port H**
  In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).

– **Port J[1:0]**
  Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+$026C.

– **Port K**
  Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefor care must be taken not to clear this bit.

– **Port M[7:6]**
  PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.

– **Port P6**
  PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.

– **Port S[7:4]**
  PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.

– **PAD[15:8] (ATD channels)**
  Out of reset the ATD channels to PAD[15:8] are disabled preventing current flows in the pins. Do not modify the ATD registers for these channels!

Document References

The Device User Guide provides information about the MC9S12B128 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core User Guide and all the individual Block User Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-2** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-2 Document References

User Guide	Version	Document Order Number
HCS12 V1.5 Core User Guide	1.5	HCS12COREUG
Clock and Reset Generator (CRG) Block User Guide	V04	S12CRGV4/D
Oscillator (OSC) Block User Guide	V02	S12OSCV2/D
Input Capture/Output Compare Timer (TIM_16B8C) Block User Guide	V01	S12TIM16B8CV1/D
Analog to Digital Converter10 Bit 16 Channel (ATD_10B16C) Block User Guide	V03	S12ATD10B16CV3/D

User Guide	Version	Document Order Number
Inter IC Bus (IIC) Block User Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block User Guide	V02	S12SCIV2/D
Serial Peripheral Interface (SPI) Block User Guide	V03	S12SPIV3/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide	V01	S12PWM8B8CV1/D
128K Byte Flash (FTS128K1) Block User Guide	V01	S12FTS128K1V1/D
1K Byte EEPROM (EETS1K) Block User Guide	V01	S12EETS1KV1/D
Motorola Scalable CAN (MSCAN) Block User Guide	V02	S12MSCANV2/D
Voltage Regulator (VREG3V3) Block User Guide	V02	S12VREG3V3V2/D
Port Integration Module (PIM_9B128) Block User Guide	V01	S12PIM9B128V1/D

Section 1 Introduction

1.1 Overview

The MC9S12B128 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 128K bytes of Flash EEPROM, 4K bytes of RAM, 1K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), serial peripheral interface (SPI), an input capture/output compare timer (TIM), 16- channel, 10-bit analog-to-digital converter (ADC), an 8-channel pulse-width modulator (PWM), one CAN 2.0 A, B software compatible module (MSCAN12) and an Inter-IC Bus. The MC9S12B128 has full 16-bit data paths throughout, however, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 22 I/O ports are available with Wake-Up capability from STOP or WAIT mode.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer’s model identical to M68HC11
    iii. Instruction queue
    iv. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Mode)
- CRG
  - Low current Colpitts or
  - Pierce oscillator,
  - PLL,
  - COP watchdog,
  - Real time interrupt,
  - Clock monitor
- 8-bit and 4-bit ports with interrupt functionality

  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 128K Flash EEPROM
  - 1K byte EEPROM
  - 4K byte RAM
- Analog-to-Digital Converter
  - 16-channels for 112 Pin Package, 8 channels for 80 Pin package options
  - 10-bit resolution
  - External conversion trigger capability
- 1M bit per second, CAN 2.0 A, B software compatible module
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Input Capture/Output Compare Timer (TIM)
  - 16-bit Counter with 7-bit Prescaler
  - 8 programmable input capture or output compare channels
  - 16-bit Pulse Accumulators
  - Simple PWM Mode
  - Modulo Reset of Timer Counter
  - External Event Counting
  - Gated Time Accumulation
- 8 PWM channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
  - Usable as interrupt inputs

- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)
- Inter-IC Bus (IIC)
  - Compatible with I2C Bus standard
  - Multi-master operation
  - Software programmable for one of 256 different serial clock frequencies
- Internal 2.5V Regulator
  - Supports an input voltage range from 2.97V to 5.5V
  - Low power mode capability
  - Includes low voltage reset (LVR) circuitry
  - Includes low voltage interrupt (LVI) circuitry
- 112-Pin LQFP or 80 QFP package
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs
  - Operation at 32 MHz equivalent to 16 MHz Bus Speed; Option 50MHz equivalent to 25MHz Bus Speed
  - Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Motorola use only**)

   - Special Peripheral Mode (**Motorola use only**)

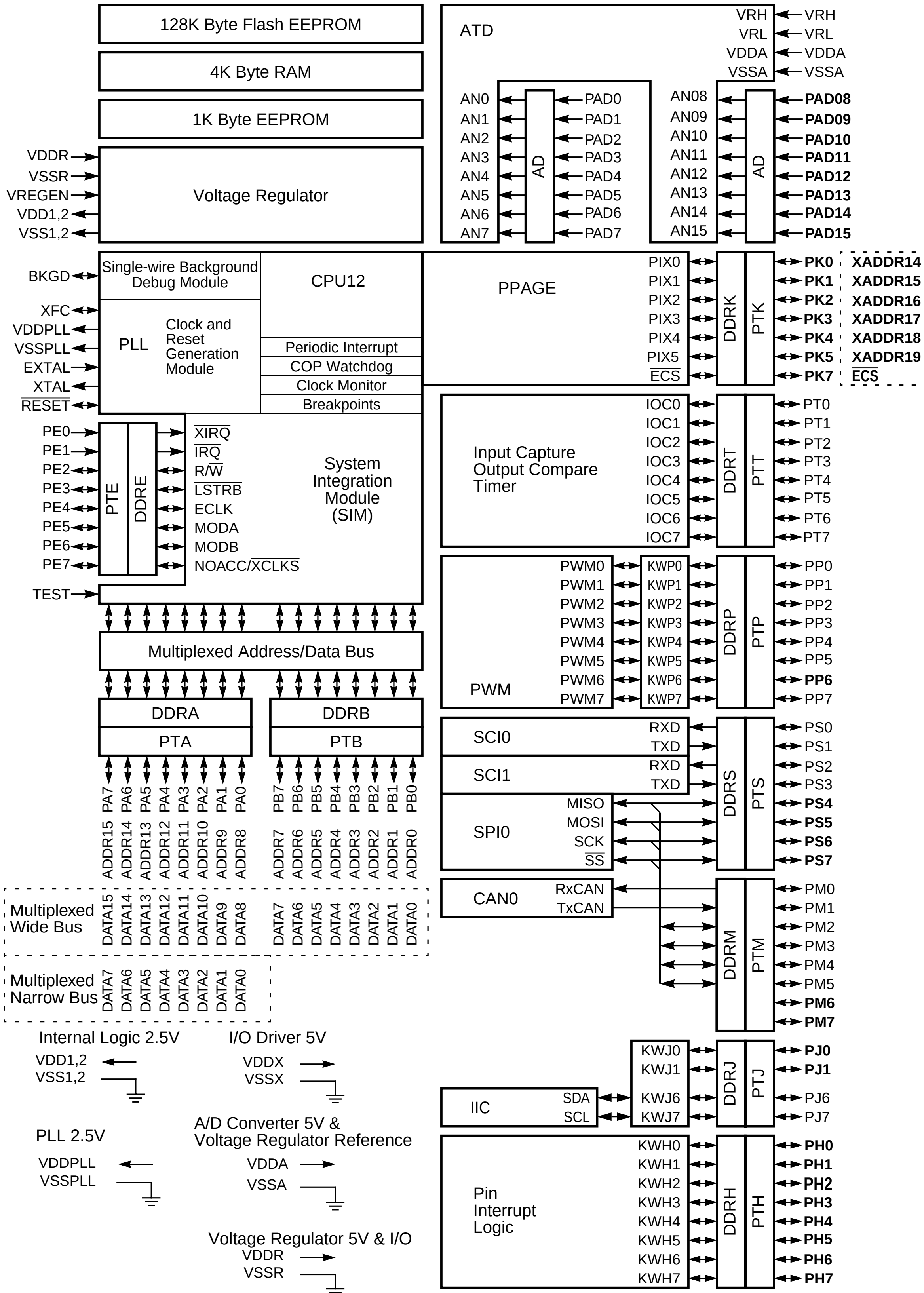
Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12B128 device.

Figure 1-1 MC9S12B128 Block Diagram



1.5 System Memory Map

Table 1-1 and **Figure 1-2** show the device memory map of the MC9S12B128 after reset. The 1K EEPROM is mapped twice in a 2K address space. Note that after reset the bottom 1k of the EEPROM ($0000 - $03FF) are hidden by the register space, and the 1K $0400 - $07FF is hidden by the RAM.

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0000 - $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018	Reserved	1
$0019	Voltage Regulator (VREG)	1
$001A - $001B	Device ID register (PARTID)	2
$001C - $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 - $0027	Reserved	8
$0028 - $002F	CORE (Background Debug Mode)	8
$0030 - $0033	CORE (PPAGE, Port K)	4
$0034 - $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 - $006F	Standard Timer Module16-bit 8-channels (TIM)	48
$0070 - $007F	Reserved	16
$0080 - $00AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$00B0 - $00C7	Reserved	24
$00C8 - $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 - $00D7	Serial Communications Interface 1 (SCI1)	8
$00D8 - $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 - $00E7	Inter IC Bus (IIC)	8
$00E8 - $00FF	Reserved	24
$0100- $010F	Flash Control Register	16
$0110 - $011B	EEPROM Control Register	12
$011C - $013F	Reserved	36
$0140 - $017F	Motorola Scalable Can (CAN0)	64
$0180 - $01FF	Reserved	128
$0200 - $0227	PWM (Pulse Width Modulator 8 Bit 8 Channel)	40
$0228 - $023F	Reserved	24
$0240 - $027F	Port Integration Module (PIM)	64
$0280 - $03FF	Reserved	384
$0000 - $07FF	EEPROM array 1k Array mapped twice in the address space	2048
$0000 - $0FFF	RAM array	4096
$0000 - $3FFF	Fixed Flash EEPROM array	16384
$4000 - $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 - $BFFF	Flash EEPROM Page Window (eight 16k windows)	16384
$C000 - $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 - $FFFF	16384

Figure 1-2 MC9S12B128 Memory Map out of Reset

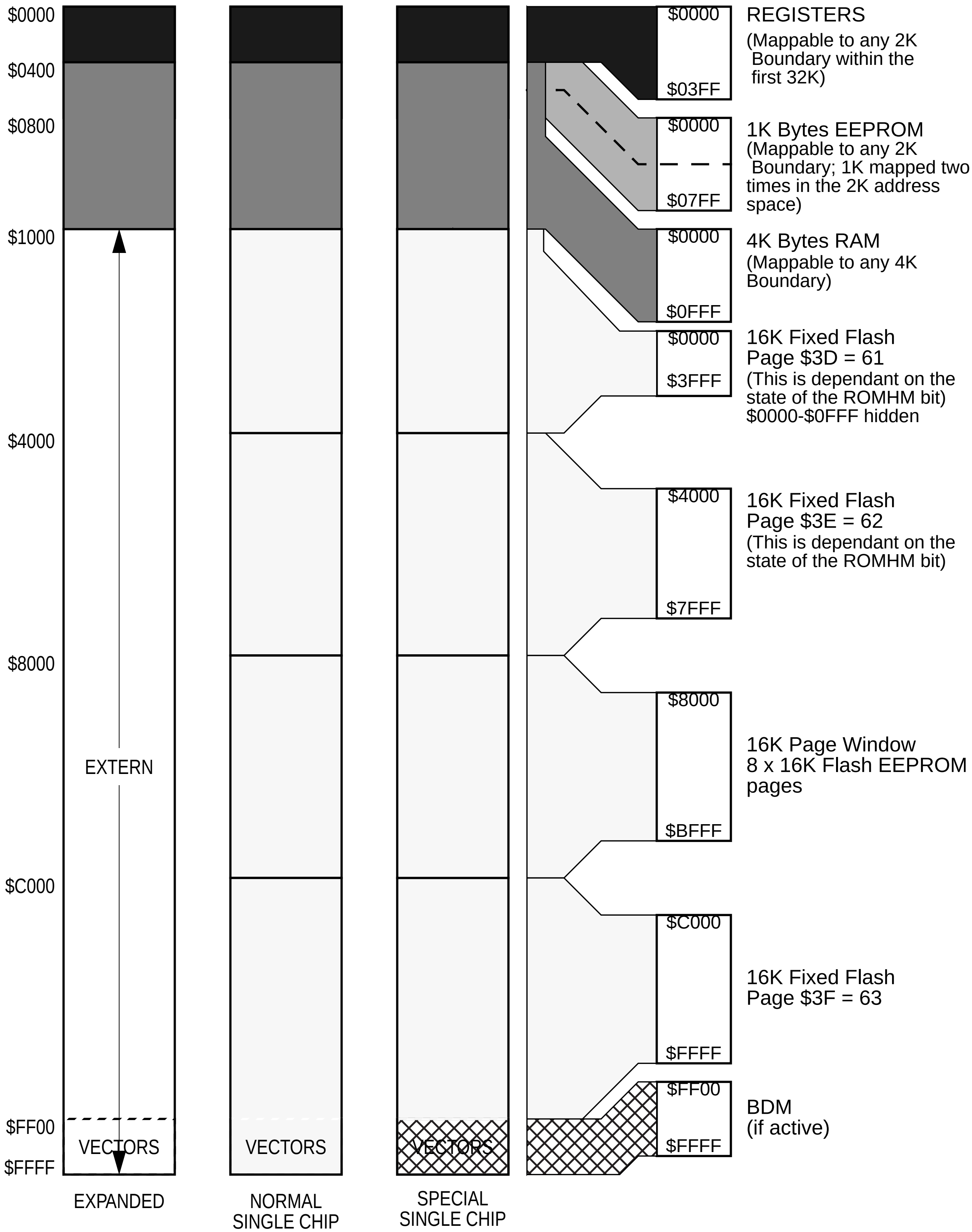
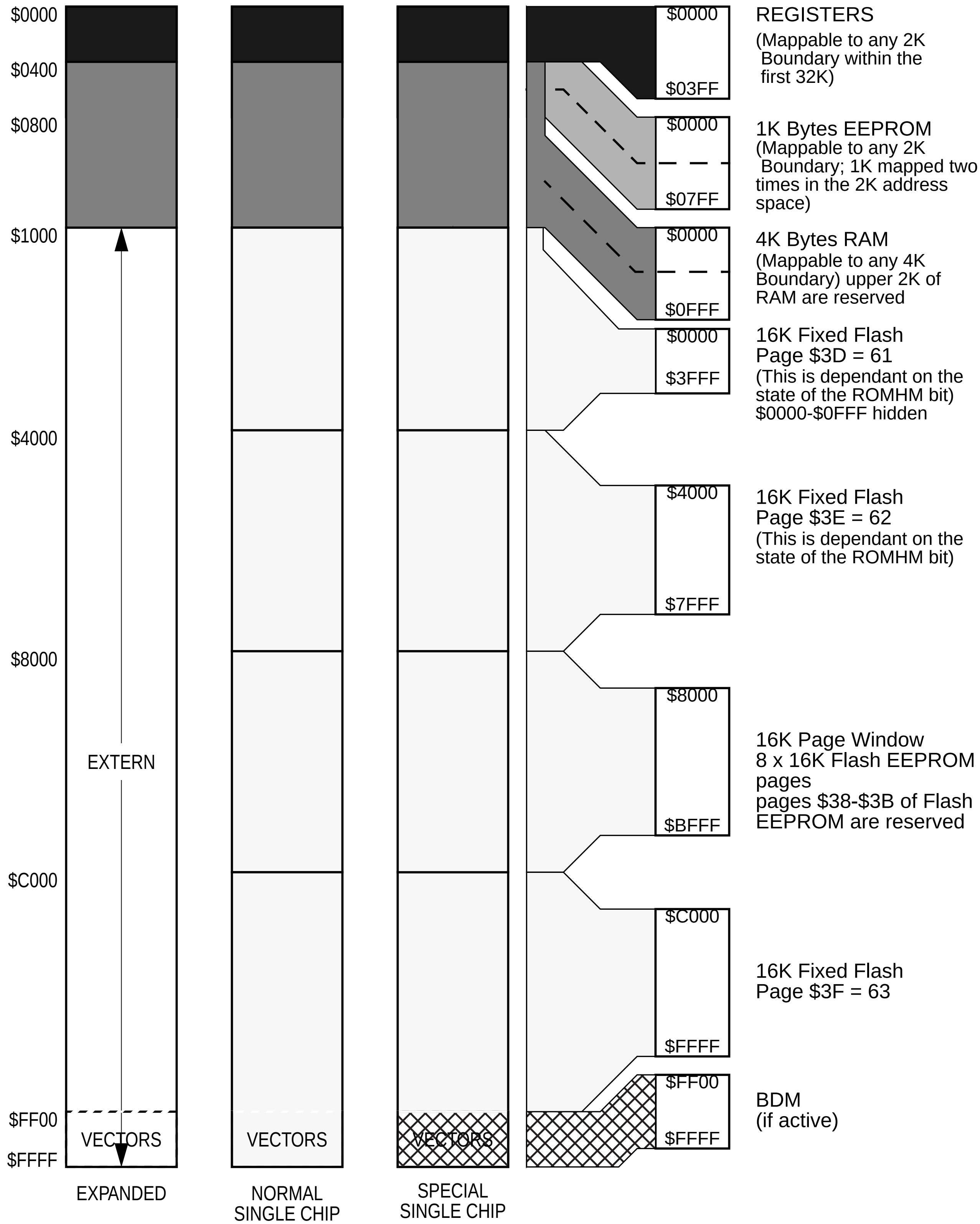


Figure 1-3 MC9S12B64P Memory Map out of Reset



1.5.1 Detailed Register Map

$0000 - $000F MEBI map 1 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								
$0012	INITEE	Read:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		Write:								
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
$0014	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0015 - $0016 INT map 1 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

$0017 - $0017 MMC map 2 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0017	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0018 - $0018 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0018	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0019 - $0019 VREG3V3 (Voltage Regulator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0019	VREGCTRL	Read:	0	0	0	0	0	LVDS	LVIE	LVIF
		Write:								

$001A - $001B Miscellaneous Peripherals (Device User Guide, Table 1-3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

$001C - $001D MMC map 3 of 4 (Core and Device User Guide, Table 1-4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

$001E - $001E MEBI map 2 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

$001F - $001F INT map 2 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $0027 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020 - $0027	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0028 - $002F BKP (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0028	BKPCT0	Read:	BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
		Write:								
$0029	BKPCT1	Read: Write:	BK0MBH	BK0MBL	BK1MBH	BK1MBL	BK0RWE	BK0RW	BK1RWE	BK1RW
$002A	BKP0X	Read:	0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
		Write:								
$002B	BKP0H	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$002C	BKP0L	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$002D	BKP1X	Read:	0	0	BK1V5	BK1V4	BK1V3	BK1V2	BK1V1	BK1V0
		Write:								
$002E	BKP1H	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$002F	BKP1L	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0030 - $0031 MMC map 4 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033 MEBI map 3 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0033	DDRK	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0034 - $003F CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		Write:								
$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		Write:								
$0036	CTFLG test only	Read:	0	0	0	0	0	0	0	0
		Write:								
$0037	CRGFLG	Read:	RTIF	PORF	LVRF	LOCKIF	LOCK	TRACK	SCMIF	SCM
		Write:								
$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		Write:								
$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:								
$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		Write:								
$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:								
$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:								
$003D	FORBYP test only	Read:	0	0	0	0	0	0	0	0
		Write:								
$003E	CTCTL test only	Read:	0	0	0	0	0	0	0	0
		Write:								
$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $006F TIM (Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0040	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		Write:								
$0041	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
$0042	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		Write:								
$0043	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		Write:								
$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		Write:								
$0048	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
$0049	TCTL2	Read:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Write:								

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$004A	TCTL3	Read:/Write:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
$004B	TCTL4	Read:/Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
$004C	TIE	Read:/Write:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
$004D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$004E	TFLG1	Read:/Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
$004F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								
$0050	TC0 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0051	TC0 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0052	TC1 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0053	TC1 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0054	TC2 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0055	TC2 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0056	TC3 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0057	TC3 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0058	TC4 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0059	TC4 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005A	TC5 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005B	TC5 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005C	TC6 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005D	TC6 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005E	TC7 (hi)	Read:/Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005F	TC7 (lo)	Read:/Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0060	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$0061	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0062	PACNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0063	PACNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0064-$006F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0070 - $007F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0070 - $007F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATDCTL0	Read:	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		Write:								
$0081	ATDCTL1	Read:	ETRIGSEL	0	0	0	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
		Write:								
$0082	ATDCTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATDCTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATDCTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATDCTL5	Read:	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
		Write:								
$0086	ATDSTAT0	Read:	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATDTEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATDTEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	ATDSTAT2	Read:	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
		Write:								
$008B	ATDSTAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	ATDDIEN0	Read:	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
		Write:								
$008D	ATDDIEN1	Read:	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		Write:								
$008E	PORTAD0	Read:	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
		Write:								
$008F	PORTAD1	Read:	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		Write:								
$0090	ATDDR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATDDR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0092	ATDDR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATDDR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATDDR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATDDR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATDDR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATDDR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATDDR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATDDR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATDDR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATDDR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATDDR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATDDR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATDDR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATDDR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A0	ATDDR8H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A1	ATDDR8L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A2	ATDDR9H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A3	ATDDR9L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A4	ATDDR10H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A5	ATDDR10L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A6	ATDDR11H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A7	ATDDR11L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A8	ATDDR12H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A9	ATDDR12L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AA	ATDDR13H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00AB	ATDDR13L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AC	ATDDR14H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AD	ATDDR14L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AE	ATDDR15H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AF	ATDDR15L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00B0 - $00C7 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00B0 - $00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCI0BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00C9	SCI0BDL	Read:/Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00CA	SCI0CR1	Read:/Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00CB	SCI0CR2	Read:/Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$00CC	SCI0SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCI0SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00CE	SCI0DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCI0DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCI1BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCI1BDL	Read:/Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00D2	SCI1CR1	Read:/Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00D3	SCI1CR2	Read:/Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

<table>
<tr><th>Address</th><th>Name</th><th></th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td rowspan="2">$00D4</td><td rowspan="2">SCI1SR1</td><td>Read:</td><td>TDRE</td><td>TC</td><td>RDRF</td><td>IDLE</td><td>OR</td><td>NF</td><td>FE</td><td>PF</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00D5</td><td rowspan="2">SCI1SR2</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">BRK13</td><td rowspan="2">TXDIR</td><td>RAF</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00D6</td><td rowspan="2">SCI1DRH</td><td>Read:</td><td>R8</td><td rowspan="2">T8</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00D7</td><td rowspan="2">SCI1DRL</td><td>Read:</td><td>R7</td><td>R6</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td></tr>
<tr><td>Write:</td><td>T7</td><td>T6</td><td>T5</td><td>T4</td><td>T3</td><td>T2</td><td>T1</td><td>T0</td></tr>
</table>

$00D8 - $00DF SPI0 (Serial Peripheral Interface)

<table>
<tr><th>Address</th><th>Name</th><th></th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td rowspan="2">$00D8</td><td rowspan="2">SPI0CR1</td><td>Read:</td><td rowspan="2">SPIE</td><td rowspan="2">SPE</td><td rowspan="2">SPTIE</td><td rowspan="2">MSTR</td><td rowspan="2">CPOL</td><td rowspan="2">CPHA</td><td rowspan="2">SSOE</td><td rowspan="2">LSBFE</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$00D9</td><td rowspan="2">SPI0CR2</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td rowspan="2">MODFEN</td><td rowspan="2">BIDIROE</td><td>0</td><td rowspan="2">SPISWAI</td><td rowspan="2">SPC0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00DA</td><td rowspan="2">SPI0BR</td><td>Read:</td><td>0</td><td rowspan="2">SPPR2</td><td rowspan="2">SPPR1</td><td rowspan="2">SPPR0</td><td>0</td><td rowspan="2">SPR2</td><td rowspan="2">SPR1</td><td rowspan="2">SPR0</td></tr>
<tr><td>Write:</td><td></td><td></td></tr>
<tr><td rowspan="2">$00DB</td><td rowspan="2">SPI0SR</td><td>Read:</td><td>SPIF</td><td>0</td><td>SPTEF</td><td>MODF</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00DC</td><td rowspan="2">Reserved</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00DD</td><td rowspan="2">SPI0DR</td><td>Read:</td><td rowspan="2">Bit7</td><td rowspan="2">6</td><td rowspan="2">5</td><td rowspan="2">4</td><td rowspan="2">3</td><td rowspan="2">2</td><td rowspan="2">1</td><td rowspan="2">Bit0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$00DE</td><td rowspan="2">Reserved</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00DF</td><td rowspan="2">Reserved</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

$00E0 - $00E7 IIC (Inter IC Bus)

<table>
<tr><th>Address</th><th>Name</th><th></th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td rowspan="2">$00E0</td><td rowspan="2">IBAD</td><td>Read:</td><td rowspan="2">ADR7</td><td rowspan="2">ADR6</td><td rowspan="2">ADR5</td><td rowspan="2">ADR4</td><td rowspan="2">ADR3</td><td rowspan="2">ADR2</td><td rowspan="2">ADR1</td><td>0</td></tr>
<tr><td>Write:</td><td></td></tr>
<tr><td rowspan="2">$00E1</td><td rowspan="2">IBFD</td><td>Read:</td><td rowspan="2">IBC7</td><td rowspan="2">IBC6</td><td rowspan="2">IBC5</td><td rowspan="2">IBC4</td><td rowspan="2">IBC3</td><td rowspan="2">IBC2</td><td rowspan="2">IBC1</td><td rowspan="2">IBC0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$00E2</td><td rowspan="2">IBCR</td><td>Read:</td><td rowspan="2">IBEN</td><td rowspan="2">IBIE</td><td rowspan="2">MS/$\overline{SL}$</td><td rowspan="2">TX/$\overline{RX}$</td><td rowspan="2">TXAK</td><td>0</td><td>0</td><td rowspan="2">IBSWAI</td></tr>
<tr><td>Write:</td><td>RSTA</td><td></td></tr>
<tr><td rowspan="2">$00E3</td><td rowspan="2">IBSR</td><td>Read:</td><td>TCF</td><td>IAAS</td><td>IBB</td><td rowspan="2">IBAL</td><td>0</td><td>SRW</td><td rowspan="2">IBIF</td><td>RXAK</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$00E4</td><td rowspan="2">IBDR</td><td>Read:</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>Write:</td></tr>
</table>

$00E0 - $00E7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E8 - $00FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E8 - $00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register (fts128k1)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
$0101	FSEC	Read:	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
$0102	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
		Write:								
$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	FADDRHI	Read: Write:	Bit 15	Bit 14	13	12	11	10	9	Bit 8
$0109	FADDRLO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$010A	FDATAHI	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$010B	FDATALO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$010C - $010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B EEPROM Control Register (eets1k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0112	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0117	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	0	0	Bit8
		Write:								
$0119	EADDRLO	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$011A	EDATAHI	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$011B	EDATALO	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								

$011C - $013F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$011C - $013F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0140 - $017F CAN0 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								

$0140 - $017F CAN0 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0150 - $0153	CAN0IDAR0 - CAN0IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0154 - $0157	CAN0IDMR0 - CAN0IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0158 - $015B	CAN0IDAR4 - CAN0IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$015C - $015F	CAN0IDMR4 - CAN0IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0160 - $016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-2**							
		Write:								
$0170 - $017F	CAN0TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-2**							

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
$0160	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN0RIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
$0161	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CAN0RIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
$0162	Standard ID	Read:								
	CAN0RIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
$0163	Standard ID	Read:								
	CAN0RIDR3	Write:								
$0164- $016B	CAN0RDSR0 - CAN0RDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
$016C	CAN0RDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$016D	Reserved	Read:								
		Write:								
$016E	CAN0RTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$016F	CAN0RTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
$0170	Extended ID CAN0TIDR0	Read: / Write:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	Standard ID	Read: / Write:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
$0171	Extended ID CAN0TIDR1	Read: / Write:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
	Standard ID	Read: / Write:	ID2	ID1	ID0	RTR	IDE=0			
$0172	Extended ID CAN0TIDR2	Read: / Write:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read: / Write:								
$0173	Extended ID CAN0TIDR3	Read: / Write:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	Standard ID	Read: / Write:								
$0174- $017B	CAN0TDSR0 - CAN0TDSR7	Read: / Write:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
$017C	CAN0TDLR	Read: / Write:					DLC3	DLC2	DLC1	DLC0
$017D	CAN0TTBPR	Read: / Write:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
$017E	CAN0TTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$017F	CAN0TTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

$0180 - $01FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0180 - $01FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0200 - $0227 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0200	PWME	Read: / Write:	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
$0201	PWMPOL	Read: / Write:	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
$0202	PWMCLK	Read: / Write:	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0

$0200 - $0227 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0203	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$0204	PWMCAE	Read: Write:	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
$0205	PWMCTL	Read:	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$0206	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$0207	PWMPRSC Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$0208	PWMSCLA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0209	PWMSCLB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$020A	PWMSCNTA Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$020B	PWMSCNTB Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$020C	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$020D	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$020E	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$020F	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$0210	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$0211	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$0212	PWMCNT6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$0213	PWMCNT7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$0214	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0215	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0216	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0217	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0218	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0219	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021A	PWMPER6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021B	PWMPER7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0200 - $0227 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$021C	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021D	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021E	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021F	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0220	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0221	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0222	PWMDTY6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0223	PWMDTY7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0224	PWMSDN	Read:	PWMIF	PWMIE	0	PWMLVL	0	PWM7IN	PWM7INL	PWM7ENA
		Write:			PWMRSTRT					
$0225-$0227	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0228 - $023F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0228 - $023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0240	PTT	Read: Write:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
$0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0242	DDRT	Read: Write:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
$0243	RDRT	Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
$0244	PERT	Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
$0245	PPST	Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTS	Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$024A	DDRS	Read: Write:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
$024B	RDRS	Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
$024C	PERS	Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
$024D	PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
$024E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read: Write:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
$0253	RDRM	Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
$0254	PERM	Read: Write:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
$0255	PPSM	Read: Write:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
$0256	WOMM	Read: Write:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
$0257	MODRR	Read:	0	0	0	MODRR4	0	0	0	0
		Write:								
$0258	PTP	Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read: Write:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
$025B	RDRP	Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
$025C	PERP	Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
$025D	PPSP	Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
$025E	PIEP	Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
$025F	PIFP	Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
$0260	PTH	Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0262	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								
$0263	RDRH	Read:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		Write:								
$0264	PERH	Read:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		Write:								
$0265	PPSH	Read:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		Write:								
$0266	PIEH	Read:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		Write:								
$0267	PIFH	Read:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		Write:								
$0268	PTJ	Read:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
		Write:								
$0269	PTIJ	Read:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
		Write:								
$026A	DDRJ	Read:	DDRJ7	DDRJ7	0	0	0	0	DDRJ1	DDRJ0
		Write:								
$026B	RDRJ	Read:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
		Write:								
$026C	PERJ	Read:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
		Write:								
$026D	PPSJ	Read:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
		Write:								
$026E	PIEJ	Read:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
		Write:								
$026F	PIFJ	Read:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
		Write:								
$0270 - $027F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0280 - $03FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0280 - $03FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B after reset). The read-only value is a unique part ID for each revision of the chip. **Table 1-3** shows the assigned part ID number.

Table 1-3 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12B128	0L80R	$2100

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-4** shows the read-only values of these registers. Refer to section Module Mapping and Control (MMC) of HCS12 Core User Guide for further details.

Table 1-4 Memory size registers

Register name	Value
MEMSIZ0	$11
MEMSIZ1	$C0

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 System Pinout

The MC9S12B128 is available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1** and **Figure 2-2** show the pin assignments.

Figure 2-1 Pin Assignments in 112-pin LQFP for MC9S12B128

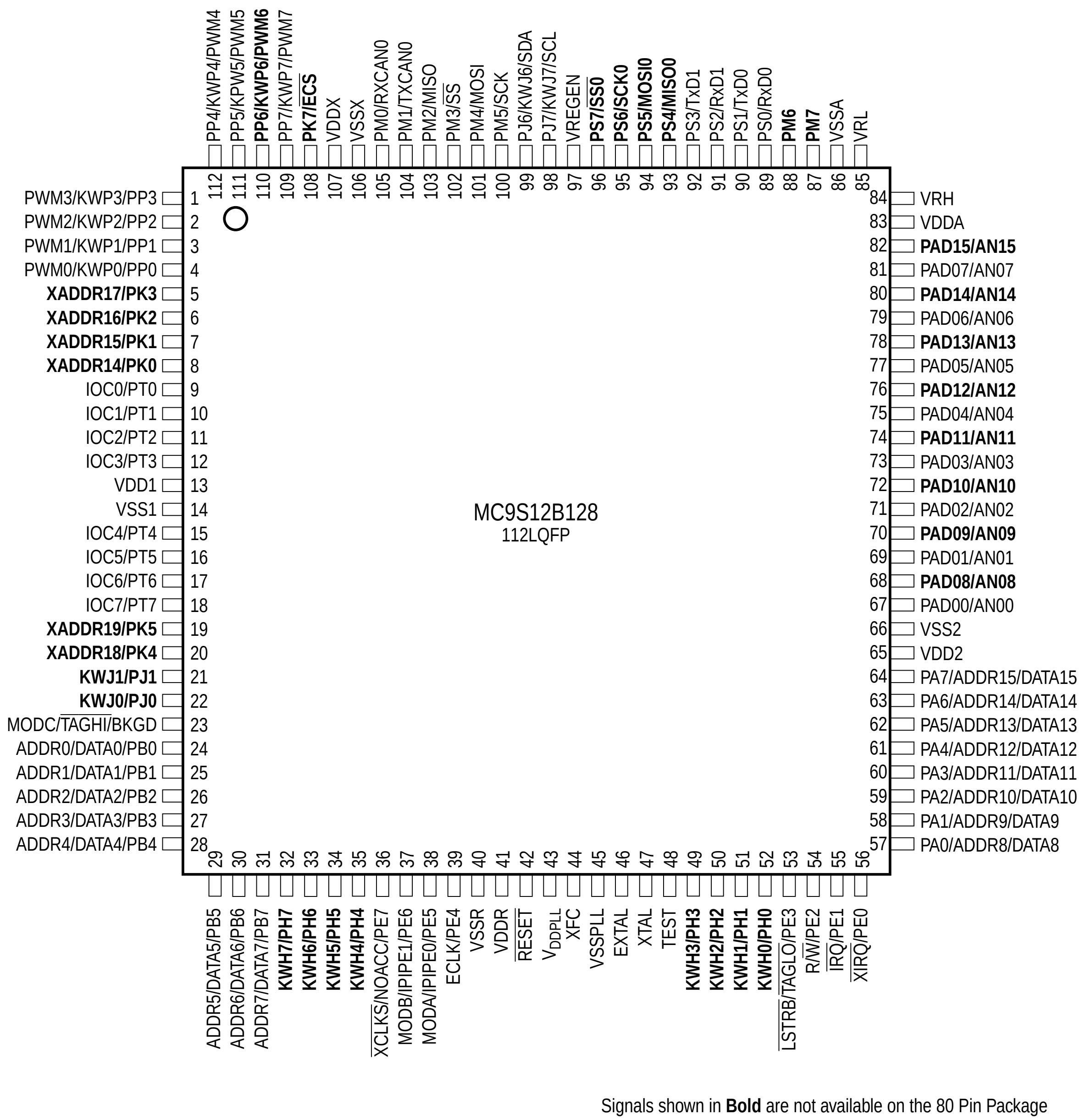
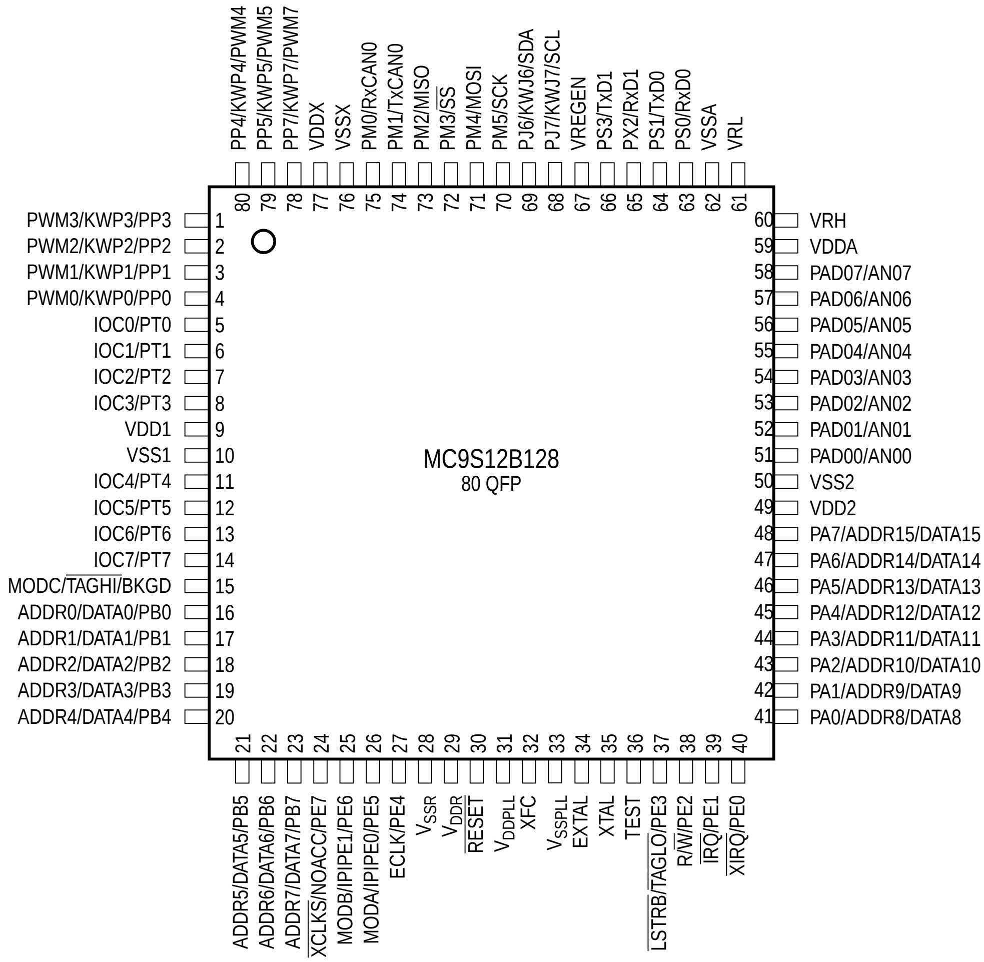


Figure 2-2 Pin Assignments in 80-pin QFP for MC9S12B128



2.1.1 Signal Properties Summary

Table 2-1 summarizes the pin functionality. Signals shown in **bold** are not available in the 80 pin package.

Table 2-1 Signal Properties

Pin Name Function1	Pin Name Function2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	None	None	Oscillator Pins
XTAL	—	—	—				
$\overline{\text{RESET}}$	—	—	—	VDDR			External Reset
TEST	—	—	—	N.A.			Test Input
VREGEN	—	—	—	VDDX			Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL			PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD[15:8]	**AN[15:8]**	**—**	**—**	VDDA	None	None	**Port AD Inputs, Analog Inputs AN[15:8] of ATD**
PAD[07:00]	AN[07:00]	—	—				Port AD Inputs, Analog Inputs AN[7:0] of ATD
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	PUCR/ PUPAE	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—		PUCR/ PUPBE		Port B I/O, Multiplexed Address/Data
PE7	NOACC	$\overline{\text{XCLKS}}$	—		PUCR/ PUPEE	Up	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—		While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—				Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—		PUCR/ PUPEE	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—				Port E I/O, Byte Strobe, Tag Low
PE2	R/$\overline{\text{W}}$	—	—				Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—				Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—				Port E Input, Non Maskable Interrupt
PH7	**KWH7**	—	—		PERH/ PPSH	Disabled	**Port H I/O, Interrupt**
PH6	**KWH6**	—	—				**Port H I/O, Interrupt**
PH5	**KWH5**	—	—				**Port H I/O, Interrupt**
PH4	**KWH4**	—	—				**Port H I/O, Interrupt**
PH3	**KWH3**	—	—				**Port H I/O, Interrupt**
PH2	**KWH2**	—	—				**Port H I/O, Interrupt**
PH1	**KWH1**	—	—				**Port H I/O, Interrupt**
PH0	**KWH0**	—	—				**Port H I/O, Interrupt**
PJ7	KWJ7	SCL	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt,SCL of IIC,
PJ6	KWJ6	SDA	—				Port J I/O, Interrupt,SDA of IIC,
PJ[1:0]	**KWJ[1:0]**	**—**	**—**				**Port J I/O, Interrupts**

Pin Name Function1	Pin Name Function2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
PK7	**$\overline{ECS}$**	**ROMCTL**	**—**	VDDX	PUCR/ PUPKE	Up	**Port K I/O, Emulation Chip Select, ROM On Enable**
PK[5:0]	**XADDR[19:14]**	**—**	**—**				**Port K I/O, Extended Addresses**
PM7	**—**	**—**	**—**		PERM/ PPSM	Disabled	**Port M I/O**
PM6	**—**	**—**	**—**				**Port M I/O**
PM5	—	SCK	—				Port M I/O, SCK of SPI0
PM4	—	MOSI	—				Port M I/O, MOSI of SPI0
PM3	—	$\overline{SS0}$	—				Port M I/O, $\overline{SS}$ of SPI0
PM2	—	MISO0	—				Port M I/O, MISO of SPI0
PM1	TXCAN0	—	—				Port M I/O, TX of CAN0
PM0	RXCAN0	—	—				Port M I/O, RX of CAN0
PP7	KWP7	PWM7	—		PERP/ PPSP		Port P I/O, Interrupt, Channel 7 of PWM
PP6	**KWP6**	**PWM6**	**—**				**Port P I/O, Interrupt, PWM Channel 6**
PP5	KWP5	PWM5	—				Port P I/O, Interrupt, PWM Channel 5
PP4	KWP4	PWM4	—				Port P I/O, Interrupt, PWM Channel 4
PP3	KWP3	PWM3	—				Port P I/O, Interrupt, PWM Channel 3
PP2	KWP2	PWM2	—				Port P I/O, Interrupt, PWM Channel 2
PP1	KWP1	PWM1	—				Port P I/O, Interrupt, PWM Channel 1
PP0	KWP0	PWM0	—				Port P I/O, Interrupt, PWM Channel 0
PS7	**$\overline{SS0}$**	**—**	**—**		PERS/ PPSS	Up	**Port S I/O, $\overline{SS}$ of SPI0**
PS6	**SCK0**	**—**	**—**				**Port S I/O, SCK of SPI0**
PS5	**MOSI0**	**—**	**—**				**Port S I/O, MOSI of SPI0**
PS4	**MISO0**	**—**	**—**				**Port S I/O, MISO of SPI0**
PS3	TXD1	—	—				Port S I/O, TXD of SCI1
PS2	RXD1	—	—				Port S I/O, RXD of SCI1
PS1	TXD0	—	—				Port S I/O, TXD of SCI0
PS0	RXD0	—	—				Port S I/O, RXD of SCI0
PT[7:0]	IOC[7:0]	—	—		PERT/ PPST	Disabled	Port T I/O, Timer channels

2.2 Detailed Signal Descriptions

2.2.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.2.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.2.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.2.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.2.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Motorola representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

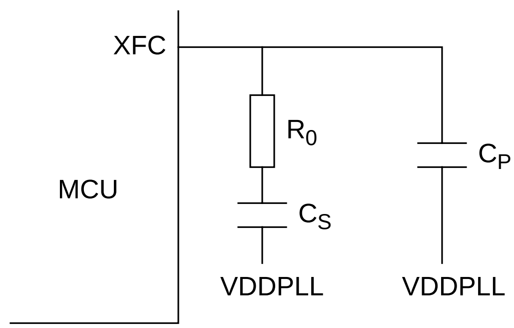


Figure 2-3 PLL Loop Filter Connections

2.2.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. This pin has a permanently enabled pull-up device.

2.2.7 PAD[15:0] / AN[15:0] — Port AD Input Pins ATD

PAD15 - PAD0 are general purpose input pins and analog inputs AN[15:0] of the analog to digital converter ATD.

2.2.8 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.2.9 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.2.10 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.
The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.

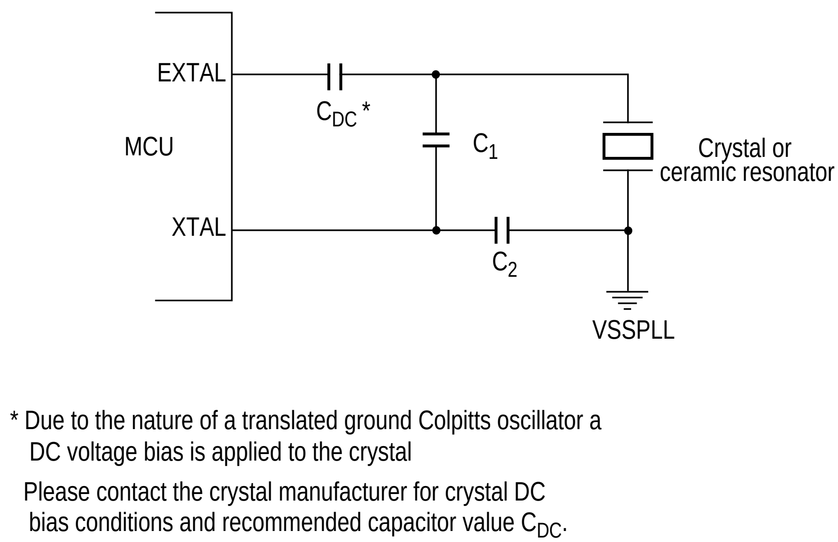


Figure 2-4 Colpitts Oscillator Connections (PE7=1)

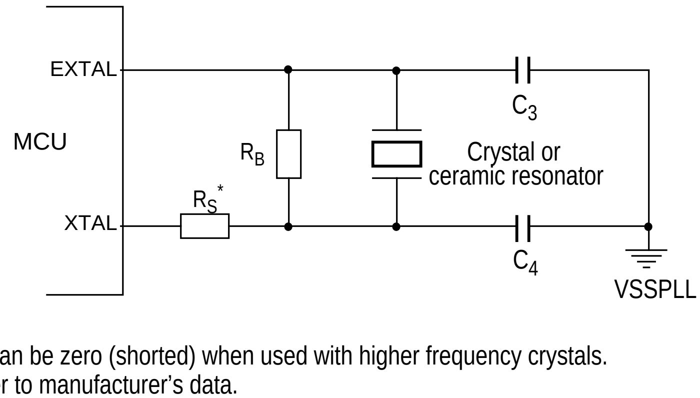


Figure 2-5 Pierce Oscillator Connections (PE7=0)

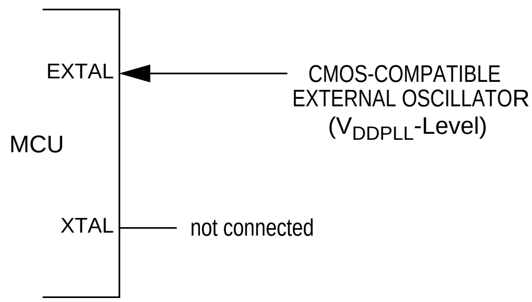


Figure 2-6 External Clock Connections (PE7=0)

2.2.11 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.2.12 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.2.13 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.2.14 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

2.2.15 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.2.16 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.2.17 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.2.18 PH7 / KWH7 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.19 PH6 / KWH6 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.20 PH5 / KWH5 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.21 PH4 / KWH4 — Port H I/O Pin 2

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.22 PH3 / KWH3 — Port H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.23 PH2 / KWH2 — Port H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.24 PH1 / KWH1 — Port H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.25 PH0 / KWH0 — Port H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.26 PJ7 / KWJ7 / SCL — Port J I/O Pins 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial clock pin SCL of the IIC module.

2.2.27 PJ6 / KWJ6 / SDA — Port J I/O Pins 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial data pin SDA of the IIC module.

2.2.28 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.2.29 PK7 / $\overline{ECS}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{ECS}$). While configurating MCU expanded modes this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{RESET}$, the state of this pin is latched to the ROMON bit. For a complete list of modes refer to **4.2 Chip Configuration Summary**.

2.2.30 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

2.2.31 PM7 — Port M I/O Pin 7

PM7 is a general purpose input or output pin.

2.2.32 PM6 — Port M I/O Pin 6

PM6 is a general purpose input or output pin.

2.2.33 PM5 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.2.34 PM4 / MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

2.2.35 PM3 / $\overline{\text{SS0}}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 0 (SPI0).

2.2.36 PM2 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

2.2.37 PM1 / TXCAN0 — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0).

2.2.38 PM0 / RXCAN0 — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0).

2.2.39 PP7 / KWP7 / PWM7 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output.

2.2.40 PP6 / KWP6 / PWM6 — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output.

2.2.41 PP5 / KWP5 / PWM5 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output.

2.2.42 PP4 / KWP4 / PWM4 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output.

2.2.43 PP3 / KWP3 / PWM3 — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output.

2.2.44 PP2 / KWP2 / PWM2 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output.

2.2.45 PP1 / KWP1 / PWM1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output.

2.2.46 PP0 / KWP0 / PWM0 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output.

2.2.47 PS7 / $\overline{\text{SS0}}$ — Port S I/O Pin 7

PS6 is a general purpose input or output pin. It can be configured as the slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 0 (SPI0).

2.2.48 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.2.49 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.2.50 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.2.51 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.2.52 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.2.53 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.2.54 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.2.55 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Timer (TIM).

2.3 Power Supply Pins

MC9S12B128 power and ground pins are described below.

NOTE: *All VSS pins must be connected together in the application.*

Table 2-2 MC9S12B128 Power and Ground Connection Summary

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
VDD1, 2	13, 65	2.5V	Internal power and ground generated by internal regulator
VSS1, 2	14, 66	0V	
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5.0V	Internal Voltage Regulator enable/disable

2.3.1 VDDX, VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDX and VSSX are the supplies for Ports J, K, M, P, T and S.

2.3.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDR and VSSR are the supplies for Ports A, B, E and H.

2.3.3 VDD1, VDD2, VSS1, VSS2 — Core Power Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

2.3.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the two analog to digital converters. It also provides the reference for the internal voltage regulator. This allows the supply voltage to ATD0/ATD1 and the reference voltage to be bypassed independently.

2.3.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.3.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

2.3.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

Section 3 System Clock Description

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the CRG Block User Guide for details on clock generation.

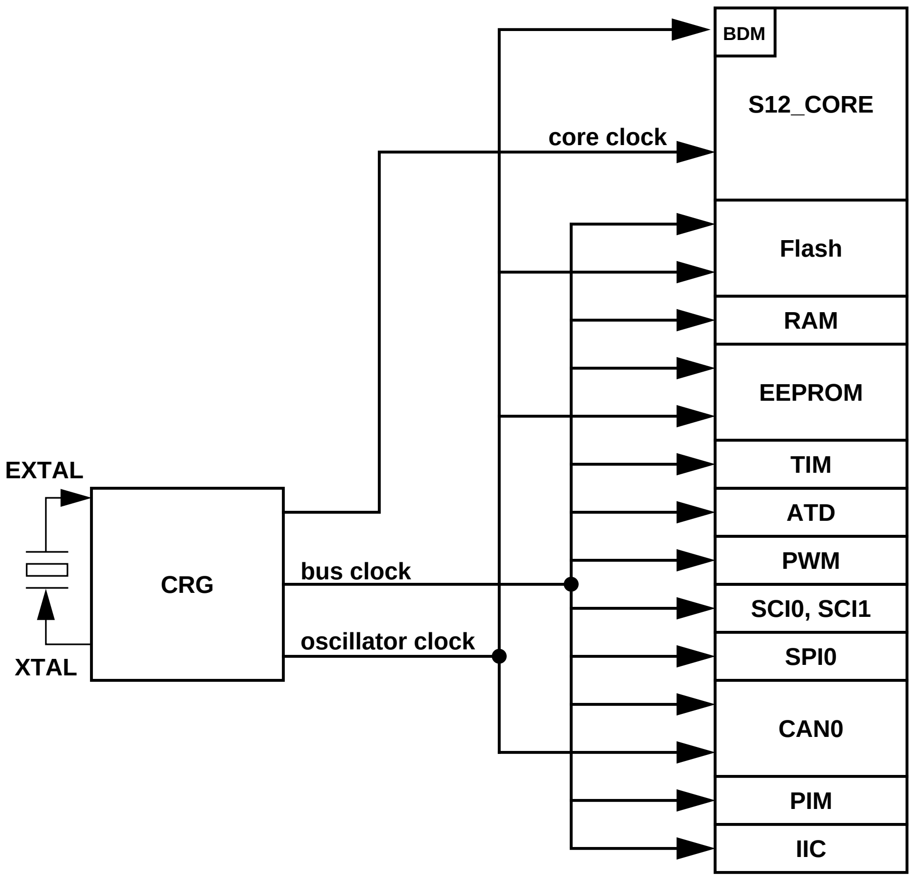


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12B128. Each mode has an associated default memory map and external bus configuration.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PK7 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	0	1	Emulation Expanded Narrow, BDM allowed
			1	0	
0	1	0	X	0	Special Test (Expanded Wide), BDM allowed
0	1	1	0	1	Emulation Expanded Wide, BDM allowed
			1	0	
1	0	0	X	1	Normal Single Chip, BDM allowed
1	0	1	0	0	Normal Expanded Narrow, BDM allowed
			1	1	
1	1	0	X	1	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal Expanded Wide, BDM allowed
			1	1	

For further explanation on the modes refer to the Core User Guide.

Table 4-2 Clock Selection Based on PE7

PE7 = $\overline{XCLKS}$	Description
1	Colpitts Oscillator selected

Table 4-2 Clock Selection Based on PE7

PE7 = $\overline{XCLKS}$	Description
0	Pierce Oscillator/external clock selected

Table 4-3 Voltage Regulator VREGEN

VREGEN	Description
1	Internal Voltage Regulator enabled
0	Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode or via a sequence of BDM commands. Unsecuring is also possible via the Backdoor Key Access. Refer to Flash Block Guide for details.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source)	None	None	–
$FFFC, $FFFD	Clock Monitor fail reset	None	PLLCTL (CME, SCME)	–
$FFFA, $FFFB	COP failure reset	None	COP rate select	–
$FFF8, $FFF9	Unimplemented instruction trap	None	None	–
$FFF6, $FFF7	SWI	None	None	–
$FFF4, $FFF5	XIRQ	X-Bit	None	–
$FFF2, $FFF3	IRQ	I-Bit	IRQCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	$F0
$FFEE, $FFEF	Standard Timer channel 0	I-Bit	TIE (C0I)	$EE
$FFEC, $FFED	Standard Timer channel 1	I-Bit	TIE (C1I)	$EC
$FFEA, $FFEB	Standard Timer channel 2	I-Bit	TIE (C2I)	$EA
$FFE8, $FFE9	Standard Timer channel 3	I-Bit	TIE (C3I)	$E8
$FFE6, $FFE7	Standard Timer channel 4	I-Bit	TIE (C4I)	$E6
$FFE4, $FFE5	Standard Timer channel 5	I-Bit	TIE (C5I)	$E4
$FFE2, $FFE3	Standard Timer channel 6	I-Bit	TIE (C6I)	$E2
$FFE0, $FFE1	Standard Timer channel 7	I-Bit	TIE (C7I)	$E0
$FFDE, $FFDF	Standard Timer overflow	I-Bit	TMSK2 (TOI)	$DE
$FFDC, $FFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	$DA
$FFD8, $FFD9	SPI0	I-Bit	SPICR1 (SPIE, SPTIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	ATD	I-Bit	ATDCTL2 (ASCIE)	$D2
$FFD0, $FFD1	Reserved	I-Bit	Reserved	$D0
$FFCE, $FFCF	Port J	I-Bit	PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0)	$CE

$FFCC, $FFCD	Port H	I-Bit	PIEH (PIEH7-0)	$CC
$FFCA, $FFCB	Reserved	I-Bit	Reserved	$CA
$FFC8, $FFC9		I-Bit		$C8
$FFC6, $FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	$C4
$FFC2, $FFC3	Reserved	I-Bit	Reserved	$C2
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBE, $FFBF	Reserved	I-Bit	Reserved	$BE
$FFBC, $FFBD		I-Bit		$BC
$FFBA, $FFBB	EEPROM	I-Bit	ECNFG (CCIE, CBEIE)	$BA
$FFB8, $FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	$B8
$FFB6, $FFB7	CAN0 wake-up	I-Bit	CANRIER (WUPIE)	$B6
$FFB4, $FFB5	CAN0 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$B4
$FFB2, $FFB3	CAN0 receive	I-Bit	CANRIER (RXFIE)	$B2
$FFB0, $FFB1	CAN0 transmit	I-Bit	CANTIER (TXEIE2-TXEIE0)	$B0
$FFAE, $FFAF	Reserved	I-Bit	Reserved	$AE
$FFAC, $FFAD		I-Bit		$AC
$FFAA, $FFAB		I-Bit		$AA
$FFA8, $FFA9		I-Bit		$A8
$FFA6, $FFA7		I-Bit		$A6
$FFA4, $FFA5		I-Bit		$A4
$FFA2, $FFA3		I-Bit		$A2
$FFA0, $FFA1		I-Bit		$A0
$FF9E, $FF9F		I-Bit		$9E
$FF9C, $FF9D		I-Bit		$9C
$FF9A, $FF9B		I-Bit		$9A
$FF98, $FF99		I-Bit		$98
$FF96, $FF97		I-Bit		$96
$FF94, $FF95		I-Bit		$94
$FF92, $FF93		I-Bit		$92
$FF90, $FF91		I-Bit		$90
$FF8E, $FF8F	Port P	I-Bit	PIEP (PIEP7-0)	$8E
$FF8C, $FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)	$8C
$FF8A, $FF8B	VREG LVI	I-Bit	CTRL0 (LVIE)	$8A
$FF80 to $FF89	Reserved			

5.3 Resets

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

For details on the different kind of resets refer to the HCS12 Core User Guide, CRG and VREG_3V3 Block User Guides.

5.3.1 I/O pins

Refer to the HCS12 Core User Guides for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

NOTE: *For devices assembled in 80-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to* **Table 2-1** *for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

5.4 Interrupts

For details on the different kind of interrupts refer to the HCS12 Core User Guide and according module Block User Guides.

Section 6 HCS12 Core Block Description

Consult the HCS12 Core User Guide for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), breakpoint module (BKP) and background debug mode module (BDM).

Table 6-1 shows the HCS12 configuration for MC9S12B128.

Table 6-1 Configuration of HCS12 Core on MC9S12B128

Name	Description	MC9S12B128 Configuration
PUCR_RESET	PUCR reset state	$90
NUM_INT	Interrupt Request Bus Width	56
INITEE_RST	INITEE reset state	$01
INITEE_WOK	INITEE Write anytime in normal mode	INITEE register is writeable once in normal modes
PPAGE_SMOD_ONLY	PPAGE Write only in special mode	PPAGE register is writable in allmodes, reset state of the PPAGE register is $00

6.1 Device-specific information

When the BDM section of S12 Core User Guide refers to *alternate clock* this is equivalent to *oscillator clock*.

Section 7 Voltage Regulator (VREG3V3) Block Description

Consult the VREG3V3 Block User Guide for information about the dual output linear voltage regulator. VREGEN is accessible externally.

Section 8 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

8.1 Device-specific information

The Low Voltage Reset feature of the CRG is available on this device.

Section 9 Oscillator (OSC) Block Description

Consult the OSC Block User Guide for information about the Oscillator module.

9.1 Device-specific information

The $\overline{XCLKS}$ input signal is active low (see **2.2.10 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 10 Standard Timer (TIM) Block Description

Consult the TIM_16B8C Block User Guide for information about the Standard Timer module. When the TIM_16B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 11 Analog to Digital Converter (ATD) Block Description

Consult the ATD_10B16C Block User Guide for information about the Analog to Digital Converter module. When the ATD_10B16C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*. The ETRIG pin option is not available.

Section 12 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 13 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12B128 device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 14 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block User Guide for information about the Serial Peripheral Interface module.

Section 15 Flash EEPROM 128K1 Block Description

Consult the FTS128K1 Block User Guide for information about the flash module.

Section 16 EEPROM 1K Block Description

Consult the EETS1K Block User Guide for information about the EEPROM module.

Section 17 RAM Block Description

This module supports single-cycle misaligned word accesses.

Section 18 MSCAN Block Description

Consult the MSCAN Block User Guide for information about the Motorola Scalable CAN Module.

Section 19 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 20 Port Integration Module (PIM) Block Description

Consult the PIM_9B128 Block User Guide for information about the Port Integration Module.

Section 21 Printed Circuit Board Layout Proposals

Table 21-1 Suggested External Component Values

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	100 .. 220nF
C2	VDD2 filter cap	ceramic X7R	100 .. 220nF
C3	VDDA filter cap	ceramic X7R	100nF
C4	VDDR filter cap	X7R/tantalum	>=100nF
C5	VDDPLL filter cap	ceramic X7R	100nF
C6	VDDX filter cap	X7R/tantalum	>=100nF
C7	OSC load cap	See PLL specification chapter	
C8	OSC load cap		
C9 / C_S	PLL loop filter cap	See PLL specification chapter	
C10 / C_P	PLL loop filter cap		
C11 / C_{DC}	DC cutoff cap	Colpitts mode only, if recommended by quartz manufacturer	
R1	PLL loop filter res	See PLL specification chapter	
R2 / R_B	OSC res	Pierce mode only	
R3 / R_S	OSC res		
Q1	Quartz		

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins(C1 - C6).
- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Figure 21-1 Recommended PCB Layout 112LQFP Colpitts Oscillator

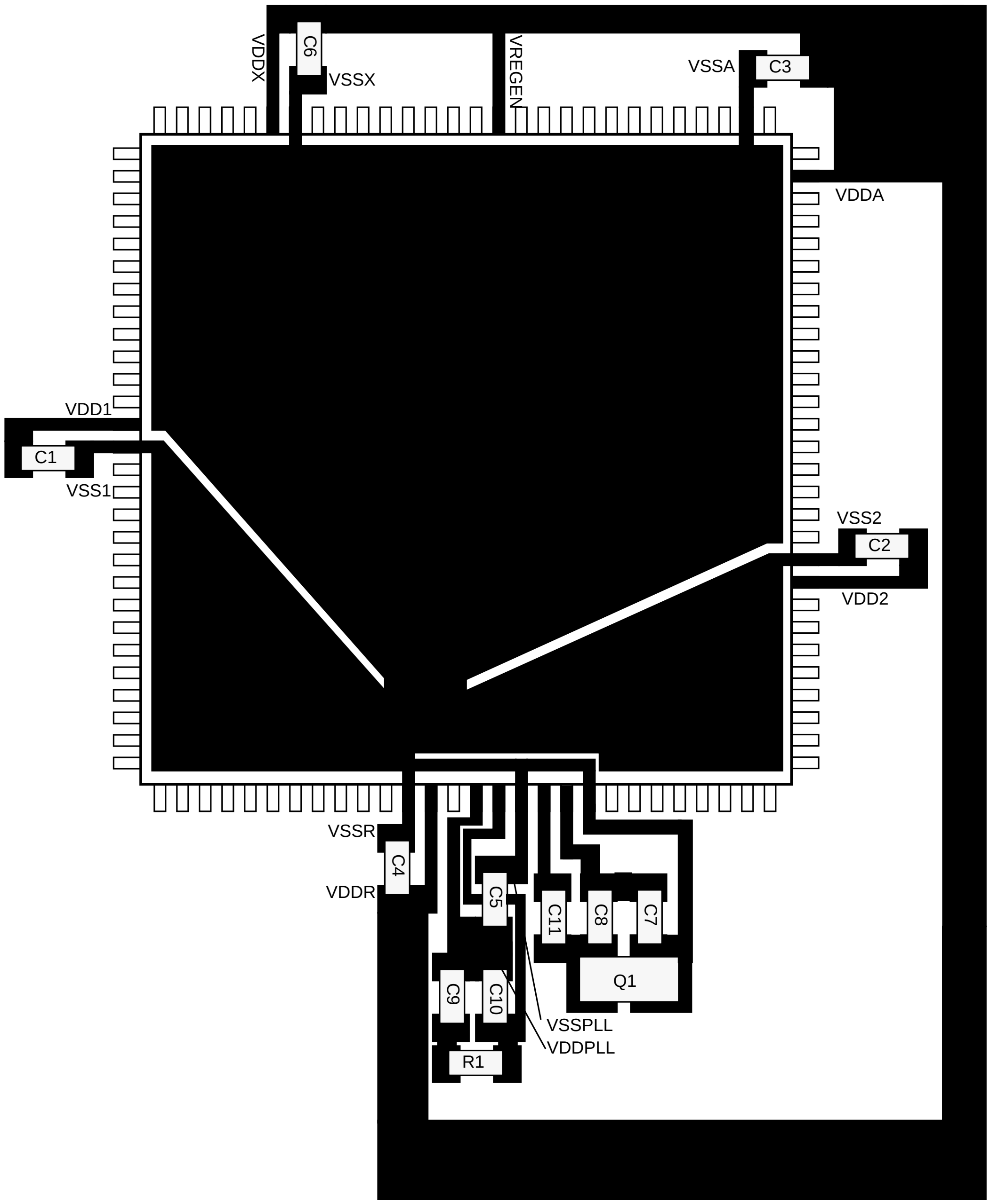


Figure 21-2 Recommended PCB Layout for 80QFP Colpitts Oscillator

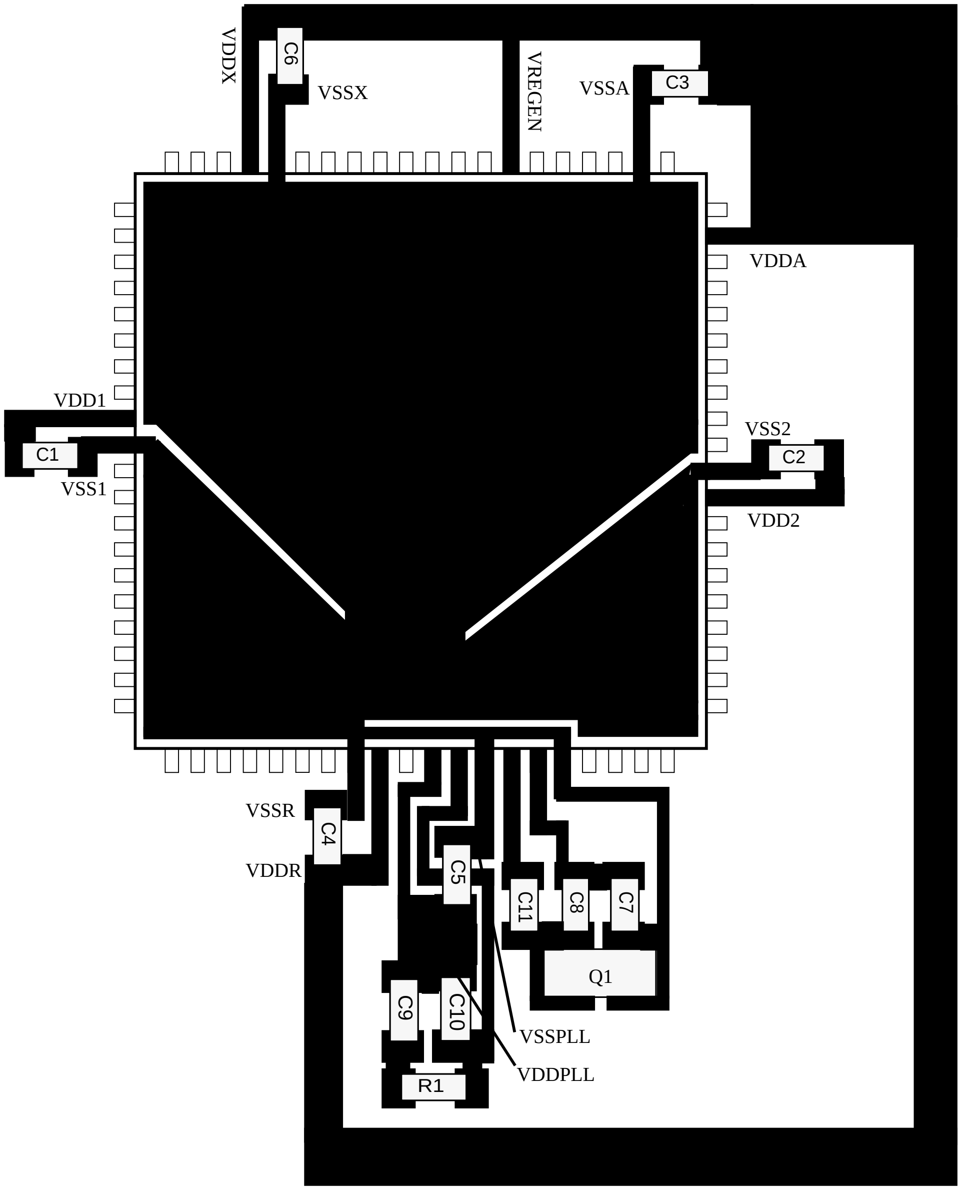


Figure 21-3 Recommended PCB Layout for 112LQFP Pierce Oscillator

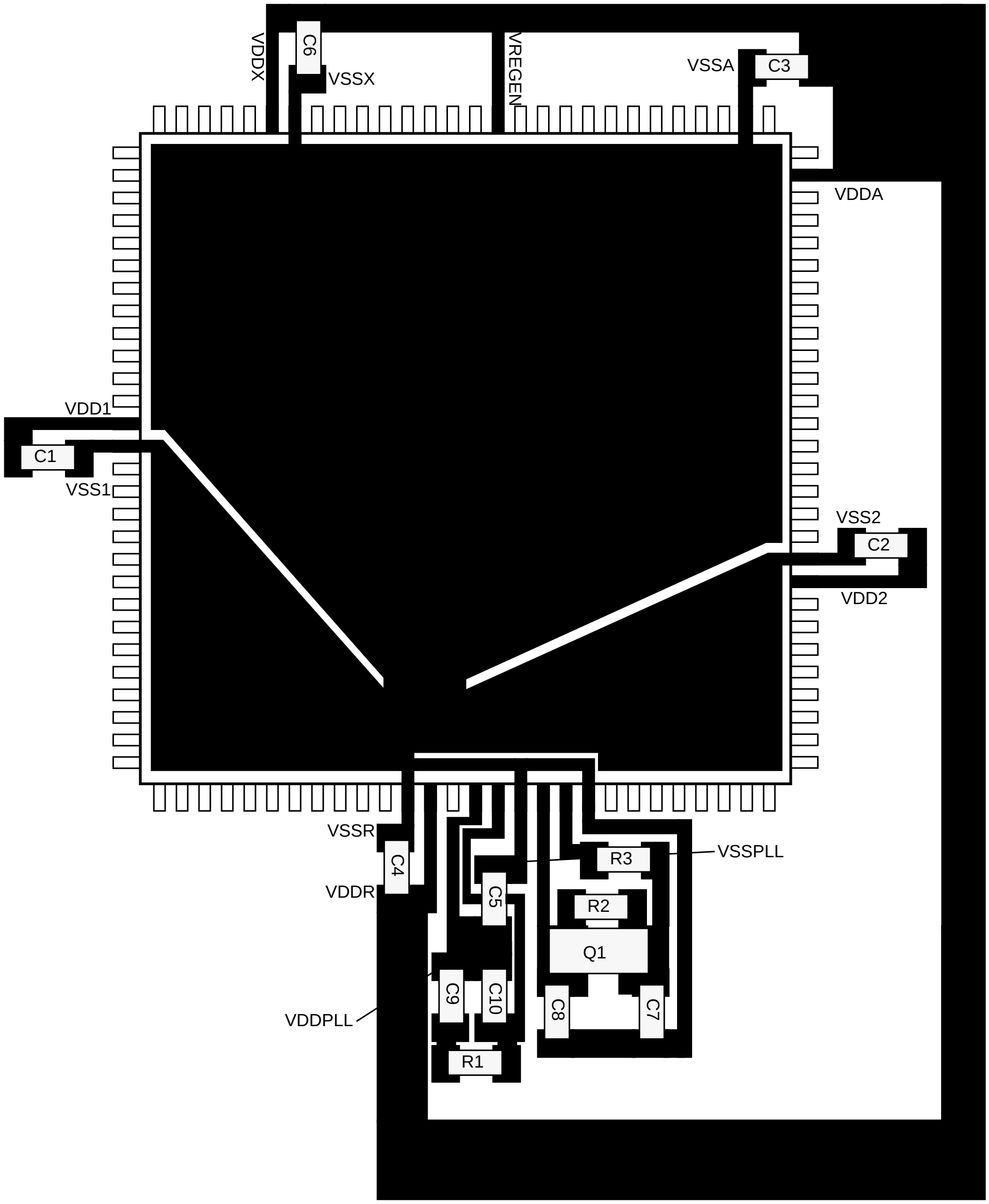
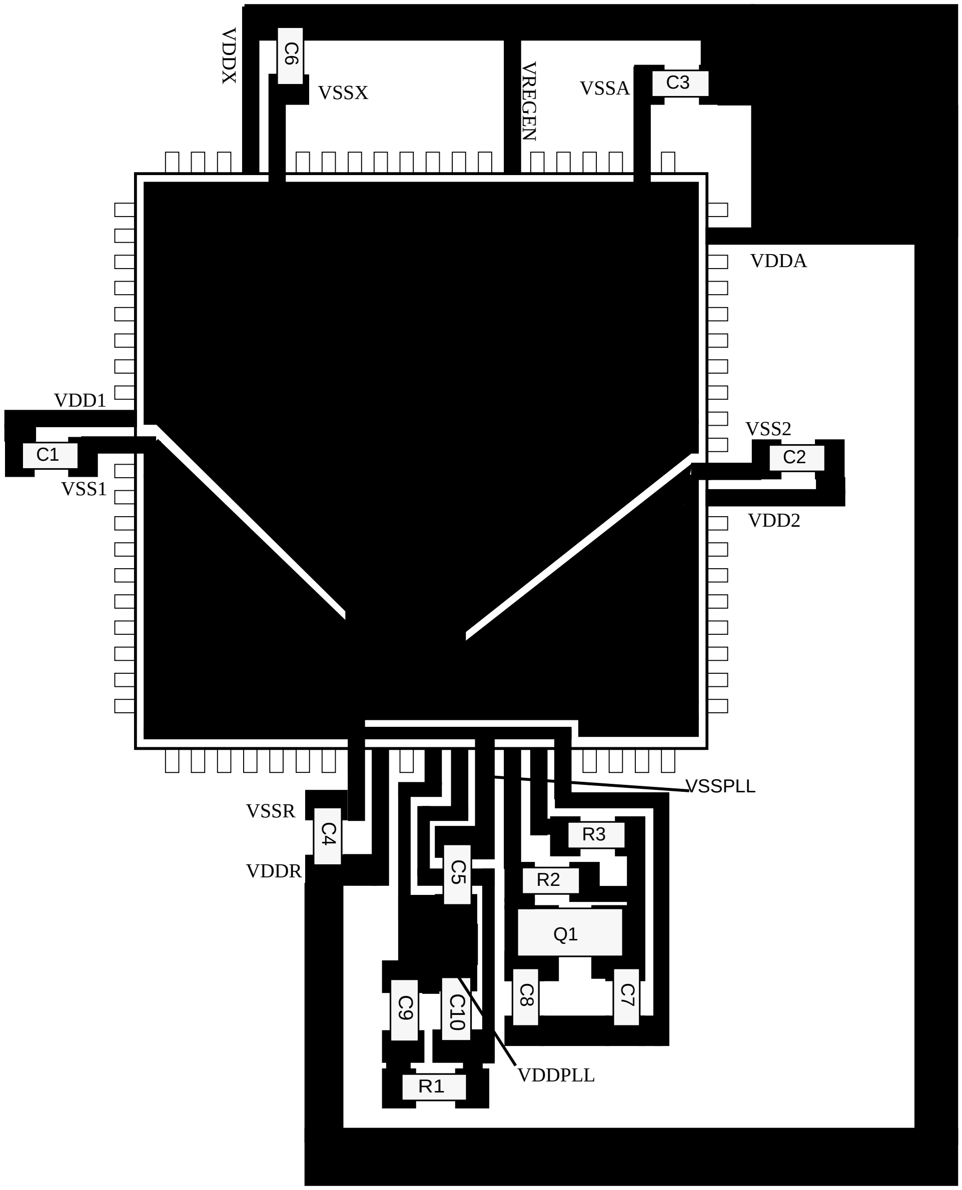


Figure 21-4 Recommended PCB Layout for 80QFP Pierce Oscillator



Appendix A Electrical Characteristics

A.1 General

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Motorola and are subject to change without notice.*

NOTE: *The part is specified and tested over the 5V and 3.3V ranges. For the intermediate range, generally the electrical specifications for the 3.3V range apply, but the part is not tested in production test in the intermediate range.*

This supplement contains the most accurate electrical information for the MC9S12B128 microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE: *This classification is shown in the column labeled “C” in the parameter tables where appropriate.*

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12B128 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the digital core.

The VDDA, VSSA pair supplies the A/D converter and the internal voltage regulator.

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.*
IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.
VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.
IDD is used for the sum of the currents flowing into VDD1 and VDD2.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.5	V
2	Digital Logic Supply Voltage [2]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.5	V
7	Analog Reference	$V_{RH,}$ V_{RL}	-0.3	6.5	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [3]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[4]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST [5]	I_{DT}	-0.25	0	mA
15	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. Beyond absolute maximum ratings device might be damaged.
2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.
4. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.
5. This pin is clamped low to V_{SSPLL}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit

Table A-2 ESD and Latch-up Test Conditions

Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	T	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	T	Machine Model (MM)	V_{MM}	200	-	V
3	T	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	T	Latch-up Current at T_A = 125°C positive negative	I_{LAT}	+100 -100	-	mA
5	T	Latch-up Current at T_A = 27°C positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to **Section A.1.8 Power Dissipation and Thermal Characteristics**.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	2.97	5	5.5	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V

Table A-4 Operating Conditions

PLL Supply Voltage [1]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator	f_{osc}	0.5	-	16	MHz
Bus Frequency	f_{bus}	0.25[2]	-	25[3]	MHz
MC9S12B128**C** Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range [4]	T_A	-40	27	85	°C
MC9S12B128**V** Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range [4]	T_A	-40	27	105	°C
MC9S12B128**M** Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range [4]	T_A	-40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. This applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.
3. See bus speed option at **Table 0-1 Derivative Differences**
4. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^{2}$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}};\text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}};\text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-8** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^{2}$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	$^oC/W$
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	$^oC/W$
3	T	Junction to Board LQFP112	θ_{JB}	–	–	31	$^oC/W$
4	T	Junction to Case LQFP112	θ_{JC}	–	–	11	$^oC/W$
5	T	Junction to Package Top LQFP112	Ψ_{JT}	–	–	2	$^oC/W$
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	–	–	51	$^oC/W$
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	–	–	41	$^oC/W$
8	T	Junction to Board QFP80	θ_{JB}	–	–	27	$^oC/W$
9	T	Junction to Case QFP80	θ_{JC}	–	–	14	$^oC/W$
10	T	Junction to Package Top QFP80	Ψ_{JT}	–	–	3	$^oC/W$

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 5V I/O Characteristics

Conditions are 4.5< VDDX <5.5V Termperature from -40¯C to +140¯C, unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	-	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} - 0.3	-	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high impedance input mode) V_{in} = V_{DD5} or V_{SS5}	I_{in}	–1	-	1	µA
5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2mA Full Drive I_{OH} = –10mA	V_{OH}	V_{DD5} – 0.8	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +2mA Full Drive I_{OL} = +10mA	V_{OL}	-	-	0.8	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	–130	µA
8	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	µA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	µA
10	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	µA
11	D	Input Capacitance	C_{in}		7	-	pF
12	T	Injection current[1] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered[2]	t_{pign}			3	µs
14	P	Port H, J, P Interrupt Input Pulse passed[2]	t_{pval}	10			µs

NOTES:

1. Refer to **Section A.1.4 Current Injection**, for more details
2. Parameter only applies in STOP or Pseudo STOP mode.

Table A-7 3.3V I/O Characteristics

Conditions are VDDX=3.3V +/-10% Termperature from -40¯C to +140¯C, unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	-	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} - 0.3	-	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high impedance input mode) V_{in} = V_{DD5} or V_{SS5}	I_{in}	–1	-	1	µA
5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –0.75mA Full Drive I_{OH} = –4.5mA	V_{OH}	V_{DD5} – 0.4	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +0.9mA Full Drive I_{OL} = +5.5mA	V_{OL}	-	-	0.4	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	–60	µA
8	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-6	-	-	µA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	60	µA
10	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	6	-	-	µA
11	D	Input Capacitance	C_{in}		7	-	pF
12	T	Injection current[1] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered[2]	t_{pign}			3	µs
14	P	Port H, J, P Interrupt Input Pulse passed[2]	t_{pval}	10			µs

NOTES:
1. Refer to **Section A.1.4 Current Injection**, for more details
2. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz or 16Mhz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-8 Supply Current Characteristics at 25MHz Bus Frequency

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			55	mA
2	 P P	Wait Supply current All modules enabled, PLL on only RTI enabled [1]	I_{DDW}			 35 7	mA
3	 C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) [1, 2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		 370 400 450 550 600 650 800 850 1200	 500 1600 2100 5000	µA
4	 C C C C C C C	Pseudo Stop Current (RTI and COP enabled) [1, 2] -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		 570 600 650 750 850 1200 1500		µA
5	 C P C C P C P C P	Stop Current [2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		 12 25 100 130 160 200 350 400 600	 100 1200 1700 5000	µA

NOTES:
1. PLL off
2. At those low power dissipation levels $T_J = T_A$ can be assumed

Table A-9 Supply Current Characteristics at 16MHz Bus Frequency

Num	C	Rating	Symbol	Min	Typ	Max	Unit
Conditions are shown in **Table A-4** unless otherwise noted							
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			55	mA
2	 P P	Wait Supply current All modules enabled, PLL on only RTI enabled [1]	I_{DDW}			 35 7	mA
3	 C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) [1, 2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		 370 400 450 550 600 650 800 850 1200	 500 1600 2100 5000	µA
4	 C C C C C C C	Pseudo Stop Current (RTI and COP enabled) [1, 2] -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		 570 600 650 750 850 1200 1500		µA
5	 C P C C P C P C P	Stop Current [2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		 12 25 100 130 160 200 350 400 600	 100 1200 1700 5000	µA

NOTES:
1. PLL off
2. At those low power dissipation levels $T_J = T_A$ can be assumed

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

The ATD is specified and tested for both the 3.3V and 5V range. For ranges between 3.3V and 5V the ATD accuracy is generally the same as in the 3.3V range but is not tested in this range in production test.

A.2.1 ATD Operating Characteristics In 5V Range

The **Table A-10** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-10 ATD Operating Characteristics In 5V Range

Conditions are shown in **Table A-4** unless otherwise noted. Supply Voltage 5V-10% <= V_{DDA} <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	$V_{RH}-V_{RL}$	4.75	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=5.0 Volts)	t_{REC}			20	µs
7	P	Reference Supply current	I_{REF}			0.750	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.75V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 ATD Operating Characteristics In 3.3V Range

The **Table A-11** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive

beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-11 ATD Operating Characteristics In 3.3V Range

Conditions are shown in **Table A-4** unless otherwise noted. Supply Voltage 3.3V-10% <= V_{DDA} <= 3.3V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}-V_{RL}	3.0	3.3	3.6	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=3.3 Volts)	t_{REC}			20	µs
7	P	Reference Supply current	I_{REF}			0.500	mA

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 3.0V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.3 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.3.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.3.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.3.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-12 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input Source Resistance	R_S	-	-	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

A.2.4 ATD accuracy

A.2.4.1 5V Range

Table A-13 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-13 ATD Conversion Performance In 5V Range

Conditions are shown in **Table A-4** unless otherwise noted
$V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV
$f_{ATDCLK} = 2.0MHz$
Supply Voltage 5V-10% <= V_{DDA} <=5V+10%

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB		20		mV
6	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error[1]	AE	-1.5	±1.0	1.5	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

A.2.4.2 3.3V Range

Table A-14 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-14 ATD Conversion Performance In 3.3V Range

Conditions are shown in **Table A-4** unless otherwise noted
$V_{REF} = V_{RH} - V_{RL} = 3.328V$. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV
$f_{ATDCLK} = 2.0MHz$
Supply Voltage 3.3V-10% <= V_{DDA} <= 3.3V+10%

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		3.25		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1.5		1.5	Counts
3	P	10-Bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-5	±2.5	5	Counts
5	P	8-Bit Resolution	LSB		13		mV
6	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	–1.5	±1.0	1.5	Counts
8	P	8-Bit Absolute Error[1]	AE	-2.0	±1.5	2.0	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

A.2.4.3 ATD Accuracy Definitions

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

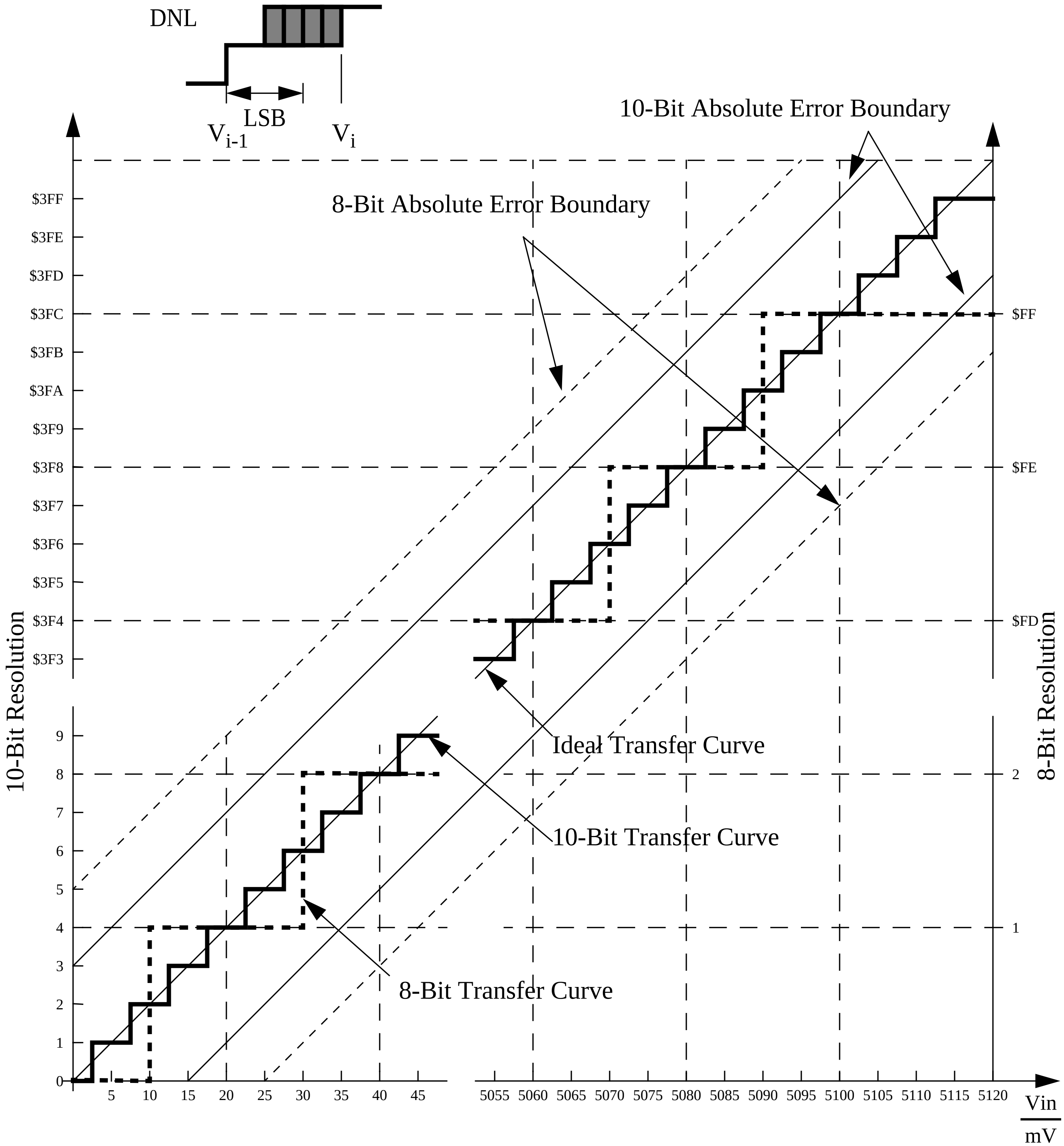


Figure A-1 ATD Accuracy Definitions

NOTE: ***Figure A-1*** *shows only definitions, for specification values refer to* ***Table A-13****.*

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-15** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Row Programming

This applies only to the Flash where up to 64 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 63 \cdot t_{bwpgm}$$

Row programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 1024 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-15 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	μs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	μs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	678.4 [2]		1035.5 [3]	μs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		32778 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]		2058[7]	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **A.3.1.1 - A.3.1.4** for guidance.
4. Burst Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6. Minimum time, if first word in the array is not blank
7. Maximum time to complete check on an erased block

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table A-16 NVM Reliability Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Data Retention at an average junction temperature of T_{Javg} = 70°C	t_{NVMRET}	15			Years
2	C	Flash number of Program/Erase cycles	n_{FLPE}	10,000			Cycles
3	C	EEPROM number of Program/Erase cycles (–40°C $\leq T_J \leq$ 0°C)	n_{EEPE}	10,000			Cycles
4	C	EEPROM number of Program/Erase cycles (0°C < $T_J \leq$ 140°C)	n_{EEPE}	100,000			Cycles

A.4 VREG_3V3

A.4.1 Operating Conditions

Table A-17 VREG_3V3 - Operating Conditions

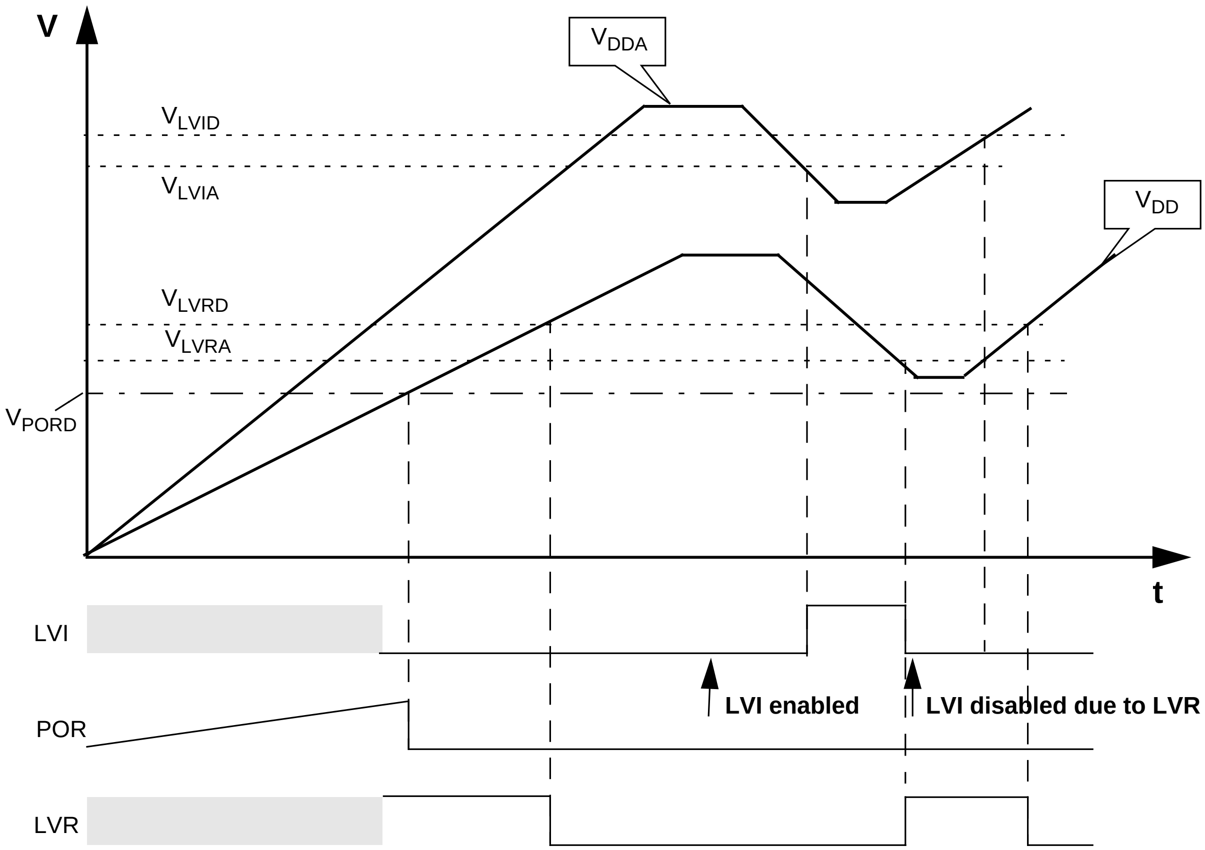
Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
1	P	Input Voltages	$V_{VDDR,A}$	2.97	—	5.5	V
2	P	Regulator Current Reduced Power Mode Shutdown Mode	I_{REG}	— —	20 12	50 40	µA µA
3	P	Output Voltage Core Full Performance Mode Reduced Power Mode Shutdown Mode	V_{DD}	2.35 1.6 —	2.5 2.5 —[1]	2.75 2.75 —	V V V
4	P	Output Voltage PLL Full Performance Mode Reduced Power Mode[2] Reduced Power Mode[3] Shutdown Mode	V_{DDPLL}	2.35 2.0 1.6 —	2.5 2.5 2.5 —[4]	2.75 2.75 2.75 —	V V V
7	P	Low Voltage Interrupt[5] Assert Level Deassert Level	V_{LVIA} V_{LVID}	4.1 4.25	4.37 4.52	4.66 4.77	V V
8	P	Low Voltage Reset[6] Assert Level	V_{LVRA}	2.25	—	—	V
9	C	Power-on Reset[7] Assert Level Deassert Level	V_{PORA} V_{PORD}	0.97 —	— —	— 2.05	V V

NOTES:
1. High Impedance Output
2. Current IDDPLL = 1mA (Colpitts Oscillator)
3. Current IDDPLL = 3mA (Pierce Oscillator)
4. High Impedance Output
5. Monitors V_{DDA}, active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.
6. Monitors V_{DD}, active only in Full Performance Mode. MCU is monitored by the POR in RPM (see **Figure A-2**)
7. Monitors V_{DD}. Active in all modes.

A.4.2 Chip Power-up and Voltage Drops

VREG_3V3 sub modules LVI (low voltage interrupt), POR (power-on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is described in **Figure A-2**.

Figure A-2 VREG_3V3 - Chip Power-up and Voltage Drops (not scaled)



A.4.3 Output Loads

A.4.3.1 Resistive Loads

On-chip voltage regulator VREG_3V3 intended to supply the internal logic and oscillator circuits allows no external DC loads.

A.4.3.2 Capacitive Loads

The capacitive loads are specified in **Table A-18**. Ceramic capacitors with X7R dielectricum are required.

Table A-18 VREG_3V3 - Capacitive Loads

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	VDD external capacitive load	C_{DDext}	200	440	12000	nF
3	VDDPLL external capacitive load	$C_{DDPLLext}$	90	220	5000	nF

A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

Table A-19 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-19 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
2	D	Startup from Reset	n_{RST}	192		196	n_{osc}
3	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
4	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.5.1.1 POR

The release level V_{PORD} (see **Table A-17**) and the assert level V_{PORA} (see **Table A-17**) are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.5.1.2 LVR

The assert level V_{LVRA} (see **Table A-17**) is derived from the V_{DD} Supply. After releasing the LVR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.5.1.3 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.5.1.4 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.5 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.5.1.6 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset.By asserting the $\overline{XCLKS}$ input during reset this oscillator can be bypassed allowing the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-20 Oscillator Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5		16	MHz
1b	C	Crystal oscillator range (Pierce) [1]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			µA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}		8[2]	100[3]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [4]	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high	t_{EXTH}	9.5			ns
9	D	External square wave rise time	t_{EXTR}			1	ns
10	D	External square wave fall time	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V

NOTES:
1. Depending on the crystal a damping series resistor might be necessary

2. f_{osc} = 4MHz, C = 22pF.
3. Maximum value is for extreme cases using high Q, low frequency crystals
4. $\overline{XCLKS}$ =0 during reset

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

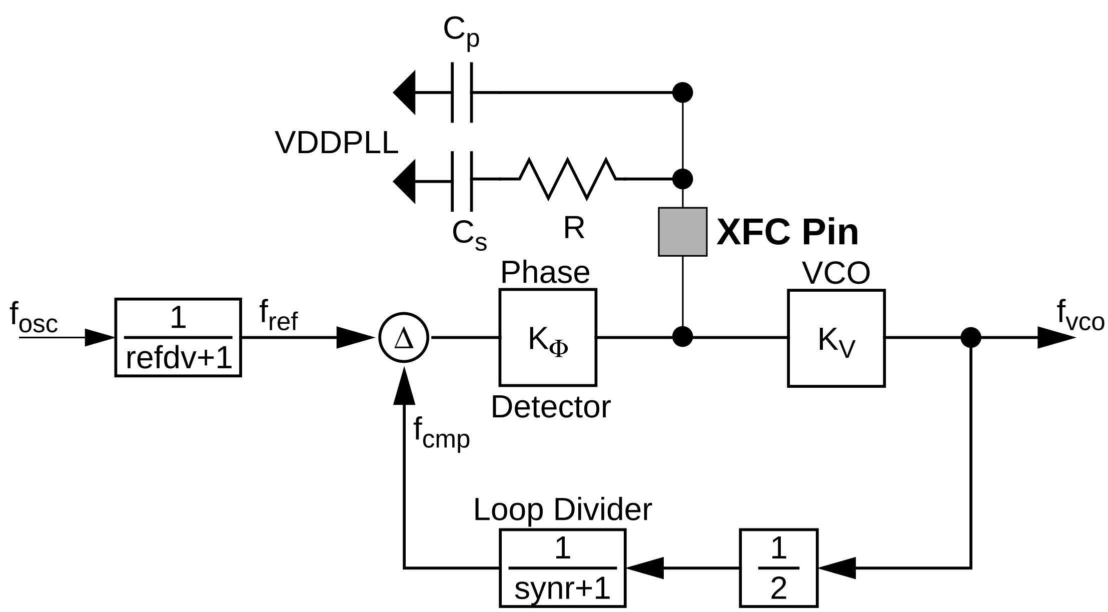


Figure A-3 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-21**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V \qquad = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by <u>at least</u> a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10};(\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) \qquad = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C=10kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \qquad = 2*\pi*50*10\text{kHz}/(316.7\text{Hz}/\Omega)=9.9\text{k}\Omega=\sim 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R};(\zeta = 0.9) \qquad = 5.19\text{nF} =\sim 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \le C_p \le C_s/10 \qquad C_p = 470\text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-3**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-4**.

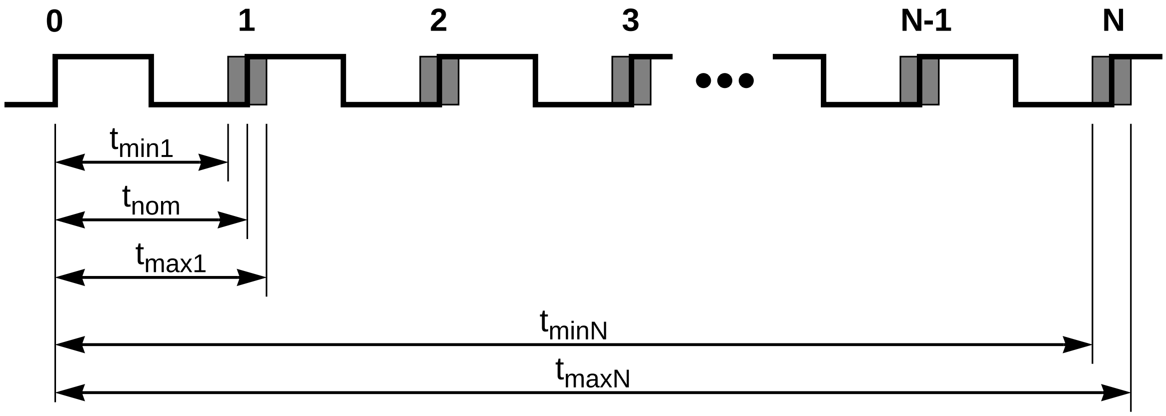


Figure A-4 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

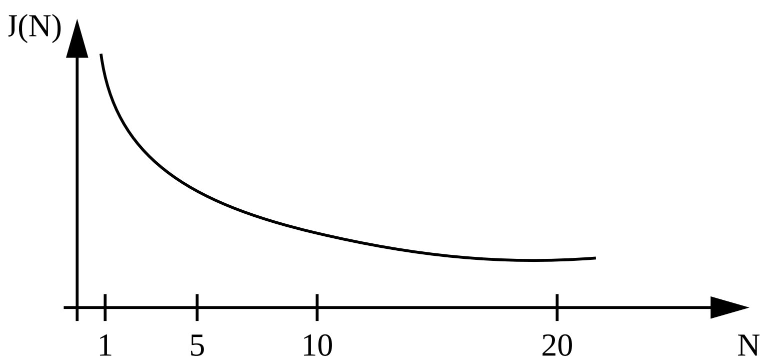


Figure A-5 Maximum bus clock jitter approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-21 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[(1)]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[(1)]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[(1)]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [(2)]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [(2)]	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		-100		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		60		MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$		38.5		µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$		3.5		µA
14	C	Jitter fit parameter 1[(2)]	j_1			1.1	%
15	C	Jitter fit parameter 2[(2)]	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{OSC} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

A.6 MSCAN

Table A-22 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	μs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			μs

A.7 SPI

This section provides electrical parametrics and ratings for the SPI.

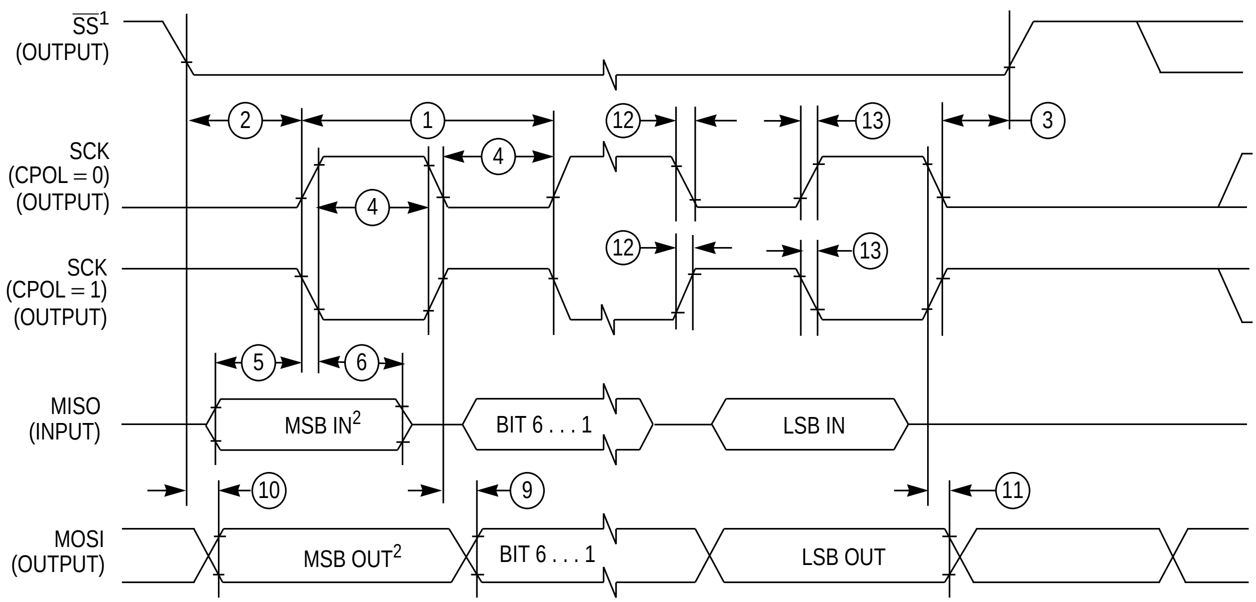
In **Table A-23** the measurement conditions are listed.

Table A-23 Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance $C_{LOAD,}$ on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) VDDX	V

A.7.1 Master Mode

In **Figure A-6** the timing diagram for master mode with transmission format CPHA=0 is depicted.

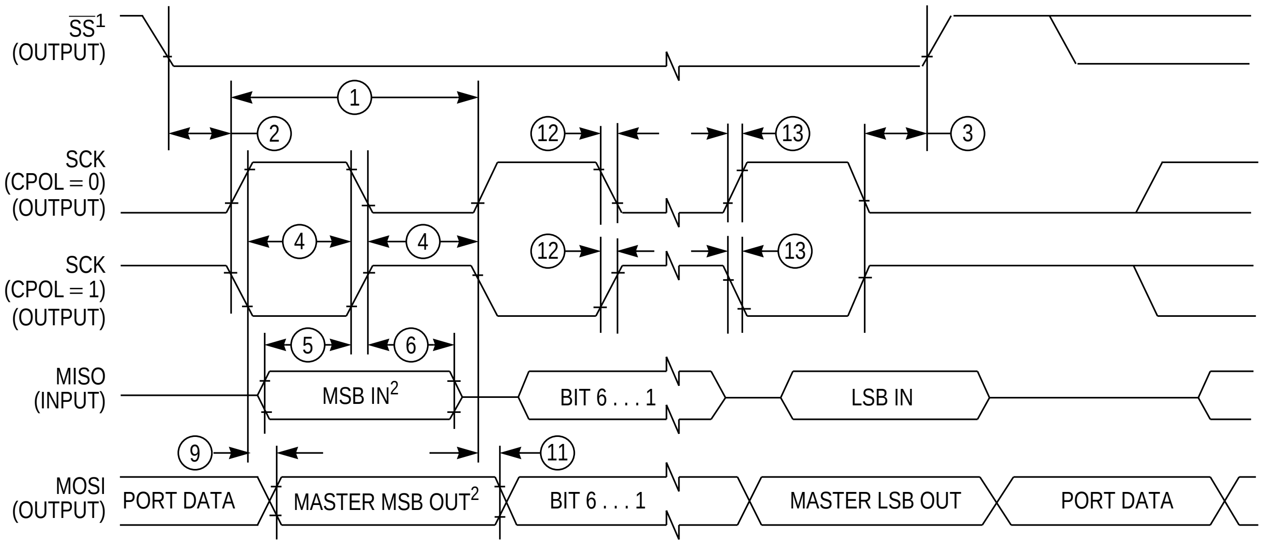


1.if configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6 SPI Master Timing (CPHA=0)

In **Figure A-7** the timing diagram for master mode with transmission format CPHA=1 is depicted.



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-7 SPI Master Timing (CPHA=1)

In **Table A-24** the timing characteristics for master mode are listed.

Table A-24 SPI Master Mode Timing Characteristics

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3	Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	30	ns
10	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

A.7.2 Slave Mode

In **Figure A-8** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

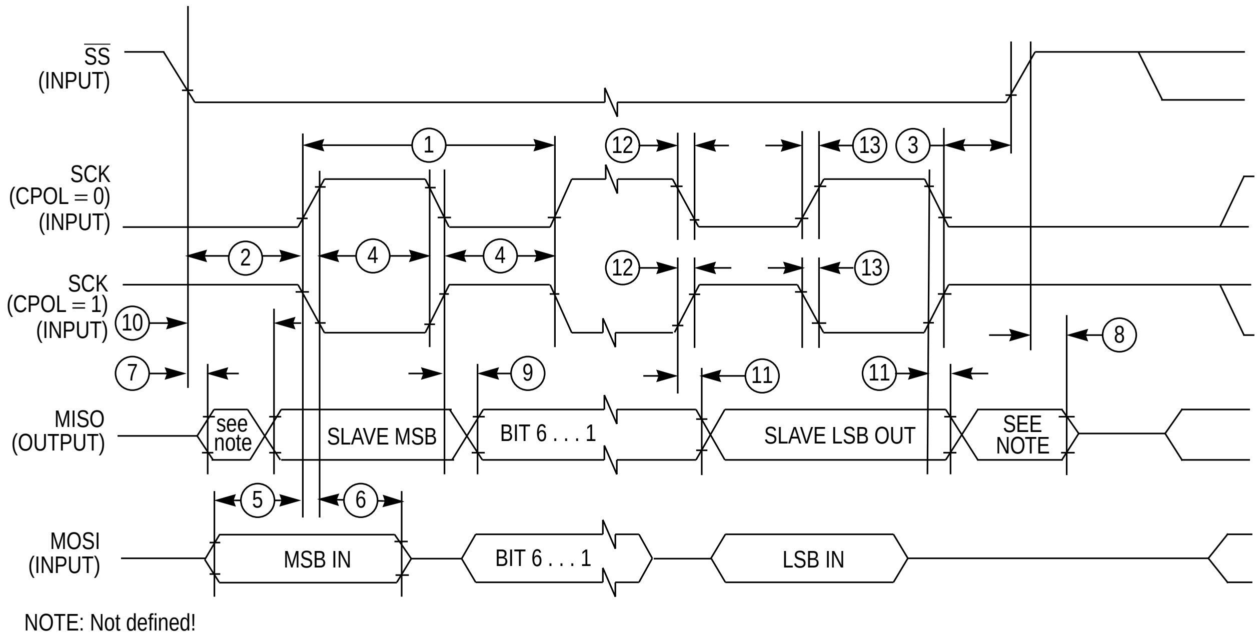


Figure A-8 SPI Slave Timing (CPHA=0)

In **Figure A-9** the timing diagram for slave mode with transmission format CPHA=1 is depicted.

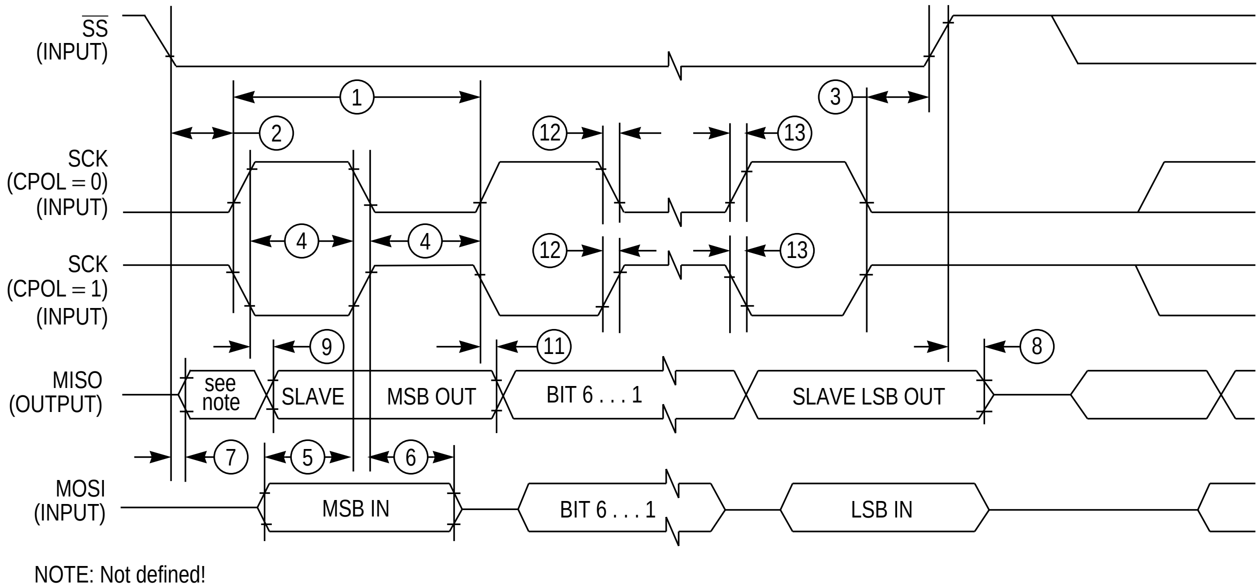


Figure A-9 SPI Slave Timing (CPHA=1)

In **Table A-25** the timing characteristics for slave mode are listed.

Table A-25 SPI Slave Mode Timing Characteristics

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	Slave Access Time (time to data active)	t_a	—	—	20	ns
8	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	30 + t_{bus} [1]	ns
10	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	30 + t_{bus} [1]	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

NOTES:
1. t_{bus} added due to internal synchronization delay

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-10** with the actual timing values shown on **Table A-26** in 5V range. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

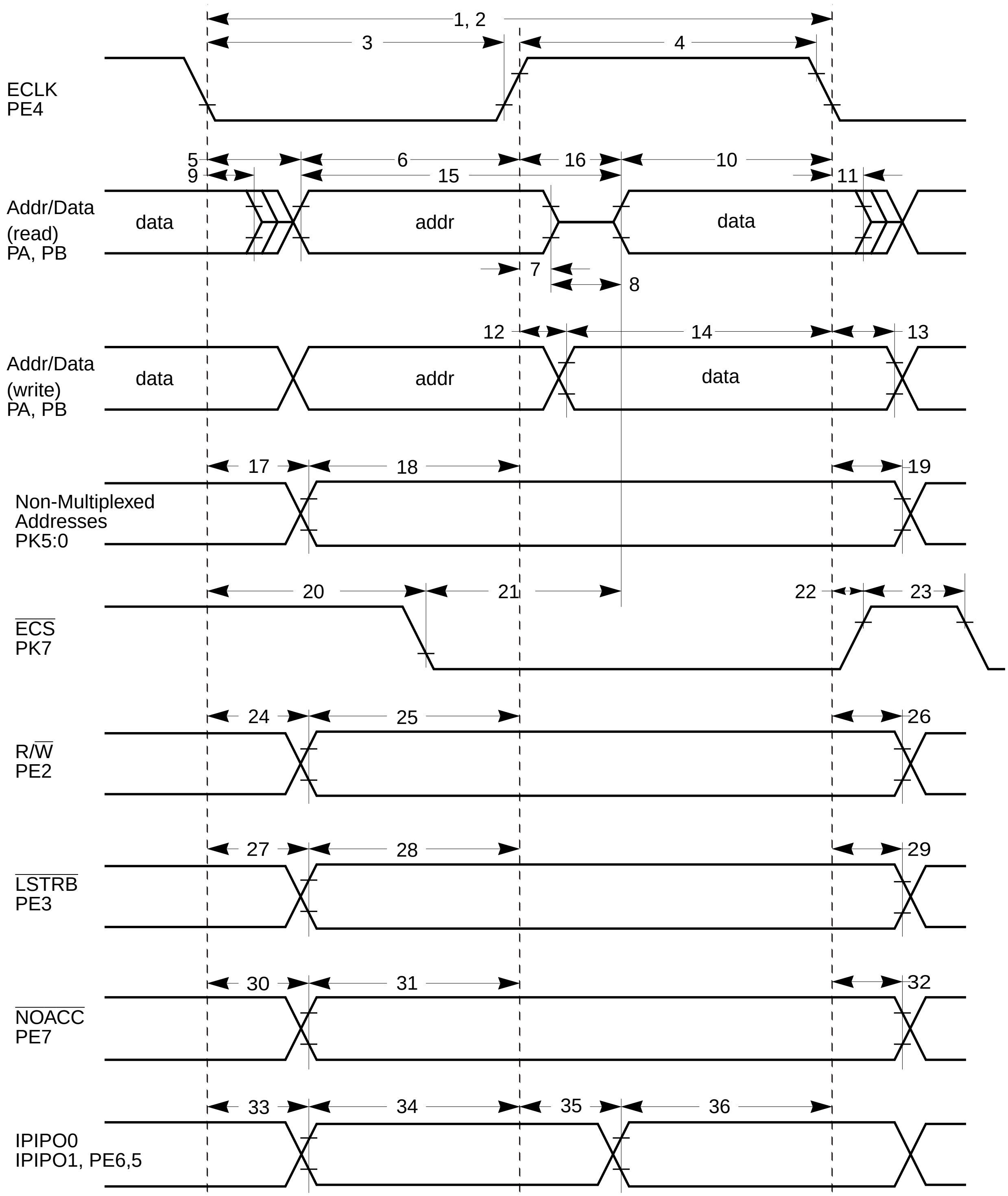


Figure A-10 General External Bus Timing

Table A-26 Expanded Bus Timing Characteristics In 5V Range

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF. Supply Voltage 5V-10% <= V_{DDX} <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time[1] (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time[1] (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time[1] (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Chip select delay time	t_{CSD}			16	ns
18	D	Chip select access time[1] (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
19	D	Chip select hold time	t_{CSH}	2			ns
20	D	Chip select negated time	t_{CSN}	8			ns
21	D	Read/write delay time	t_{RWD}			7	ns
22	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
23	D	Read/write hold time	t_{RWH}	2			ns
24	D	Low strobe delay time	t_{LSD}			7	ns
25	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
26	D	Low strobe hold time	t_{LSH}	2			ns
27	D	NOACC strobe delay time	t_{NOD}			7	ns
28	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns
29	D	NOACC hold time	t_{NOH}	2			ns
30	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns

Table A-26 Expanded Bus Timing Characteristics In 5V Range

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF. Supply Voltage 5V-10% <= V_{DDX} <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
31	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	11			ns
32	D	IPIPO[1:0] delay time[1] (PW_{EH}-t_{P1V})	t_{P1D}	2		25	ns
33	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

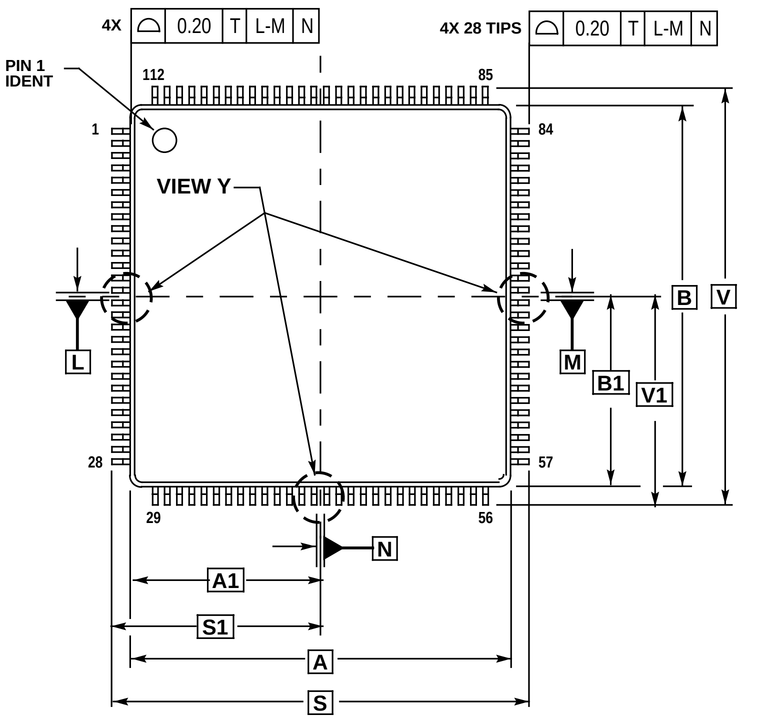
NOTES:
1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

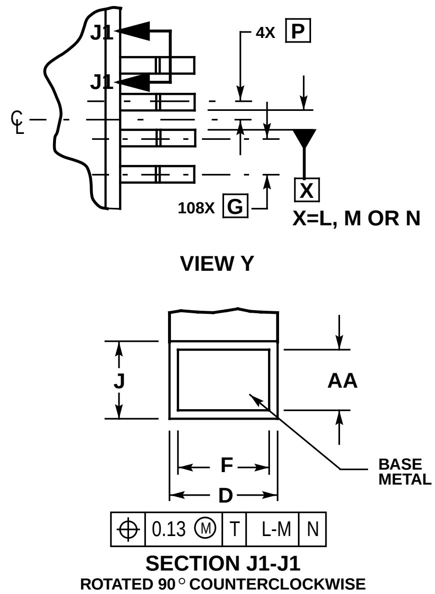
Appendix B Package Information

B.1 General

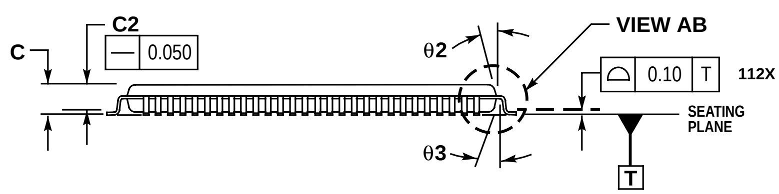
This section provides the physical dimensions of the MC9S12B128 packages.

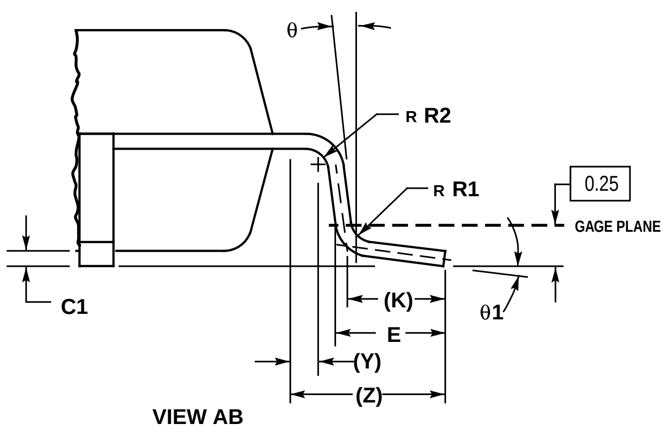
B.2 112-pin LQFP package





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

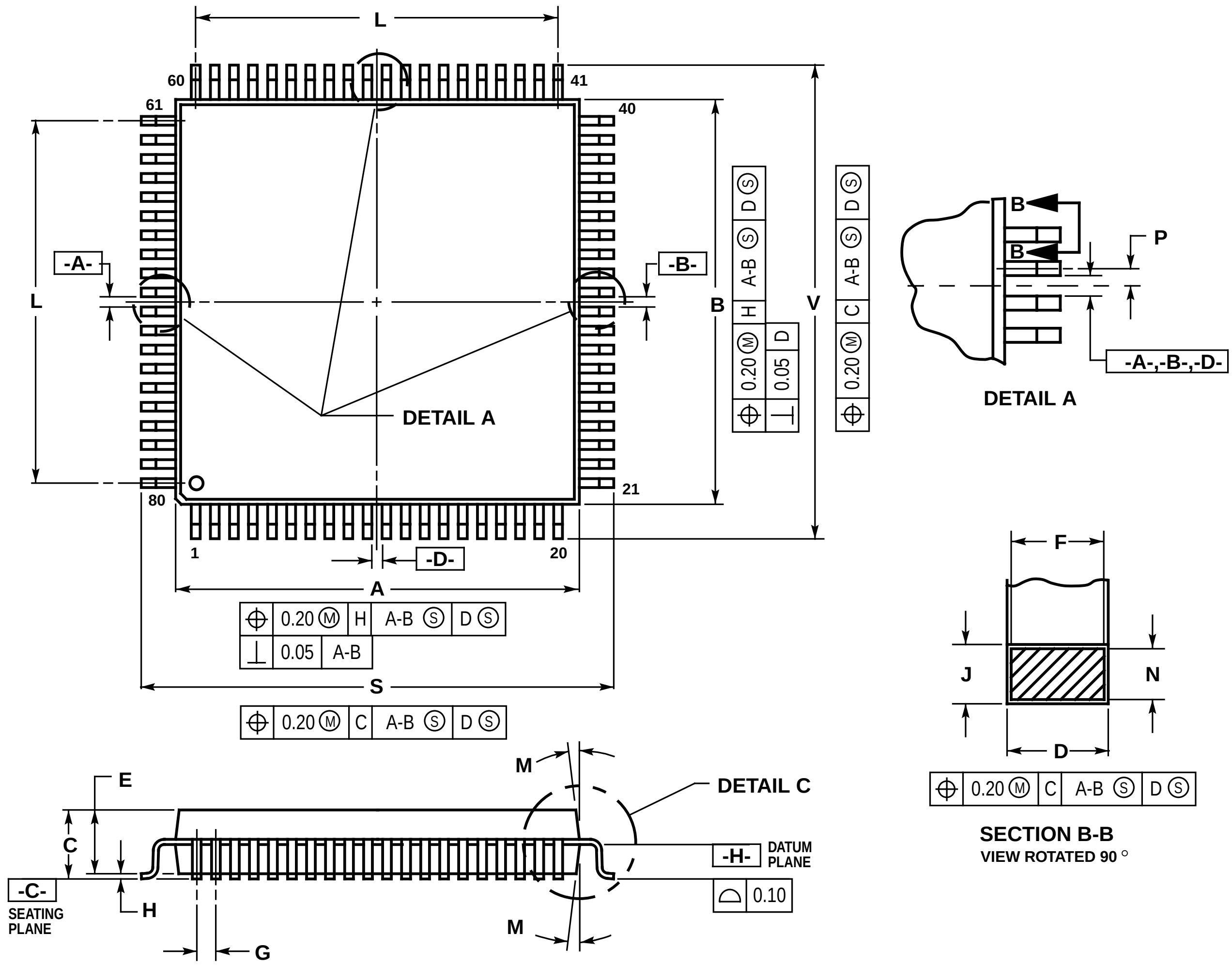


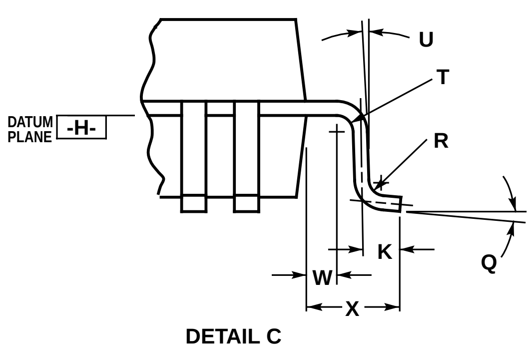


DIM	MILLIMETERS	
	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)

B.3 80-pin QFP package





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5 °	10 °
N	0.13	0.17
P	0.325 BSC	
Q	0 °	7 °
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0 °	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure B-2 80-pin QFP Mechanical Dimensions (case no. 841B)

Device User Guide End Sheet

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