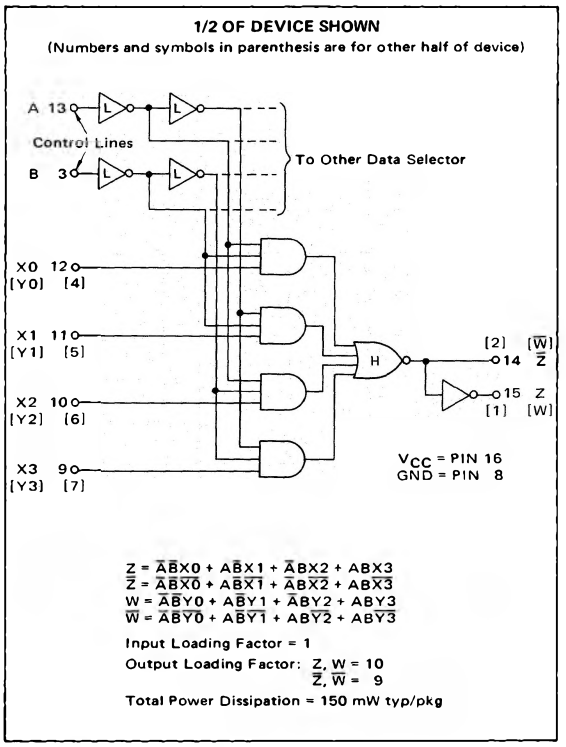
DUAL 4-CHANNEL
DATA SELECTOR

MC9309L*
MC8309L,P*



This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR-INVERT gates with active pullup outputs, and low-level inverters on the control inputs. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the complementary outputs.

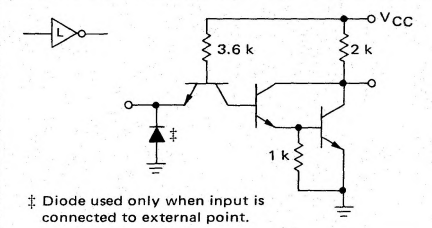
Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

The MC9309/8309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss.

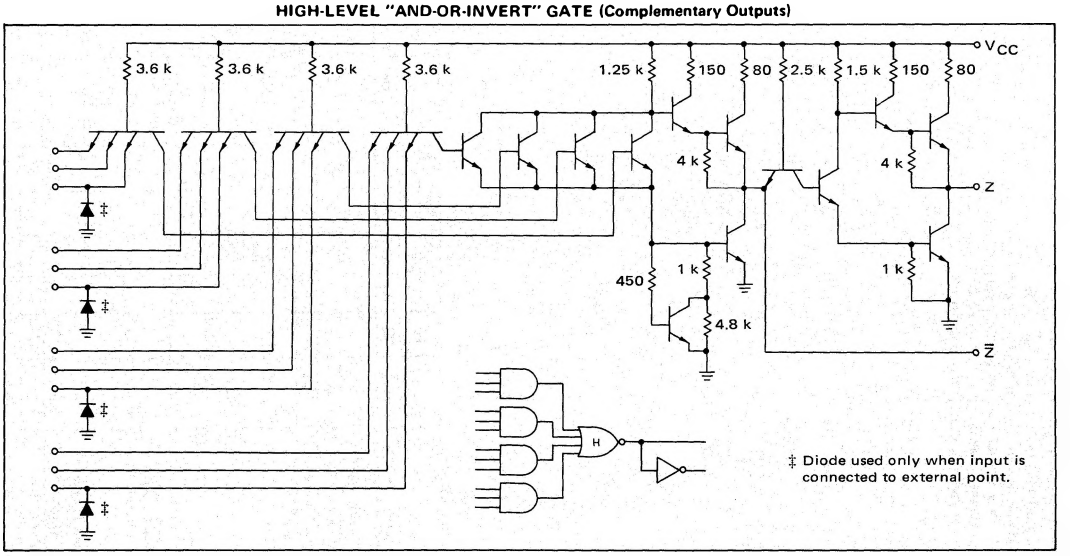
TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	Z	$\overline{Z}$	CONDITIONS
A	24	16	X0 = X2 = X3 = logic "0", X1 = logic "1". A and B are defined by the logic equations.
X1	17	9	

LOW-LEVEL INVERTER



HIGH-LEVEL "AND-OR-INVERT" GATE (Complementary Outputs)



*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

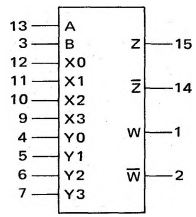
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table. Additionally, test all input-output combinations according to the truth table.

TRUTH TABLE

INPUTS						OUTPUTS		INPUTS				OUTPUTS	
A	B	X0	X1	X2	X3	Z	$\overline{Z}$	Y0	Y1	Y2	Y3	W	$\overline{W}$
0	0	0	ϕ	ϕ	ϕ	0	1	0	ϕ	ϕ	ϕ	0	1
0	0	1	ϕ	ϕ	ϕ	1	0	1	ϕ	ϕ	ϕ	1	0
1	0	ϕ	0	ϕ	ϕ	0	1	ϕ	0	ϕ	ϕ	0	1
1	0	ϕ	1	ϕ	ϕ	1	0	ϕ	1	ϕ	ϕ	1	0
0	1	ϕ	ϕ	0	ϕ	0	1	ϕ	ϕ	0	ϕ	0	1
0	1	ϕ	ϕ	1	ϕ	1	0	ϕ	ϕ	1	ϕ	1	0
1	1	ϕ	ϕ	ϕ	0	0	1	ϕ	ϕ	ϕ	0	0	1
1	1	ϕ	ϕ	ϕ	1	1	0	ϕ	ϕ	ϕ	1	1	0

ϕ = Input level does not affect output.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
		mA							Volts							
		I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OH1}	I_{OH2}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC9309	-55°C	12.4	11.2	16.0	14.4	-1.2	-1.08	–	0.80	2.0	0.4	4.5	–	4.5	5.5	–
	+25°C	12.4	11.2	16.0	14.4	-1.2	-1.08	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5	2.4
	+125°C	12.4	11.2	16.0	14.4	-1.2	-1.08	–	0.80	1.4	0.4	4.5	–	4.5	5.5	–
MC8309	0°C	14.1	12.7	16.0	14.4	-1.2	-1.08	–	0.85	1.9	0.45	4.5	–	4.75	5.25	–
	+25°C	14.1	12.7	16.0	14.4	-1.2	-1.08	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25	2.4
	+75°C	14.1	12.7	16.0	14.4	-1.2	-1.08	–	0.85	1.6	0.45	4.5	–	4.75	5.25	–

Characteristic	Symbol	Pin Under Test	MC9309 Test Limits						MC8309 Test Limits						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													Gnd
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OH1}	I_{OH2}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max																
Input																														
Forward Current	I_F	3	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	–	–	–	3	–	–	–	16	–	8
Leakage Current	I_R	3	–	60	–	60	–	60	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	–	–	–	3	–	–	16	–	8
Clamp Voltage	V_D	3	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	3	–	–	–	–	16	–	–	–	8
Output																														
Output Voltage	V_{OL1}	1	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	1	–	–	–	–	–	–	6,13	3	–	–	–	16	–	–	8
		2	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	2	–	–	–	–	–	13	3,6	–	–	–	16	–	–	8
	V_{OL2}	1	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	–	1	–	–	–	–	6,13	3	–	–	–	–	16	–	8
		2	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	–	–	2	–	–	–	13	3,6	–	–	–	–	16	–	8
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	–	–	1	–	–	13	3,6	–	–	–	16	–	–	8
		2	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	–	–	–	2	–	6,13	3	–	–	–	16	–	–	8
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	16	–	–	–	40	–	–	–	–	–	43	–	–	mAdc	–	–	–	–	–	–	–	–	3,4,5,6, 7,9,10, 11,12,13	–	–	16	–	–	–	8
Switching Parameters																Pulse In		Pulse Out													
Turn-On Delay	t_{pd-}	13/15	–	–	–	32	–	–	–	–	–	36	–	–	ns	13		15		–	–	–	–	–	–	–	16	–	–	11	3,8,9,10,12
Turn-Off Delay	t_{pd+}	13/15	–	–	–	32	–	–	–	–	–	36	–	–	ns	13		15		–	–	–	–	–	–	–	16	–	–	11	3,8,9,10,12

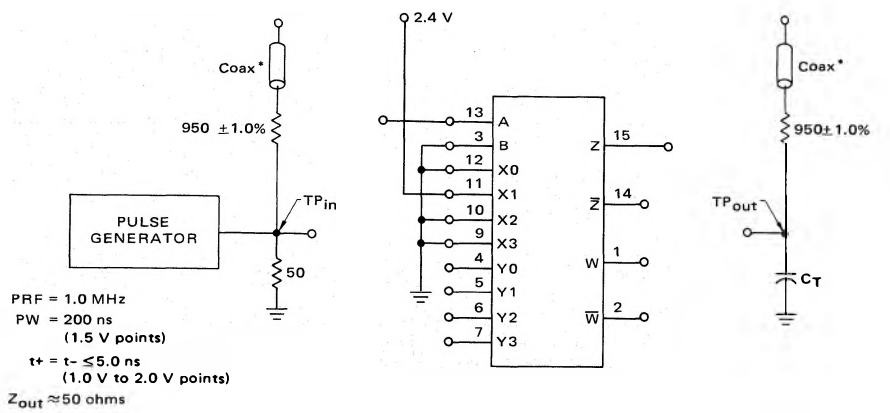
INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC9309 INPUT LOADING FACTOR	MC9309 OUTPUT LOADING FACTOR	
		Z	$\overline{Z}$
MC9300	1.0	10	9.0
MC500	1.06	10.6	9.5
MC2100	0.7	7.0	6.3
MC3100	0.7	7.0	6.3
MC4300	1.0	10	9.0
MC5400	1.0	7.75	7.0
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	9.4	8.4

FAMILY	MC8309 INPUT LOADING FACTOR	MC8309 OUTPUT LOADING FACTOR	
		Z	$\overline{Z}$
MC8300	1.0	10	9.0
MC400	1.0	9.0	8.1
MC2000	0.6	6.0	5.4
MC3000	0.7	7.4	6.6
MC4000	1.0	10	9.0
MC7400	1.0	8.75	7.8
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	10.8	9.7

*Due to logic "1" state drive limitations of the MDTL family.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.