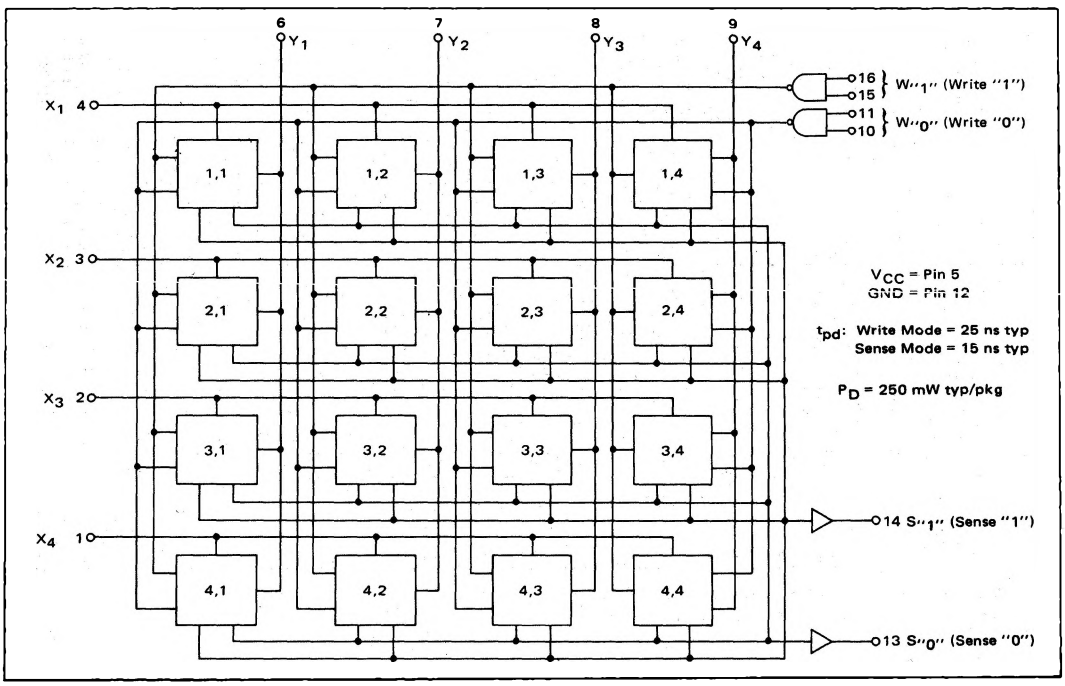
16-BIT SCRATCH PAD MEMORY CELL WITH GATED INPUTS

MC5484L*
MC7484L,P*

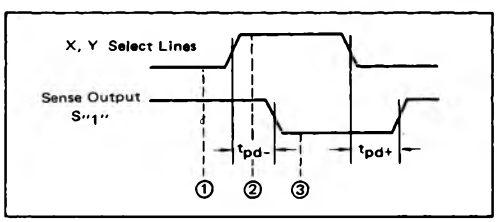
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two gated write amplifiers allow a "1" or a "0" to be written into a selected bit.



– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM



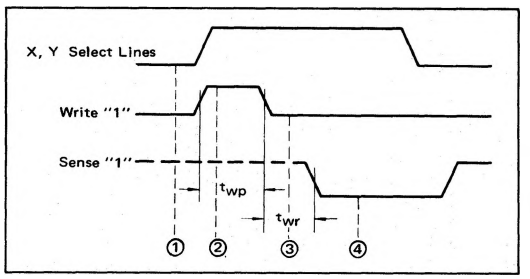
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time (t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

FIGURE 2 – WRITE MODE TIMING DIAGRAM



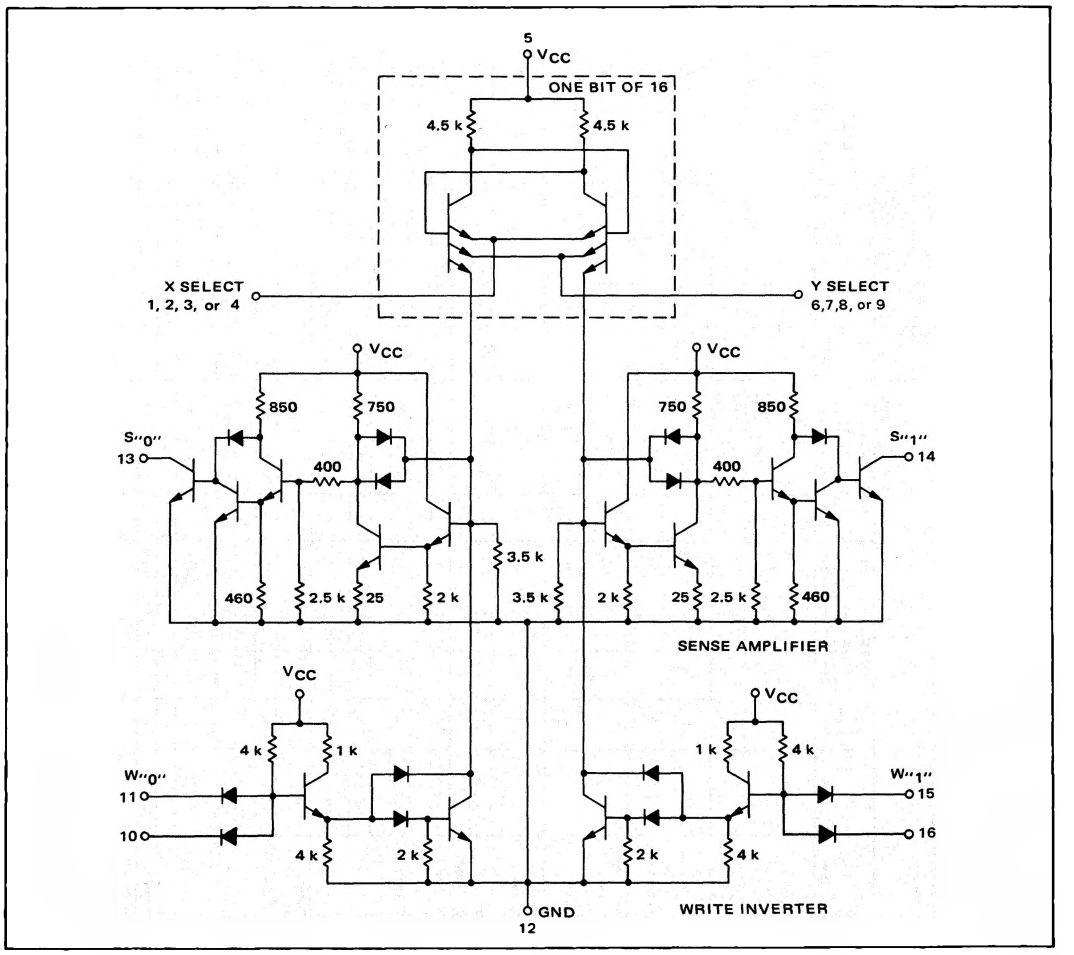
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).

③ Write "1" line returned to low state.

④ The stored bit can be read after the write recovery time (t_{wr}) of 60 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit. Other bits are tested in the same manner. In addition, test procedures are shown for only one Write input of each level. The other Write inputs are tested in the same manner.

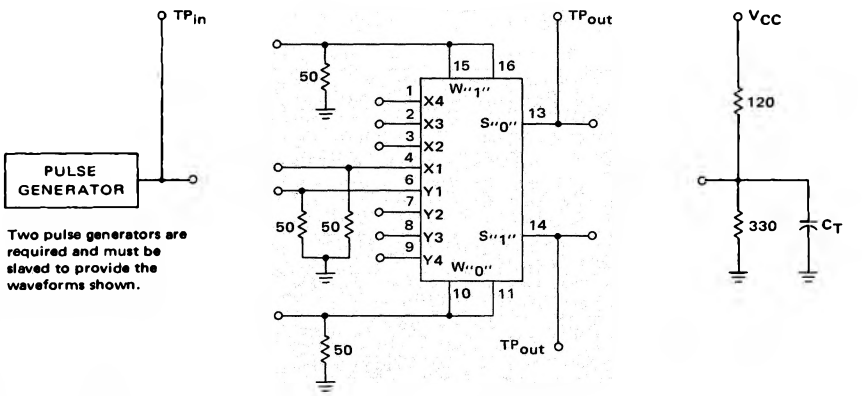
	TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
	mA			Volts										
	$I_{S"0"}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	$V_{th\,W}$	V_{out}	V_{CCL}	V_{CCH}	
MC5484	40	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	2.0	2.0	4.5	5.5	
MC7484	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	2.0	2.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC5484 Test Limits -55 to +125°C Min	Max	Unit	MC7484 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{S"0"}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	$V_{th\,W}$	V_{out}	V_{CCL}	V_{CCH}	Gnd
Input																						
Forward Current Address Lines	I_F	1	–	-11	mAdc	–	-11	mAdc	–	–	–	–	–	–	1	6,7,8,9	–	–	–	–	5	2,3,4,10,11,12,15,16
		6	–	-11	mAdc	–	-11	mAdc	–	–	–	–	–	–	6	1,2,3,4	–	–	–	–	5	7,8,9,10,11,12,15,16
Write Inputs		10	–	-1.60	mAdc	–	-1.60	mAdc	–	–	–	–	–	–	10	–	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	–	-1.60	mAdc	–	-1.60	mAdc	–	–	–	–	–	–	15	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Leakage Current Address Lines	I_R	1	–	0.4	mAdc	–	0.4	mAdc	–	–	–	–	–	–	–	1	–	–	–	–	5	2,3,4,6,7,8,9,10,11,12,15,16
		6	–	0.4	mAdc	–	0.4	mAdc	–	–	–	–	–	–	–	6	–	–	–	–	5	1,2,3,4,7,8,9,10,11,12,15,16
Write Inputs		10	–	0.1	mAdc	–	0.1	mAdc	–	–	–	–	–	–	–	10	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	–	0.1	mAdc	–	0.1	mAdc	–	–	–	–	–	–	–	15	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Breakdown Voltage Address Lines	BV_{in}	1	5.5	–	Vdc	5.5	–	Vdc	–	–	1	–	–	–	–	–	–	–	–	–	5	2,3,4,6,7,8,9,10,11,12,15,16
		6	5.5	–	Vdc	5.5	–	Vdc	–	–	6	–	–	–	–	–	–	–	–	–	5	1,2,3,4,7,8,9,10,11,12,15,16
Write Inputs		10	5.5	–	Vdc	5.5	–	Vdc	–	10	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	5.5	–	Vdc	5.5	–	Vdc	–	15	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Output (Note 1)																						
Output Voltage Write "1"	**	–	–	–	–	–	–	–	–	–	–	–		10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0" Inhibit	**	–	–	–	–	–	–	–	–	–	–	1,6	–	–	15,16	10,11	–	–	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	15,16	–	–	1,6	10,11	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	13	–	0.45	Vdc	–	0.45	Vdc	13	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1" Inhibit	**	–	–	–	–	–	–	–	–	–	–	1,6	–	–	10,11	16,16	–	–	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	13	–	0.45	Vdc	–	0.45	Vdc	13	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Leakage Current Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Leakage Current	I_{OLK}	14	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	1,6	–	–	–	–	–	14	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	15,16	–	–	1,6	10,11	–	5	–	2,3,4,7,8,9,12
Leakage Current	I_{OLK}	13	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	1,6	–	–	–	–	–	13	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	15,16	1,6,7,8,9	–	–	5	–	2,3,4,10,11,12
Leakage Current	I_{OLK}	13	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	–	–	–	–	1,6,7,8,9	–	13	5	–	2,3,4,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	10,11	1,6,7,8,9	–	–	5	–	2,3,4,12,15,16
Leakage Current	I_{OLK}	14	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	–	–	–	–	1,6,7,8,9	–	14	5	–	2,3,4,10,11,12,15,16
Power Requirements (Total Device)																						
Power Supply Drain	I_{PD}	5	–	78 #	mAdc	–	91 #	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10, 11,12,13,14,15,16

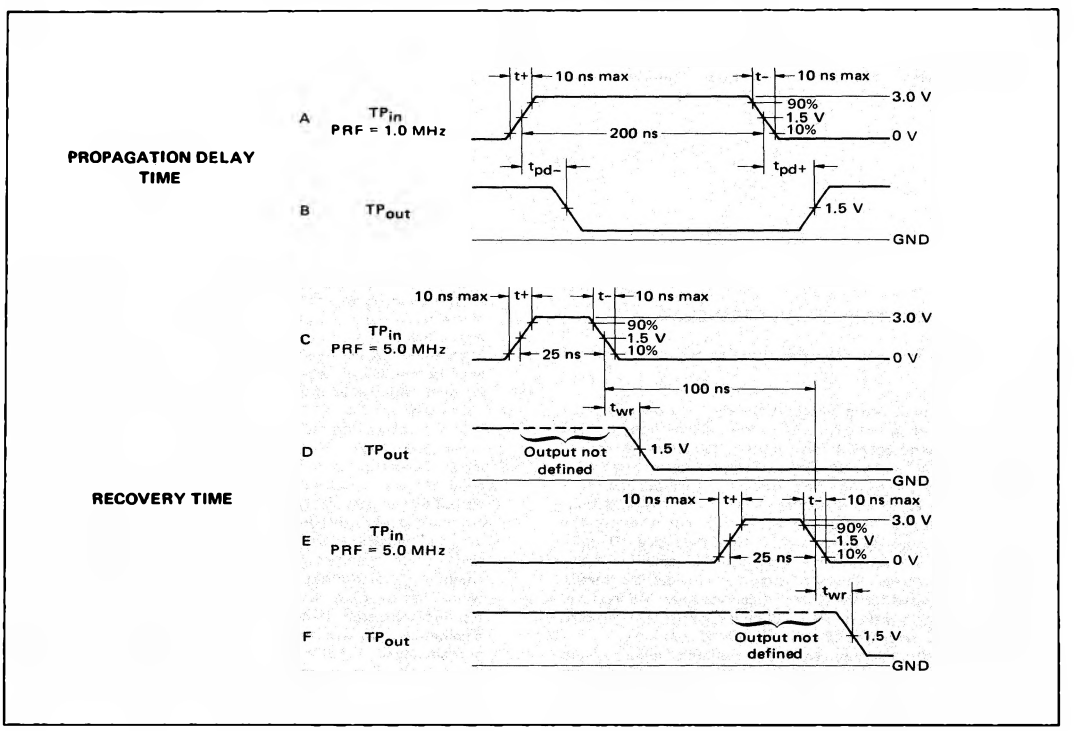
Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. ** Indicates preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		C_T*	Limits	
			4 X_1	3 X_2	2 X_3	1 X_4	6 Y_1	7 Y_2	8 Y_3	9 Y_4	10 W "0"	15 W "1"	13 S "0"	14 S "1"	pF	MC5484 ns max	MC7484 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	15	25	25
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	15	25	25
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd-}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	15	45	45
	t_{pd-}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	55	55
Turn-On Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd-}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	15	45	45
	t_{pd-}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	55	55
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	B	–	15	30	30
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	–	B	15	30	30
Write Recovery Time	t_{wr}	14	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	–	D	15	60	60
		13	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	–	15	60	60
																ns min	ns min
Write Pulse Width	t_{wp}	–	Tested during t_{wr} tests.													25	25

*Capacitance value for load of the Switching Time Test Circuit

**Preconditioning procedures for subsequent test.

OPERATING CHARACTERISTICS

Sixteen flip-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Each flip-flop, consisting of two cross-coupled triple-emitter transistors, is used to store one bit. Memory status of a particular bit is determined by sensing which of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical "1" sensing outputs are connected to the sense logic "1" amplifier input, and all 16 of the logical "0" sensing outputs are connected to the sense logic "0" amplifier input. The remaining emitters on each transistor provides the matrix connections required for the X- and Y-address lines. Address line inputs are normally held at logic "0" and currents from all conducting flip-flop transistors flow out of these address lines.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logic "1" voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logic "0" level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logic "1" or the sense amplifier associated with a logic "0" is activated. When this occurs, the output of the activated sense amplifier drops from a logic "1" to a logic "0" level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing.

To store new information in a flip-flop, it is necessary to address it and apply logic "1" voltage to the appropriate write amplifier input. The output of the write amplifier responds by dropping to a logic "0" level. Since all logic "0" sense lines are connected to the output of the logic "0" write amplifier and all logic "1" sense lines are connected to the output of the logic "1" write amplifier, a logic "0" voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on, causing the other transistor to turn off.

TYPICAL APPLICATIONS

A fast scratch pad memory offers the system designer several design alternatives. Temporary memory with a greater storage capacity than simple registers can be distributed throughout a system. The basic technique for expanding bit capacity is shown in Figure 3; Figure 4 illustrates a method for expanding word capacity.

Optimum design of the selection line drivers depends on the specific system application. The maximum load presented to the drivers by the selection lines is a function of the sequence used to address the memory. The desired logic swing and noise immunity should also be considered when designing the drivers. Each of the 16 flip-flops draws a maximum dc supply current of 2.75 mA (for V_{CC} = 5.0 Vdc). The total current flowing in all 16 flip-flops, and consequently the summed current in the eight selection lines, is 44 mA. (Each selection line is tested for a maximum of 11 mA).

Consider the sequence involved in selecting the four bits X_1Y_1, X_1Y_2, X_1Y_3, and X_1Y_4 simultaneously. If the four Y select lines are enabled before the X_1 line then each of the four X lines must carry the full current from four cells, i.e., 11 mA. The Y drivers must also have the capability of sinking 11 mA if the four X drivers are enabled before a Y driver. However, if the memory accessing sequence specifies that only a single bit may be selected at a time and, consequently, that only one of the X (or Y) selection lines may be high at a time, then the driver requirements can be relaxed somewhat. This is possible because of current sharing in the multi-emitters of the storage flip-flop transistors. If the voltages at the emitters of the "on" transistor differ by no more than approximately 100 mV, then each emitter will carry an appreciable portion of the transistor current. The saturation characteristics of the drivers determine the emitter potentials and, therefore, the division of cell current among the various drivers. Since the V_{OL} of the driver will increase if the collector current increases, the selection currents will be almost evenly distributed among the drivers if the driver saturation characteristics are reasonably uniform. If operation is restricted to a single X selection line and a single Y selection line and current sharing is assumed, then each select line must be capable of carrying the full current from a single cell plus approximately one half of the current from three cells. Each line must, therefore, carry:

$$11/4 + (3)\ (1/2)\ (11/4) = 6.88\ \text{mA}.$$

Since the dc output levels of the driver transistors determine the noise immunity of the selection line, the system noise environment and the desired noise immunity should enter into the driver selection.

FIGURE 3 – 16 WORD, N BIT MEMORY

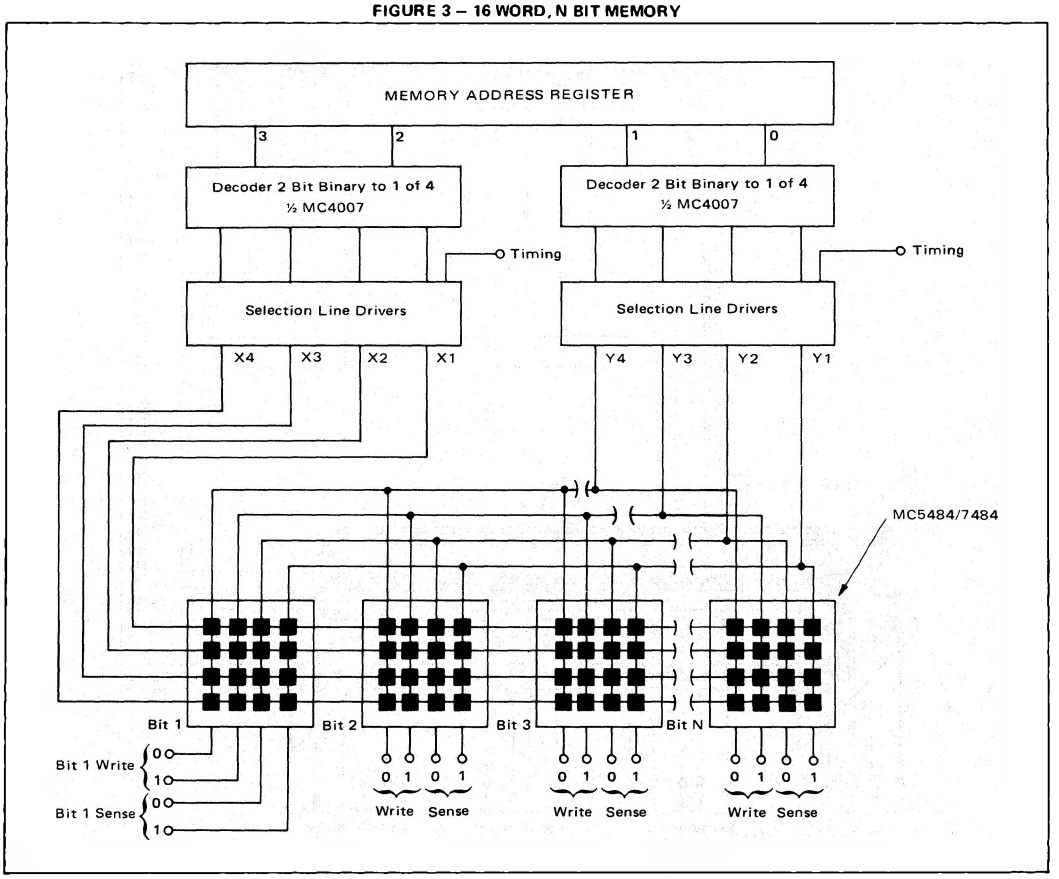


FIGURE 4 – 64 WORD, 4 BIT MEMORY