4-BIT BINARY
FULL ADDER

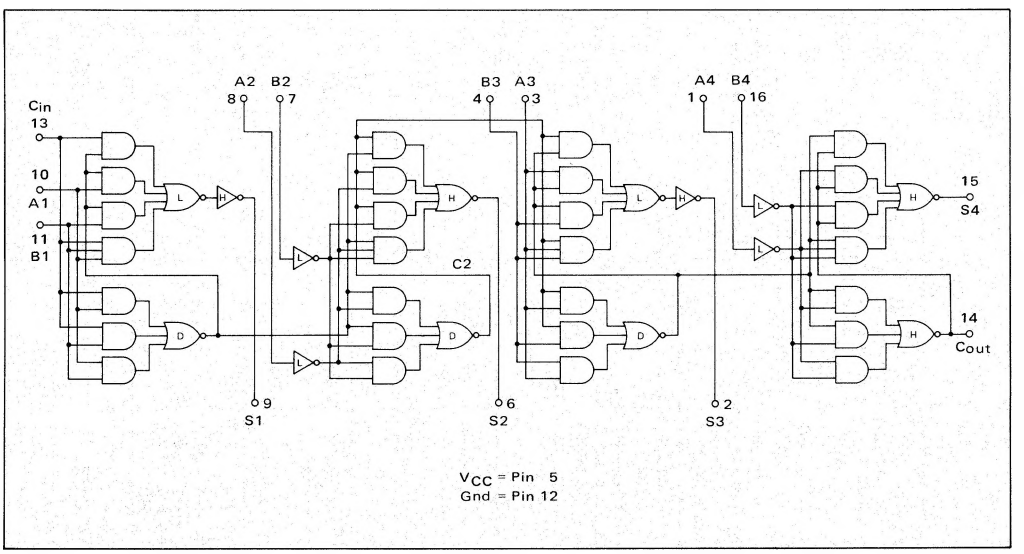
MC5483L*
MC7483L,P*

INPUT				OUTPUT					
				When $C_{in}=0$			When $C_{in}=1$		
				When C2 = 0			When C2 = 1		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	S1 / S3	S2 / S4	C2 / C_o	S1 / S3	S2 / S4	C2 / C_o
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

This device performs the logical addition of two 4-bit binary numbers. The Sum outputs for each bit and the Carry from the fourth bit (C4) are provided. A look-ahead carry is provided internally, utilizing a Darlington-connected serial carry within each bit.

Low and high-level inverters and gates are used in the construction of the MC5483/7483 to maximize output drive capability and minimize power dissipation.

Input conditions at A1, A2, B1, B2, and C_{in} are used to determine outputs S1 and S2, and the value of the internal carry, C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs S3, S4, and C_{out}.



Input Loading Factor:
A1, A3, B1, B3, C0 = 4
A2, A4, B2, B4 = 1

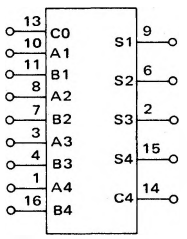
Output Loading Factor:
S1, S2, S3, S4 = 10
C_{out} = 5

Total Power Dissipation = 390 mW typ/pkg
Propagation Delay Time = 35 ns typ

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one set of input conditions. To complete testing, sequence through remaining input conditions according to the truth table.

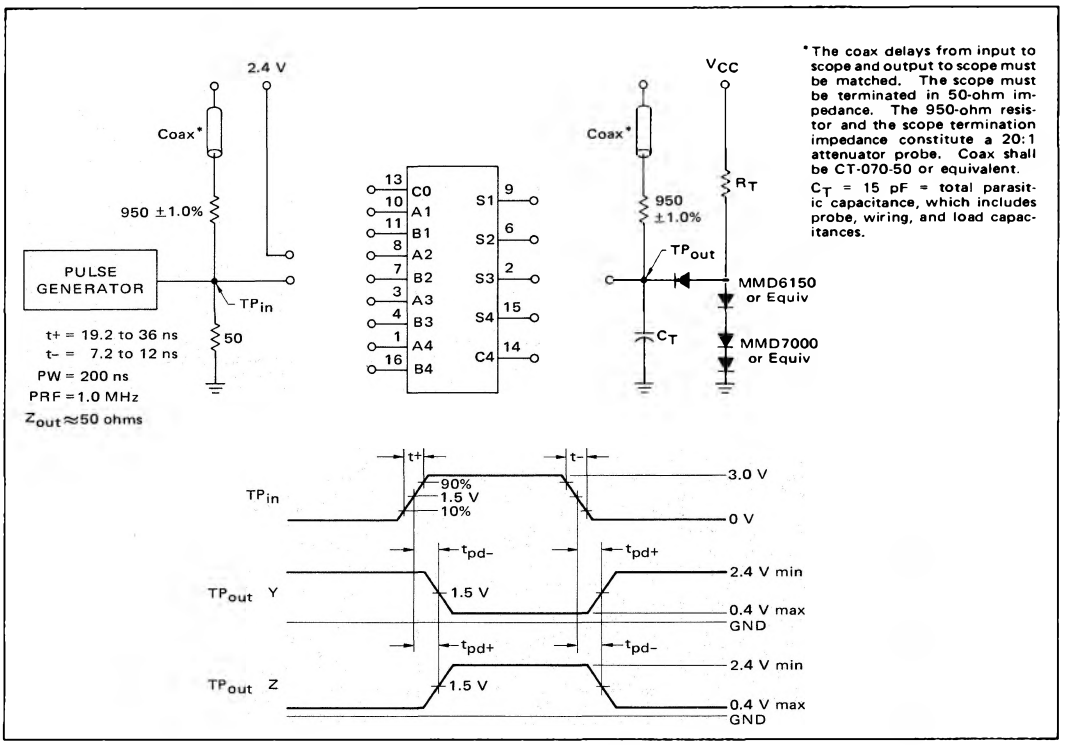


									TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
									mA				Volts							
									I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}
									MC5483	16	8.0	-0.4	-0.2	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5
									MC7483	16	8.0	-0.4	-0.2	0.4	2.4	5.5	4.5	2.0	0.8	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5483 Test Limits -55 to +125°C Min	Max	Unit	MC7483 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	–	1	–	–	–	–	–	–	5	12
		3	–	-6.4		–	-6.4		–	–	–	–	3	–	–	4,7,8	–	–	–		
		4	–	-6.4		–	-6.4		–	–	–	–	4	–	–	3,7,8	–	–	–		
		7	–	-1.6		–	-1.6		–	–	–	–	7	–	–	–	–	–	–		
		8	–	-1.6		–	-1.6		–	–	–	–	8	–	–	–	–	–	–		
		10	–	-6.4		–	-6.4		–	–	–	–	10	–	–	11,13	–	–	–		
		11	–	↓		–	↓		–	–	–	–	11	–	–	10,13	–	–	–		
		13	–	↓		–	↓		–	–	–	–	13	–	–	10,11	–	–	–		
		16	–	-1.6	↓	–	-1.6	↓	–	–	–	–	16	–	–	–	–	–	–	↓	↓
Leakage Current	I_{R1}	1	–	40	μAdc	–	40	μAdc	–	–	–	–	–	1	–	–	–	–	–	5	12
		3	–	160		–	160		–	–	–	–	–	3	–	–	–	–	–		4,7,8,12
		4	–	160		–	160		–	–	–	–	–	4	–	–	–	–	–		3,7,8,12
		7	–	40		–	40		–	–	–	–	–	7	–	–	–	–	–		12
		8	–	40		–	40		–	–	–	–	–	8	–	–	–	–	–		12
		10	–	160		–	160		–	–	–	–	–	10	–	–	–	–	–		11,12,13
		11	–	↓		–	↓		–	–	–	–	–	11	–	–	–	–	–		10,12,13
		13	–	↓		–	↓		–	–	–	–	–	13	–	–	–	–	–		10,11,12
		16	–	40	↓	–	40	↓	–	–	–	–	–	16	–	–	–	–	–	↓	12
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	–	1	–	–	–	–	5	12
		3	–	↓		–	↓		–	–	–	–	–	–	3	–	–	–	–		4,7,8,12
		4	–	↓		–	↓		–	–	–	–	–	–	4	–	–	–	–		3,7,8,12
		7	–	↓		–	↓		–	–	–	–	–	–	7	–	–	–	–		12
		8	–	↓		–	↓		–	–	–	–	–	–	8	–	–	–	–		12
		10	–	↓		–	↓		–	–	–	–	–	–	10	–	–	–	–		11,12,13
		11	–	↓		–	↓		–	–	–	–	–	–	11	–	–	–	–		10,12,13
		13	–	↓		–	↓		–	–	–	–	–	–	13	–	–	–	–		10,11,12
		16	–	↓	↓	–	↓	↓	–	–	–	–	–	–	16	–	–	–	–	↓	12
Output																					
Output Voltage	V_{OL}	2	–	0.4	Vdc	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1,3,4,7,8,16	5	–	12
		6	–	↓		–	↓		6	–	–	–	–	–	–	–	–	7,8,10,11,13		–	
		9	–	↓		–	↓		9	–	–	–	–	–	–	–	–	7,8,10,11,13		–	
		14	–	↓		–	↓		–	14	–	–	–	–	–	–	–	1,16		–	
		15	–	↓		–	↓		15	–	–	–	–	–	–	–	–	1,3,4,7,8,16	↓	–	↓
	V_{OH}	2	2.4	–	Vdc	2.4	–	Vdc	–	–	2	–	–	–	–	–	3	1,4,7,8,16	5	–	12
		6	↓	–	↓	↓	–	↓	–	–	6	–	–	–	–	–	10,11	7,8,13	↓	–	↓
		9	↓	–	↓	↓	–	↓	–	–	9	–	–	–	–	–	10,11,13	7,8	↓	–	↓
		14	↓	–	↓	↓	–	↓	–	–	–	14	–	–	–	–	1,16	3,4	↓	–	↓
		15	↓	–	↓	↓	–	↓	–	–	15	–	–	–	–	–	3,7,8	1,4,16	↓	–	↓
Short-Circuit Current	I_{SC}	2	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	–	–	1,3,4,7,8, 10,11,13,16	–	–	–	5	2,12
		6	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	↓	–	–	–		6,12
		9	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	↓	–	–	–		9,12
		14	↓	-70	↓	↓	-70	↓	–	–	–	–	–	–	–	↓	–	–	–		12,14
		15	↓	-55	↓	↓	-55	↓	–	–	–	–	–	–	–	↓	–	–	–	↓	12,15
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	16	–	110**	mAdc	–	128**	mAdc	–	–	–	–	–	–	–	1,3,8,10	–	–	–	5	4,7,11,12,16

**Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

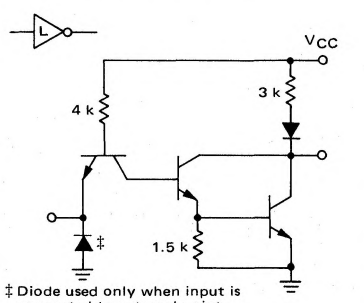
(Letters shown in output columns refer to waveforms. Dash indicates pin left open.)

TEST	FROM INPUT	TO OUTPUT	INPUT A4 Pin 1	A3 Pin 3	B3 Pin 4	B2 Pin 7	A2 Pin 8	A1 Pin 10	B1 Pin 11	C0 Pin 13	B4 Pin 16	OUTPUT S1 Pin 9	S2 Pin 6	S3 Pin 2	S4 Pin 15	C4 Pin 14	R_T Ohms	LIMITS (ns) Max
t_{pd+}	C0	S1	–	–	–	Gnd	Gnd	2.4 V	Gnd	–	–	Y	–	–	–	–	400	34
t_{pd-}																		40
t_{pd+}	C0	S2	–	–	–	Gnd	2.4 V	2.4 V	Gnd	–	–	–	Y	–	–	–	400	38
t_{pd-}																		42
t_{pd+}	C0	S3	–	2.4 V	Gnd	Gnd	2.4 V	2.4 V	Gnd	–	–	–	–	Y	–	–	400	50
t_{pd-}																		60
t_{pd+}	C0	S4	2.4 V	2.4 V	Gnd	Gnd	2.4 V	2.4 V	Gnd	–	Gnd	–	–	–	Y	–	400	55
t_{pd-}																		55
t_{pd+}	C0	C4	2.4 V	2.4 V	Gnd	Gnd	2.4 V	2.4 V	Gnd	–	Gnd	–	–	–	①	Z	780	48
t_{pd-}																		32
t_{pd+}	A2	S2	–	–	–	Gnd	–	Gnd	Gnd	Gnd	–	–	Z	–	–	–	400	40
t_{pd-}																		35
t_{pd+}	B2	S2	–	–	–	–	Gnd	Gnd	Gnd	Gnd	–	–	Z	–	–	–	400	40
t_{pd-}																		35
t_{pd+}	A4	S4	–	Gnd	Gnd	–	–	–	–	–	Gnd	–	–	–	Z	–	400	40
t_{pd-}																		35
t_{pd+}	B4	S4	Gnd	Gnd	Gnd	–	–	–	–	–	–	–	–	–	Z	–	400	40
t_{pd-}																		35

① Apply load circuit of same configuration as load of Switching Time Test Circuit.

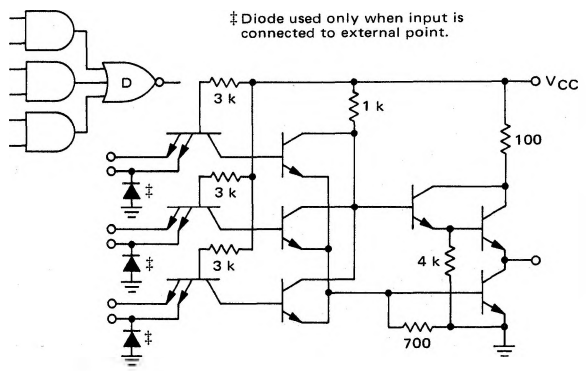
This full adder is constructed using gates and inverters interconnected as shown by the logic diagram.

LOW-LEVEL INVERTER

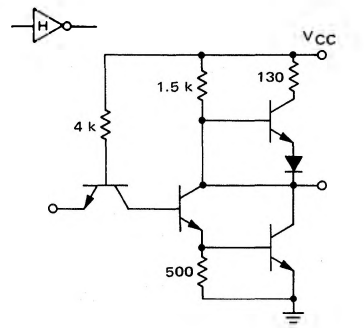


‡ Diode used only when input is connected to external point.

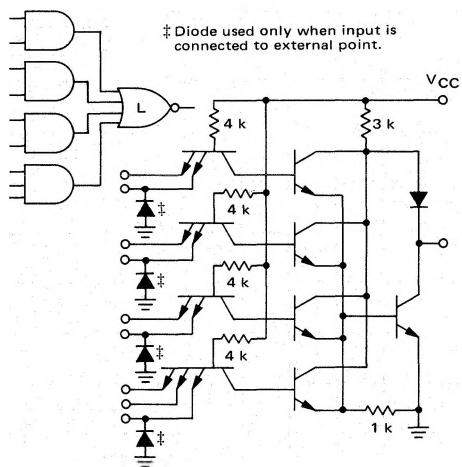
"AND-OR-INVERT" GATE WITH DARLINGTON OUTPUT



HIGH-LEVEL INVERTER



LOW-LEVEL "AND-OR-INVERT" GATE



HIGH-LEVEL "AND-OR-INVERT" GATE