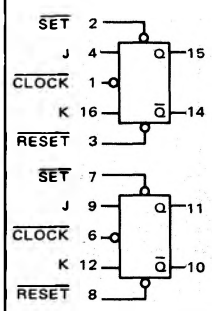
DUAL J-K FLIP-FLOP

MC7476P*



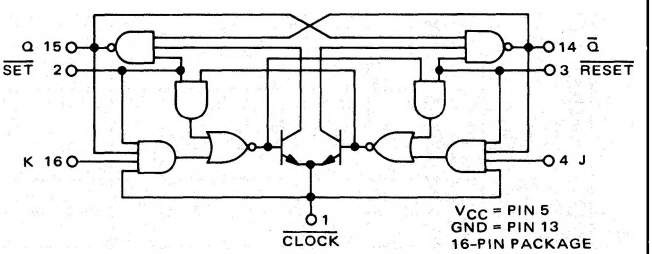
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Input Loading Factor:
J, K = 1
$\overline{\text{CLOCK}}$, $\overline{\text{SET}}$, $\overline{\text{RESET}}$ = 2

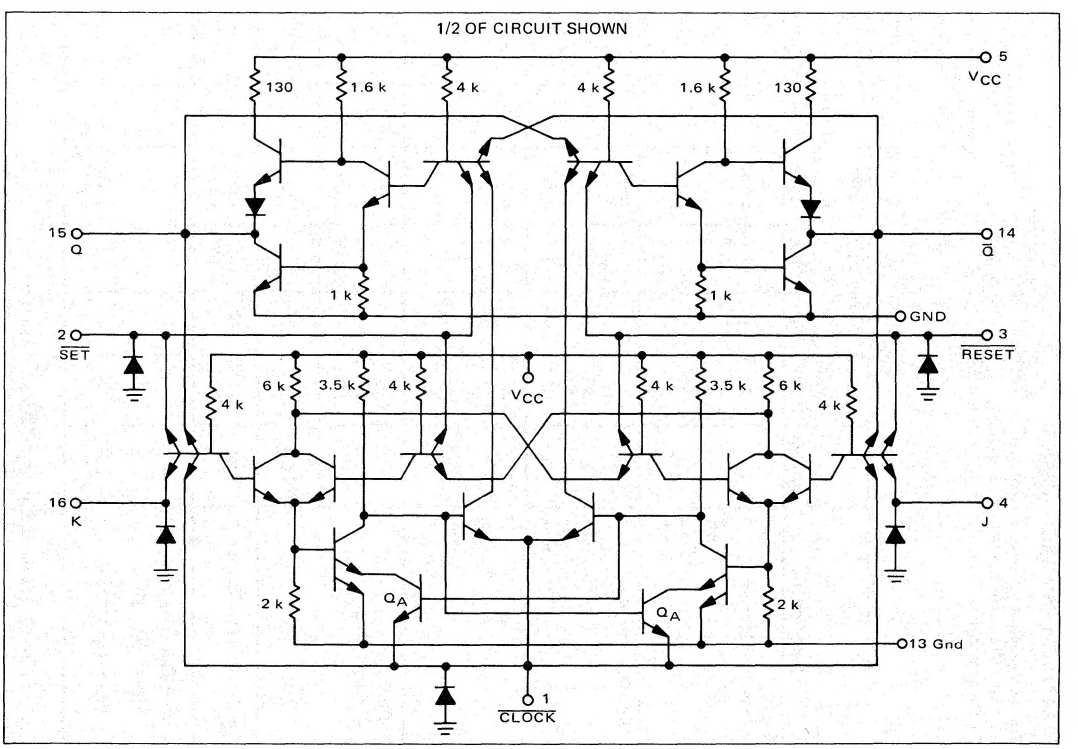
Output Loading Factor = 10
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 15 MHz typ

This negative-edge-clocked dual J-K flip-flop operates on the master-slave principle. The device is quite useful for simple registers and counters where multiple J and K inputs are not required. Available only in the 16-pin package, this device provides both $\overline{\text{SET}}$ and $\overline{\text{RESET}}$ inputs on both flip-flops in the package.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

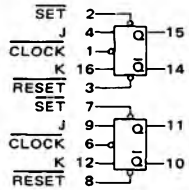


* P suffix = 16-pin plastic package (Case 612)
See General Information section for package outline dimensions.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC7476 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Input																	
Forward Current J	I_F	4	-	-1.6	mAdc	-	-	4	-	-	1,3*	-	-	-	-	5	6,9,12,13
K		16	-	-1.6		-	-	16	-	-	1,2*	-	-	-	-		
$\overline{\text{Set}}$		2	-	-3.2		-	-	2	-	-	4,16	-	-	-	-		
$\overline{\text{Reset}}$		3	-			-	-	3	-	-	4,16	-	-	-	-		
$\overline{\text{Clock}}$		1	-			-	-	1	-	-	2*,4,16	-	-	-	-		
		1	-			-	-	1	-	-	3*,4,16	-	-	-	-		
Leakage Current J	I_{R1}	4	-	40	μAdc	-	-	-	4	-	-	-	-	-	-	5	1,3,6,9,12,13
K		16	-	40		-	-	-	16	-	-	-	-	-	-		1,2,6,9,12,13
$\overline{\text{Set}}$		2	-	80		-	-	-	2	-	-	-	-	-	-		1,6,9,12,13,16
$\overline{\text{Reset}}$		3	-			-	-	-	3	-	-	-	-	-	-		1,4,6,9,12,13
$\overline{\text{Clock}}$		1**	-			-	-	-	1	-	-	-	-	-	-		2,3,4,6,9,12,13,16
J	I_{R2}	4	-	1.0	mAdc	-	-	-	-	4	-	-	-	-	-	5	1,3,6,9,12,13
K		16	-			-	-	-	-	16	-	-	-	-	-		1,2,6,9,12,13
$\overline{\text{Set}}$		2	-			-	-	-	-	2	-	-	-	-	-		1,6,9,12,13,16
$\overline{\text{Reset}}$		3	-			-	-	-	-	3	-	-	-	-	-		1,4,6,9,12,13
$\overline{\text{Clock}}$		1	-			-	-	-	-	1	-	-	-	-	-		2,3,4,6,9,12,13,16
Output																	
Output Voltage	V_{OL}	14	-	0.40	Vdc	14	-	-	-	-	-	3	2	-	5	-	6,9,12,13
		15	-	0.40	Vdc	15	-	-	-	-	-	2	3	-	5	-	6,9,12,13
	V_{OH}	14	2.4	-	Vdc	-	14	-	-	-	-	2	3	-	5	-	6,9,12,13
		15	2.4	-	Vdc	-	15	-	-	-	-	3	2	-	5	-	6,9,12,13
Short-Circuit Current	I_{SC}	14	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	3,6,9,12,13,14
		15	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	2,6,9,12,13,15
Power Requirements (Total Device)																	
Power Supply Drain	I_{PD}	5	-	32	mAdc	-	-	-	-	-	-	-	-	5	-	-	2,7,13
		5	-	32	mAdc	-	-	-	-	-	-	-	-	5	-	-	3,8,13

*Momentarily ground pin prior to taking measurement.

**Under normal operating conditions this current is negative. This test guarantees that positive leakage will not exceed the limit shown.

OPERATING CHARACTERISTICS

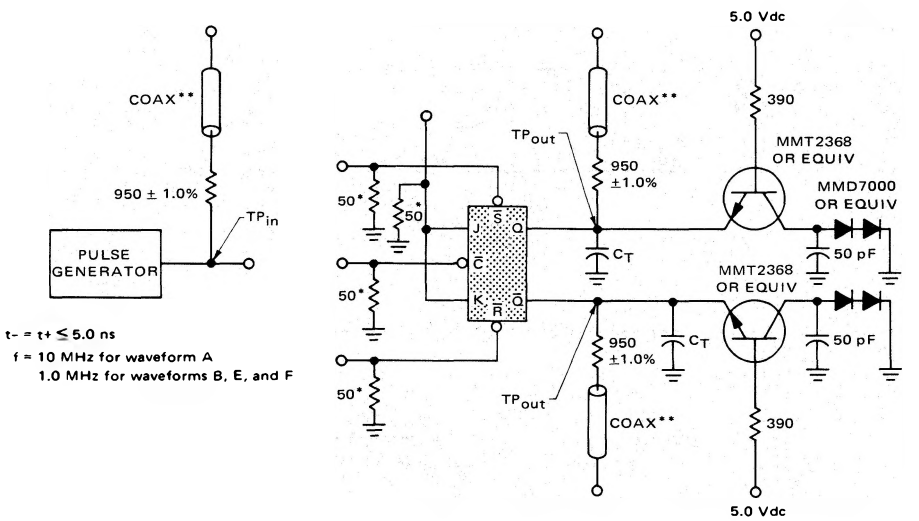
Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{RESET}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{RESET}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of -2.0 V appear at the clock.

SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together for testing $\overline{\text{SET}}$ and $\overline{\text{RESET}}$. Only one pulse generator is required for J, K, and $\overline{\text{CLOCK}}$ tests.

*Resistor used only when that input is under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

OPERATING CHARACTERISTICS (continued)

TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	2.4 V	†	†	10	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	2.4 V	C	C	–	50	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	2.4 V	D	D	–	50	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	E	F	G	H	10	50	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	E	F	G	H	10	50	ns
Enable Voltage	V_{EN}	B	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	B	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS