MC68175

Advance Information

FLEXchip™ SIGNAL PROCESSOR

The FLEX™ protocol is a multi-speed, high-performance protocol adopted by leading service providers worldwide as a de facto paging standard. The FLEX protocol gives service providers the increased capacity, added reliability, and enhanced pager battery performance they need today. It also provides an upward migration path to the service provider that is completely transparent to the end user.

The MC68175 FLEXchip™ IC is part of a total solution available from Motorola for providing FLEX capabilities in a low-power, low-cost system. The FLEXchip simplifies implementation of a FLEX paging device by interfacing with any of several off-the-shelf paging receivers, such as the MC13150 or MC3374, and any of several off-the-shelf host microcontroller / microprocessors. The primary function of the FLEXchip is to process information received and demodulated from a FLEX-radio paging channel, select messages addressed to the paging device, and communicate the message information to the host. The host interprets the message information in an appropriate manner (numeric, alphanumeric, binary, etc.) and handles all the I / O activity. The FLEXchip IC also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low power mode when message information for the paging device is not being received. **Figure 1** shows the MC68175 functional block diagram.

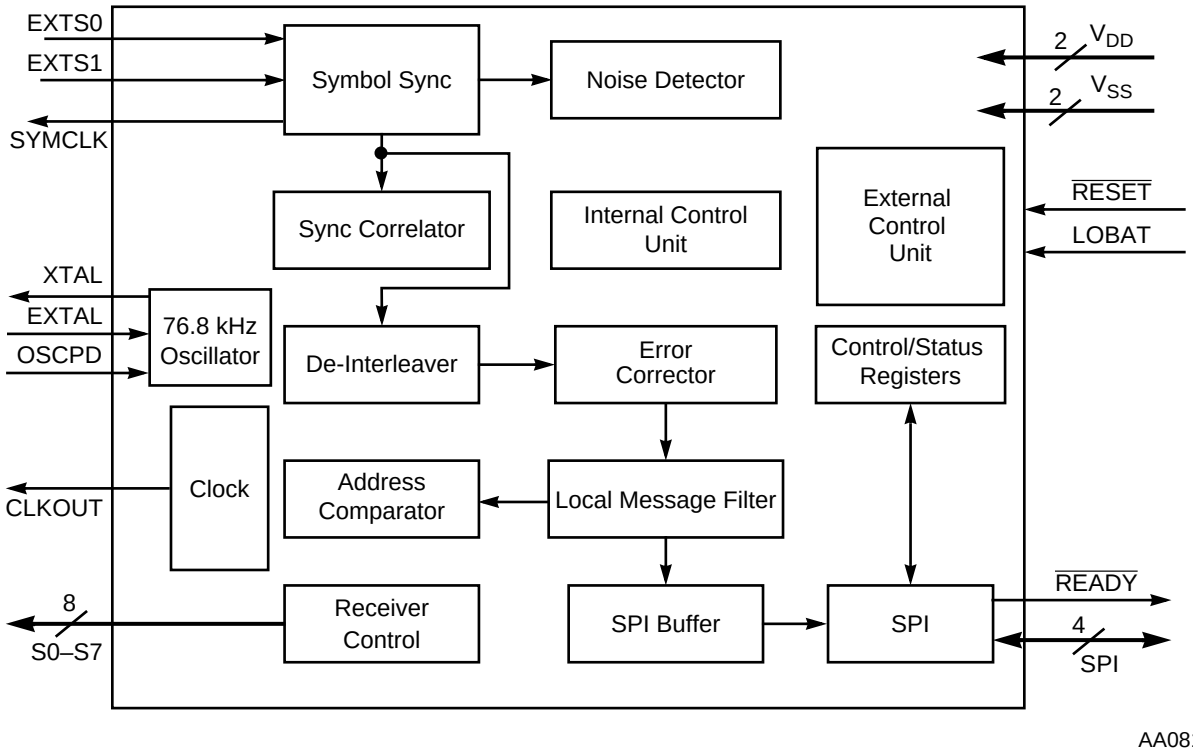

Figure 1 MC68175 Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

Email: dsphelp@dsp.sps.mot.com

Internet: http://www.motorola-dsp.com

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
PIN	True	Asserted	V_{IH} / V_{OH}
PIN	False	Deasserted	V_{IL} / V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

- FLEX paging protocol signal processor
- Sixteen programmable user address words
- Sixteen fixed temporary addresses
- 1600-, 3200-, and 6400-bits-per-second decoding
- Any-phase or single-phase decoding
- Uses standard Serial Peripheral Interface (SPI) in Slave mode
- Allows low current Stop mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX software fragmentation and group messaging support
- Real time clock over-the-air update support
- Compatible with synthesized receivers
- Low Battery Indication (external detector)
- 1.8 to 3.3 V low power operation
- 32-pin Thin Quad Flat Pack (TQFP) package

ADDITIONAL SUPPORT

FLEX System Software from Motorola is a family of software components for building world-class products incorporating messaging capabilities. FLEXstack™ Software is specifically designed to support the FLEXchip IC. FLEXstack Software runs on a product's host processor and takes care of communicating with the FLEXchip IC and fully interpreting the codewords that are passed to the host from the FLEXchip IC.

DOCUMENTATION

This document is the primary document supporting the MC68175 FLEXchip IC. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

SIGNAL GROUPINGS

The input and output signals of the MC68175 are organized into six functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**.

Table 1-1 MC68175 Functional Signal Groupings

Functional Group	Number of Signals	Detailed Description
Power Input and Monitoring	7	**Table 1-2**
Processor Clocks	1	**Table 1-3**
Reset	1	**Table 1-4**
Current Symbol Inputs	2	**Table 1-5**
Serial Peripheral Interface (SPI)	5	**Table 1-6**
Receiver Control Port	8	**Table 1-7**

Figure 1-1 is a diagram of MC68175 signals by functional group.

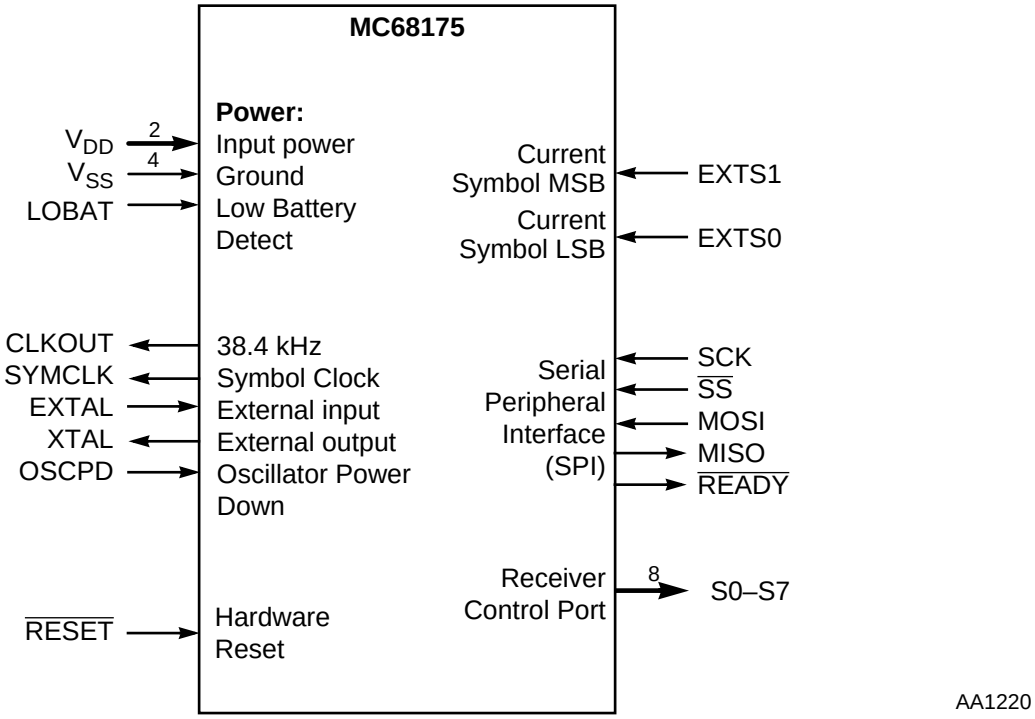


Figure 1-1 Signals Identified by Functional Group

POWER INPUT AND MONITORING

Table 1-2 Power Input, Monitoring, and Control Signals

Power Name	Description
V_{DD}	**Power**—V_{DD} is the input power for the IC.
V_{SS}	**Ground**—V_{SS} is ground connection for the IC.
LOBAT	**Low Battery**—LOBAT provides an input signal to indicate to the IC when external battery power is going low.

PROCESSOR CLOCK

Table 1-3 Processor Clock Signals

Signal Name	Type	State During Reset	Signal Description
CLKOUT	Output	Indeterminate	**Clock Output**—This is typically a 38.4 kHz clock output (derived from 76.8 kHz oscillator).
SYMCLK	Output	Indeterminate	**Recovered Symbol Clock**—Data is synchronized to the internal clock and this recovered clock output enhances lockon capability by reducing jitter from cable-induced noise.
EXTAL	Input	Input	**External Clock/Crystal Input**—EXTAL interfaces the internal crystal oscillator input to a 76.8 kHz crystal input or other external input clock.
XTAL	Output	Indeterminate	**External Clock/Crystal Output**—This is typically a 76.8 kHz clock output.
OSCPD	Input	Input	**Oscillator Power Down**—This input determines whether the internal oscillator is used. Connect this pin to V_{SS} when using the 76.8 kHz crystal input. Connect this pin to V_{DD} when using an external input clock signal.

RESET

Table 1-4 Test and Reset Signals

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Input	**Reset**—This input is a direct hardware reset on the FLEXchip IC. When $\overline{\text{RESET}}$ is asserted low, the FLEXchip IC is initialized and placed in the Reset state.

CURRENT SYMBOL INPUTS

Table 1-5 Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
EXTS1	Input	Input	**External Symbol 1**—This is the Most Significant Bit (MSB) of the symbol being tested.
EXTS0	Input	Input	**External Symbol 0**—This is the Least Significant Bit (LSB) of the symbol being tested.

SERIAL PERIPHERAL INTERFACE (SPI)

Table 1-6 Serial Peripheral Interface (SPI) Signals

Signal Name	Signal Type	State During Reset	Signal Description
SCK	Input	Input	**SPI Serial Clock**—The SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if the Slave Select ($\overline{SS}$) signal is not asserted.
$\overline{SS}$	Input	Input	**SPI Slave Select**—This signal is used to enable the SPI slave for transfer.
MOSI	Input	Input	**SPI Master-Out-Slave-In**—Since the MC68175 is always a slave device, this is the data input for SPI communications. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data.
MISO	Output	Tri-stated	**SPI Master-In-Slave-Out**—Since the MC68175 is always a slave device, this is the data output for SPI communications. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data.
$\overline{READY}$	Output	Output, driven high	**SPI Ready**—This signal is driven low when the FLEXchip IC is ready for an SPI packet.

RECEIVER CONTROL PORT

Table 1-7 Receiver Control Port Signals

Signal Name	Signal Type	State During Reset	Signal Description
S0–S7	Output	Tri-stated	**Serial Port 0–Serial Port 7**—These signals are the eight receiver control ports.

SECTION 2

SPECIFICATIONS

INTRODUCTION

The MC68175 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	−0.3 to +3.6	V
All input voltages	V_{IN}	GND − 0.5 to V_{CC} + 0.5	V
Current drain per pin excluding V_{DD} and V_{SS}	I	10	mA
Operating temperature range	T_A	–30 to +85	°C
Storage temperature	T_{STG}	–55 to +150	°C

Notes: 1. GND = 0 V, V_{CC} = 1.8 to 3.3 V, T_A = 0°C to +70°C
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$ or θ_{JA}	95	°C / W
Thermal characterization parameter	Ψ_{JT}	21	°C / W

Note: Junction-to-ambient thermal resistance is based on measurements on a horizontal, single-sided Printed Circuit Board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111) Values were measured with the parts mounted on thermal test boards meeting the specification EIA / JESD51-3.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	1.8	2.0 or 3.3	3.6	V
Input high voltage $\overline{RESET}$, $\overline{SS}$, SCK, MOSI All other inputs	V_{IH}	 $0.75 \times V_{DD}$ $0.7 \times V_{DD}$	 — —	 V_{CC} V_{CC}	 V V
Input low voltage	V_{IL}	—	—	$0.2 \times V_{DD}$	V
Input leakage current	I_{IN}	–0.25	—	0.25	µA
High impedance (off-state) input current (@ 1.44 V / 0.3 V)	I_{TSI}	–10	—	+10	µA
Output high voltage (I_{OH} = –1.0 mA)	V_{OH}	$0.8 \times V_{DD}$	—	—	V
Output low voltage (I_{OL} = 2.8 mA)	V_{OL}	—	—	0.3	V
Internal Supply Current	I_{CC}	—	100	—	µA
Input capacitance	C_{IN}	—	10	—	pF
Note: The Internal Supply Current value is for static I_{CC}.					

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of $0.2 \times V_{DD}$ in V and a V_{IH} minimum of $0.7 \times V_{DD}$ in V for all inputs. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. MC68175 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at $0.3 \times V_{DD}$ in V and $0.6 \times V_{DD}$ in V, respectively.

INITIALIZATION TIMING

(VCC = 1.8 to 3.6 V, TA = –30 to + 85°C)

Table 2-4 Initialization Timing

Characteristic	Conditions	Symbol	Min	Max	Unit
Oscillator Start-up Time	—	t_{START}	—	5	sec
$\overline{\text{RESET}}$ Hold Time	—	t_{RESET}	200	—	ns
$\overline{\text{RESET}}$ High to $\overline{\text{READY}}$ Low	—	t_{RHRL}	76,800	76,800	T
Oscillator Warmed Up to $\overline{\text{READY}}$ Low	C_L = 50pf	t_{OWRL}	—	1	sec
Note: T is one period of the 76.8 kHz clock source. From power-up, the oscillator start-up time can impact the availability and period of clock strobes. This can affect the actual $\overline{\text{RESET}}$ high to $\overline{\text{READY}}$ low timing.					

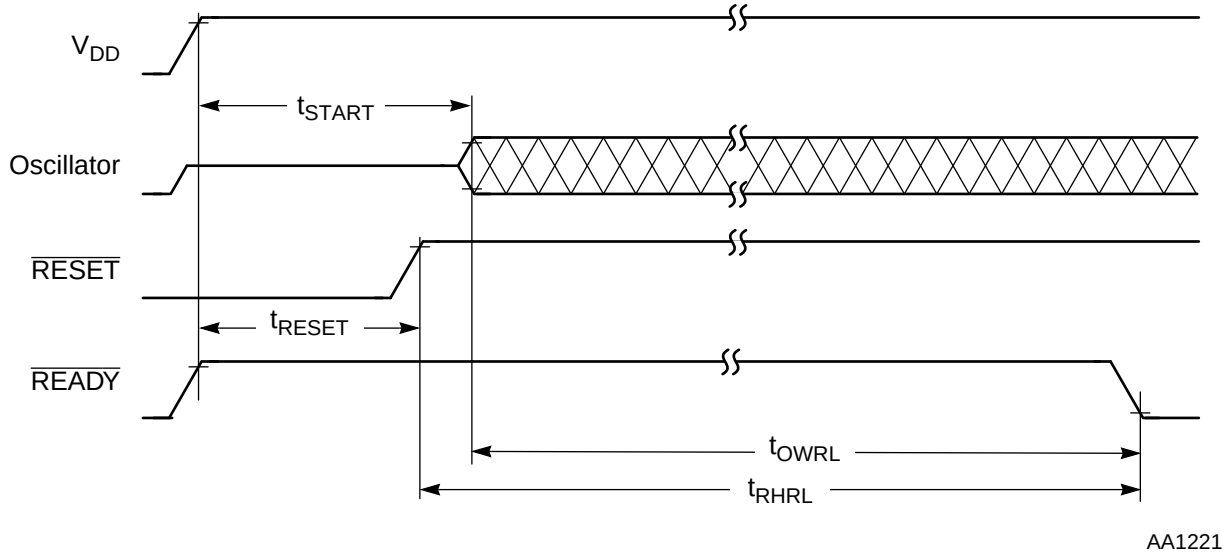


Figure 2-1 Startup Timing

RESET TIMING

(VCC = 1.8 to 3.6 V, TA = –30 to 85°C)

Table 2-5 Reset Timing

Characteristic	Conditions	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ Pulse Width	—	t_{RL}	200	—	ns
$\overline{\text{RESET}}$ Low to $\overline{\text{READY}}$ High	—	t_{RLRH}	—	200	ns
$\overline{\text{RESET}}$ High to $\overline{\text{READY}}$ Low	Requires stable 76.8 kHz clock source	t_{RHRL}	—	1	sec

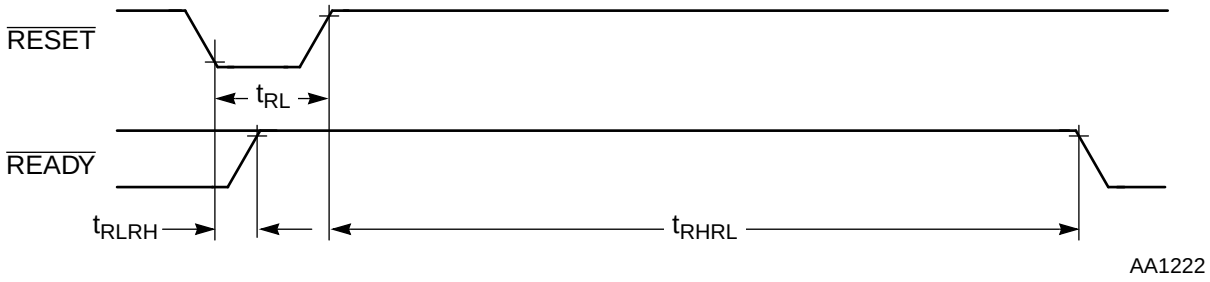


Figure 2-2 Reset Timing

SERIAL PERIPHERAL INTERFACE (SPI) TIMING

(V_{CC} = 1.8 to 3.6 V, T_A = –30 to +85°C)

Table 2-6 SPI Timing

Characteristic	Conditions	Symbol	Min	Max	Unit
Operating Frequency	—	f_{OP}	0	1	MHz
Cycle Time	—	t_{CYC}	1000	—	ns
Select Lead Time	—	t_{LEAD1}	200	—	ns
De-select Lag Time	—	t_{LAG1}	200	—	ns
Select-to-Ready Time	Previous packet did not program an address word; C_L = 50 pf	t_{RDY}	—	80	µs
Select-to-Ready Time	Previous packet programmed an address word; C_L = 50 pf	t_{RDY}	—	420	µs
Ready High Time	—	t_{RH}	50	—	µs
Ready Lead Time	—	t_{LEAD2}	200	—	ns
Not Ready Lag Time	C_L = 50pf	t_{LAG2}	—	200	ns
MOSI Data Setup Time	—	t_{SU}	200	—	ns
MOSI Data Hold Time	—	t_{HI}	200	—	ns
MISO Access Time	C_L = 50pf	t_{AC}	0	200	ns
MISO Disable Time	—	t_{DIS}	—	300	ns
MISO Data Valid Time	C_L = 50pf	t_V	—	200	ns
MISO Data Hold Time	—	t_{HO}	0	—	ns
$\overline{SS}$ High Time	—	t_{SSH}	200	—	ns
SCK High Time	—	t_{SCKH}	300	—	ns
SCK Low Time	—	t_{SCKL}	300	—	ns
SCK Rise Time	20% to 70% V_{DD}	t_R		1	µs
SCK Fall Time	20% to 70% V_{DD}	t_F		1	µs

Note: When the host reprograms an address word with a Host-to-FLEXchip packet ID > 127 (decimal), there may be an added delay before FLEXchip is ready for another packet.

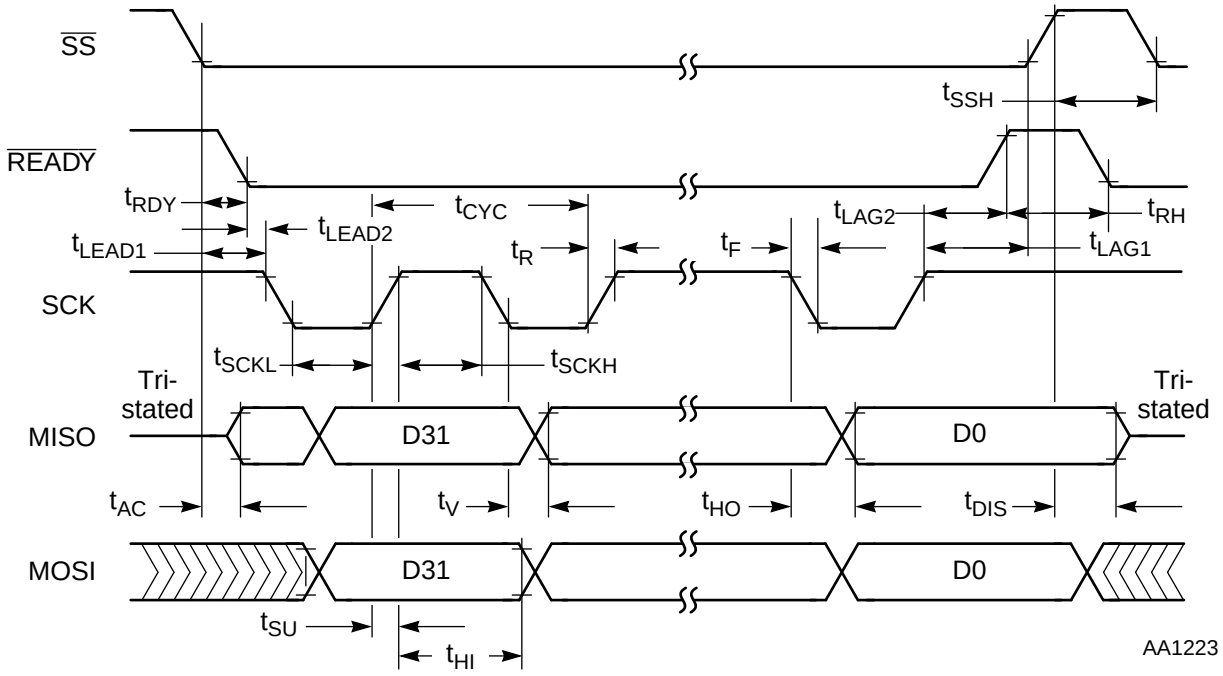


Figure 2-3 SPI Timing

Serial Peripheral Interface (SPI) Timing

SECTION 3

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

This sections provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated. The MC68175 is available in a 32-pin Thin Quad Flat Pack (TQFP) package.

TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

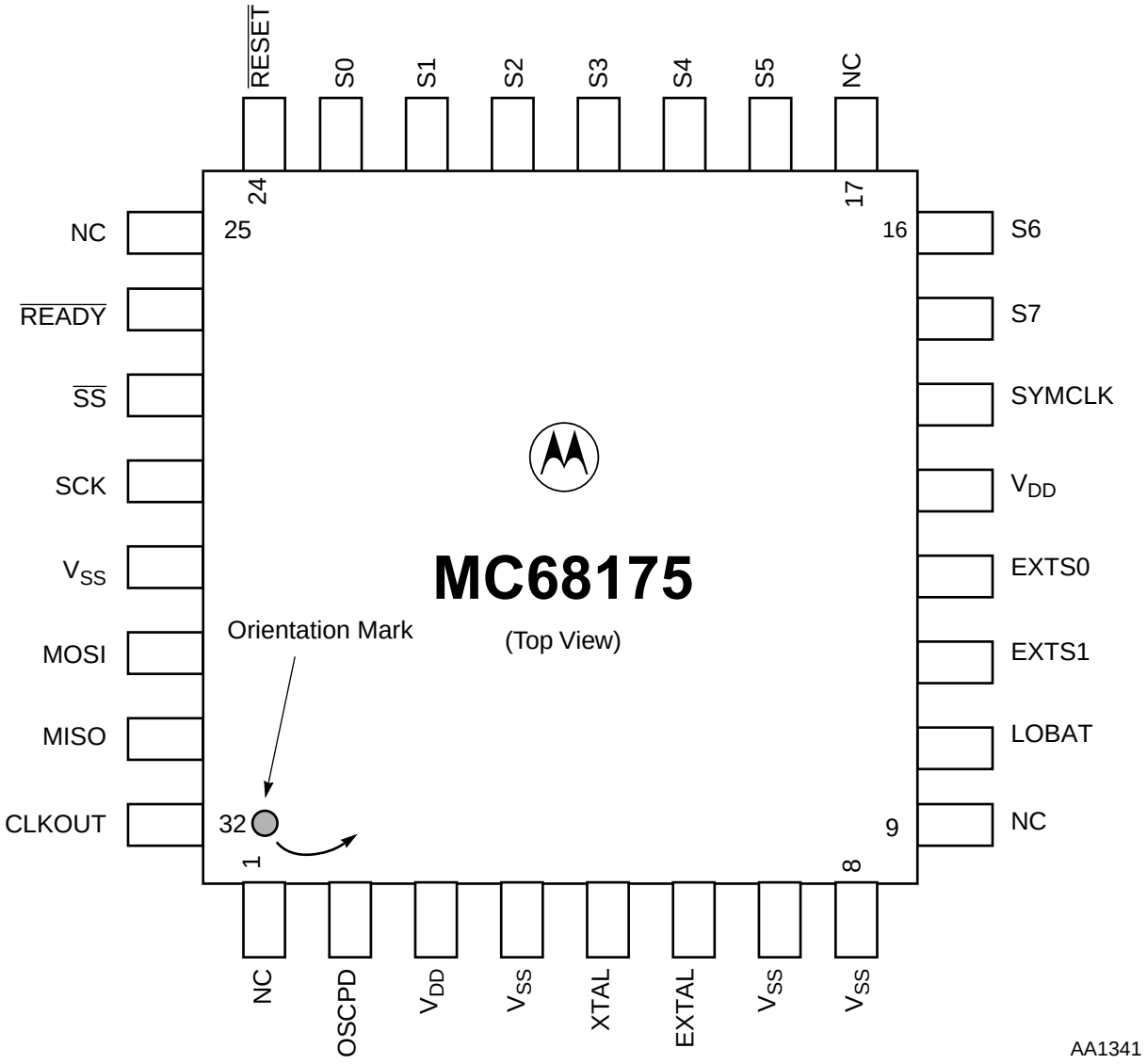


Figure 3-1 MC68175 Thin Quad Flat Pack (TQFP), Top View

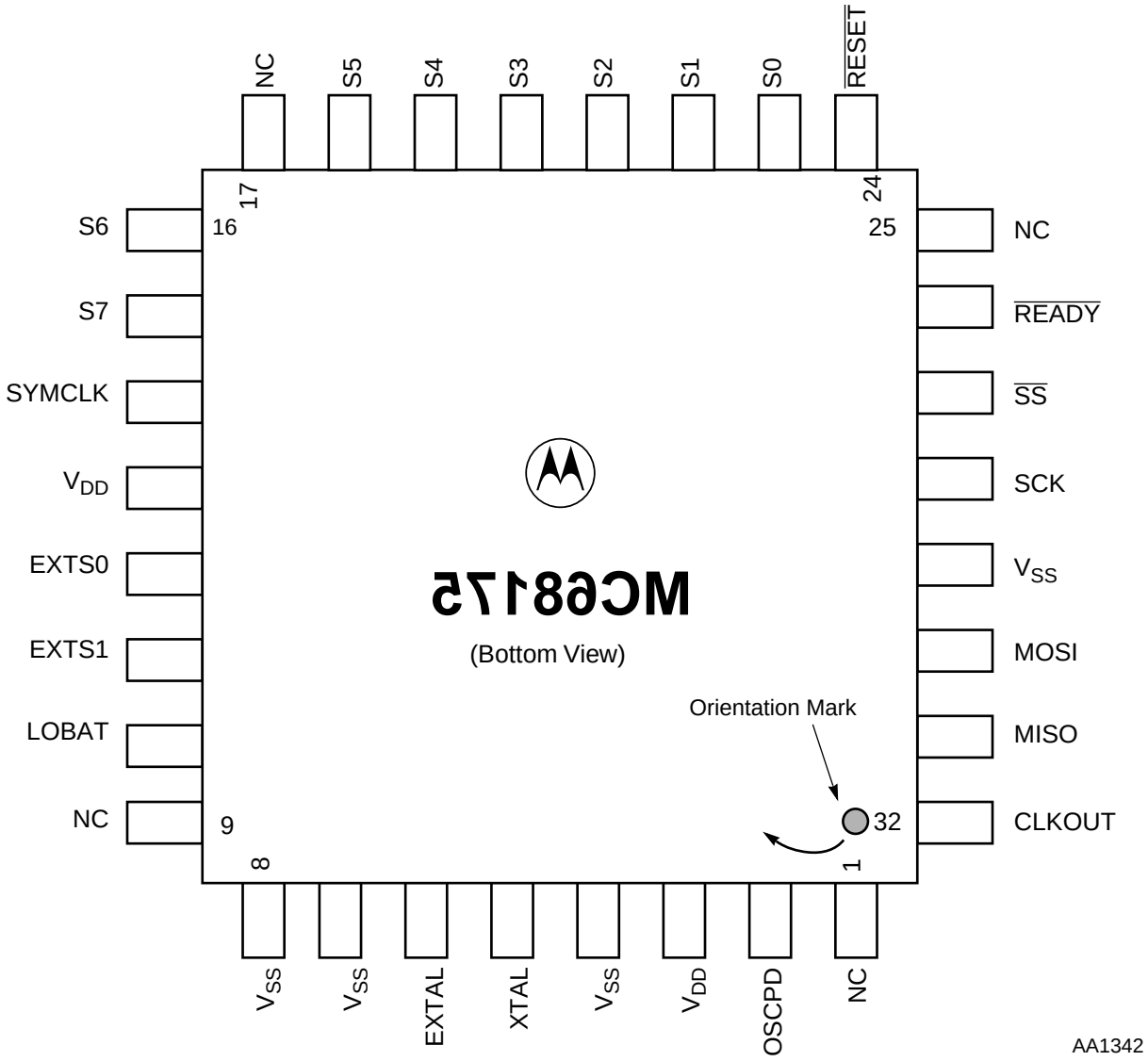


Figure 3-2 MC68175 Thin Quad Flat Pack (TQFP), Bottom View

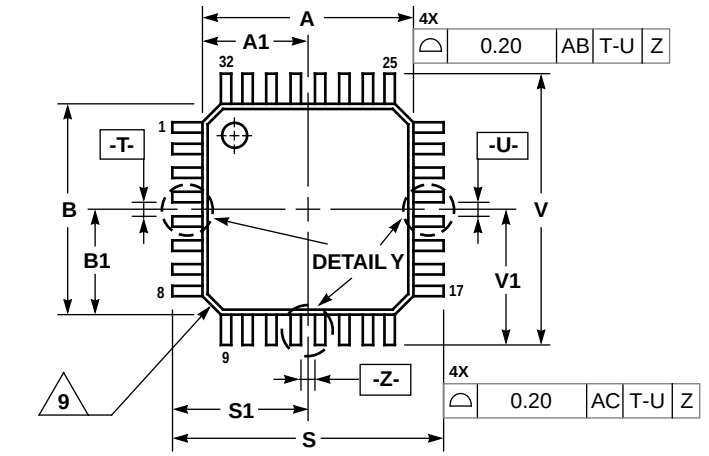
Table 3-1 Signal by Pin Number

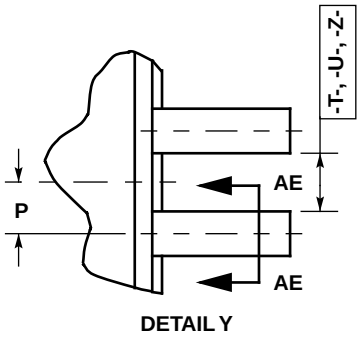
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	NC[1]	9	NC[1]	17	NC[1]	25	NC[1]
2	OSCPD	10	LOBAT	18	S5	26	$\overline{\text{READY}}$
3	V_{DD}	11	EXTS1	19	S4	27	$\overline{\text{SS}}$
4	V_{SS}[2]	12	EXTS0	20	S3	28	SCK
5	XTAL	13	V_{DD}	21	S2	29	V_{SS}[2]
6	EXTAL	14	SYMCLK	22	S1	30	MOSI
7	V_{SS}[2]	15	S7	23	S0	31	MISO
8	V_{SS}[2]	16	S6	24	$\overline{\text{RESET}}$	32	CLKOUT

Notes: 1. NC indicates reserved pins. These pins must not be connected to any external line.
2. To ensure proper chip operation, all V_{SS} pins must be connected to GND.

Table 3-2 Signal by Name

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
CLKOUT	32	NC	9	S2	21	SYMCLK	14
EXTAL	6	NC	17	S3	20	V_{DD}	3
EXTS0	12	NC	25	S4	19	V_{DD}	13
EXTS1	11	OSCPD	2	S5	18	V_{SS}	4
LOBAT	10	$\overline{\text{READY}}$	26	S6	16	V_{SS}	7
MISO	31	$\overline{\text{RESET}}$	24	S7	15	V_{SS}	8
MOSI	30	S0	23	SCK	28	V_{SS}	29
NC	1	S1	22	$\overline{\text{SS}}$	27	XTAL	5





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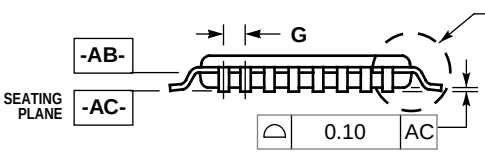

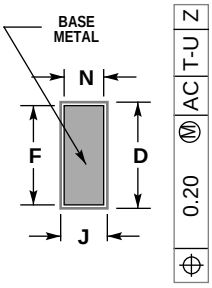

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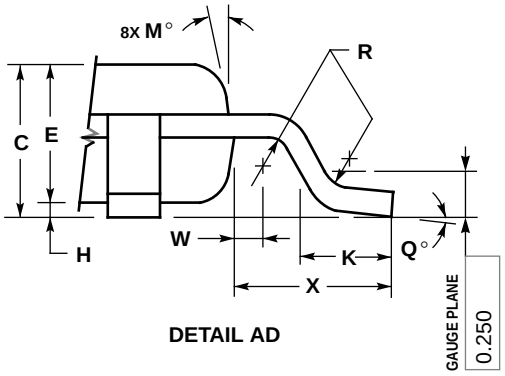


DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.300	0.450
E	1.350	1.450
F	0.300	0.400
G	0.800 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
M	12° REF	
N	0.090	0.160
P	0.400 BSC	
Q	1°	5°
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
X	1.000 REF	

CASE 873A-02
ISSUE A

DATE 12/16/93

Figure 3-3 32-pin Thin Quad Flat Pack (TQFP) Mechanical Information

ORDERING DRAWINGS

Complete mechanical information regarding MC68175 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6609

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The MC68175 32-pin TQFP package mechanical drawing is referenced as 873A-02.

SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C / W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C / W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C / W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C / W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

APPLICATION DESIGN CONSIDERATIONS

The FLEXchip IC connects to a receiver capable of converting a four-level audio signal into a 2-bit digital signal. The FLEXchip IC has eight receiver control lines used for warming up and shutting down a receiver in stages. The FLEXchip IC has dual bandwidth control signals for two post detection filter bandwidths for receiving the two symbol rates of the FLEX signal. The FLEXchip IC has the ability to detect a low battery signal during the receiver control sequences. It interfaces to a host MCU through a standard SPI. It has a 38.4 kHz clock output capable of driving other devices. It has a 1 minute timer that offers low power support for time of day function on the host. **Figure 4-1** shows a typical application block diagram.

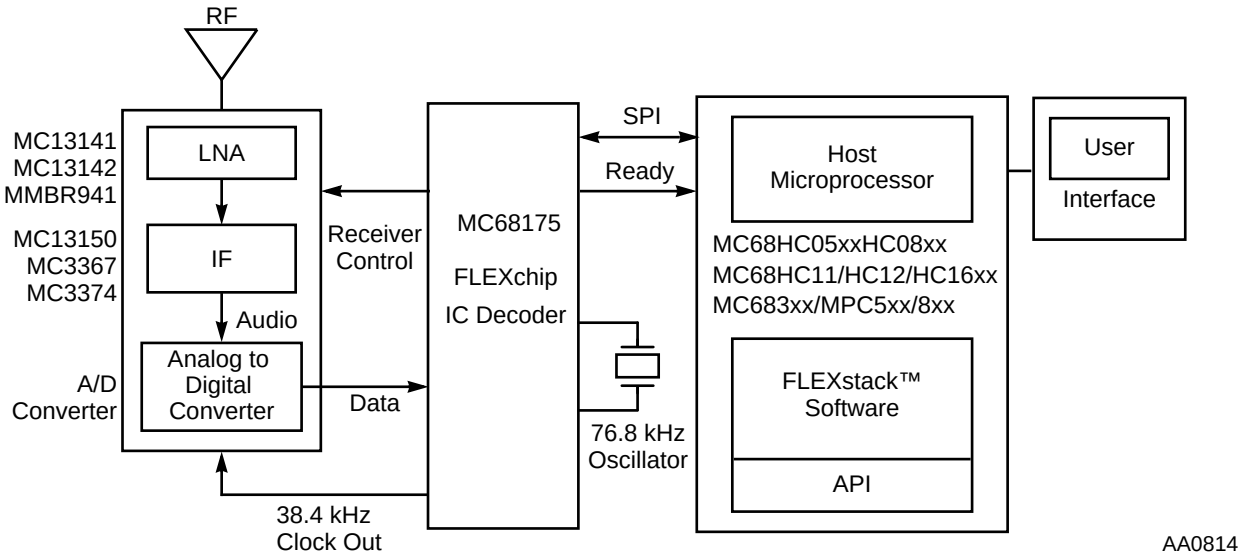
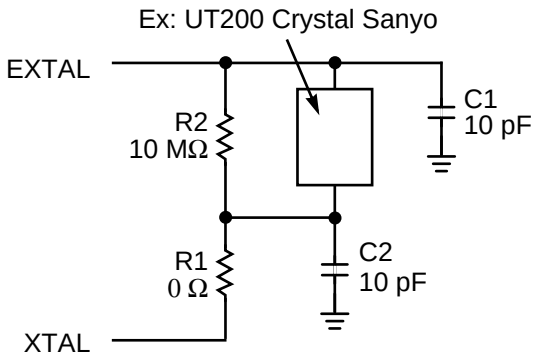


Figure 4-1 FLEXchip System Block Diagram

Figure 4-2 shows a recommended circuit for a 76.8 kHz crystal input.



Note: R1 can be increased in size to be used as a current limiter, if needed. AA1069

Figure 4-2 Input Circuit for 76.8 kHz Crystal

Appendix A of this document provides a background of the FLEX signal protocol. **Appendix B** provides a description of the way in which the MC68175 FLEXchip IC handles packets through the SPI, including sections that describe transfer from the host to the decoder from the decoder to the host. **Appendix C** provides a sample application to illustrate how the MC68175 FLEXchip IC might be used in an application.

SECTION 5

ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
MC68175	2 / 3 V	Thin Quad Flat Pack (TQFP)	32	1	MC68175FA

APPENDIX A

FLEX OVERVIEW

FLEX SIGNAL STRUCTURE

As shown in **Figure A-1**, a FLEX signal is transmitted on a radio channel and consists of a series of four-minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of these frames. Any unassigned frames are not processed, thus reducing power required for signal processing and extending battery life. If required, however, the pager may temporarily process more complex information, because individual FLEX cycles can assign additional frames dynamically using collapse, fragmentation, temporary addressing, or carry-on information within the FLEX signal.

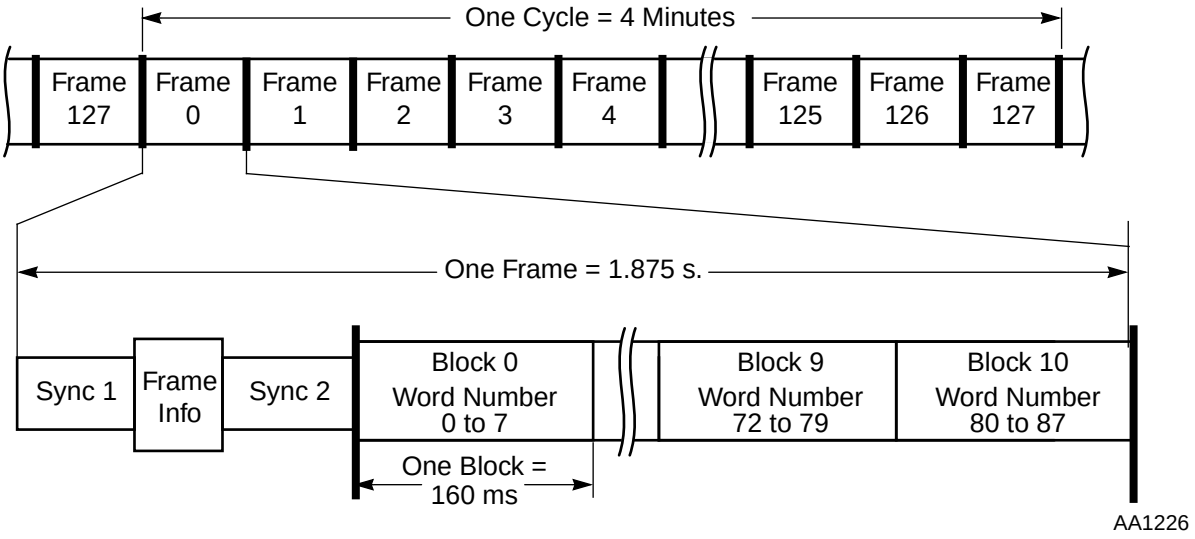


Figure A-1 FLEX™ Signal Structure

FLEX FRAME STRUCTURE

As shown in **Figure A-1** on page A-1, each FLEX frame consists of:

- Synchronization portion
- Data portion—Eleven data blocks lasting 160 milliseconds each

Frame Synchronization Portion

The synchronization portion consists of:

- First synchronization signal at 1600 bps
- Frame Information Word including:
  - Frame Number 0–127 (7 bits)
  - Cycle Number 0–14 (4 bits)
- Second synchronization signal at the data rate of the interleaved portion.

FIRST SYNCHRONIZATION SIGNAL

The first synchronization signal is transmitted at 1600 bps and provides a signal to lock onto the specific frame.

FRAME INFORMATION WORD

The Frame Information Word transmits 11 bits that are divided into a 7-bit frame number and a 4-bit cycle number. This allows the pager to identify the frame and the cycle in which it resides uniquely.

SECOND SYNCHRONIZATION SIGNAL

The second synchronization signal indicates the rate at which the data portion is transmitted, 1600, 3200 or 6400 bits per second.

The 1600 bps rate is transmitted as a single phase of information (A), as shown in **Figure A-2**, at 1600 symbols per second using 2-level Frequency Shift Keyed (FSK) modulation.

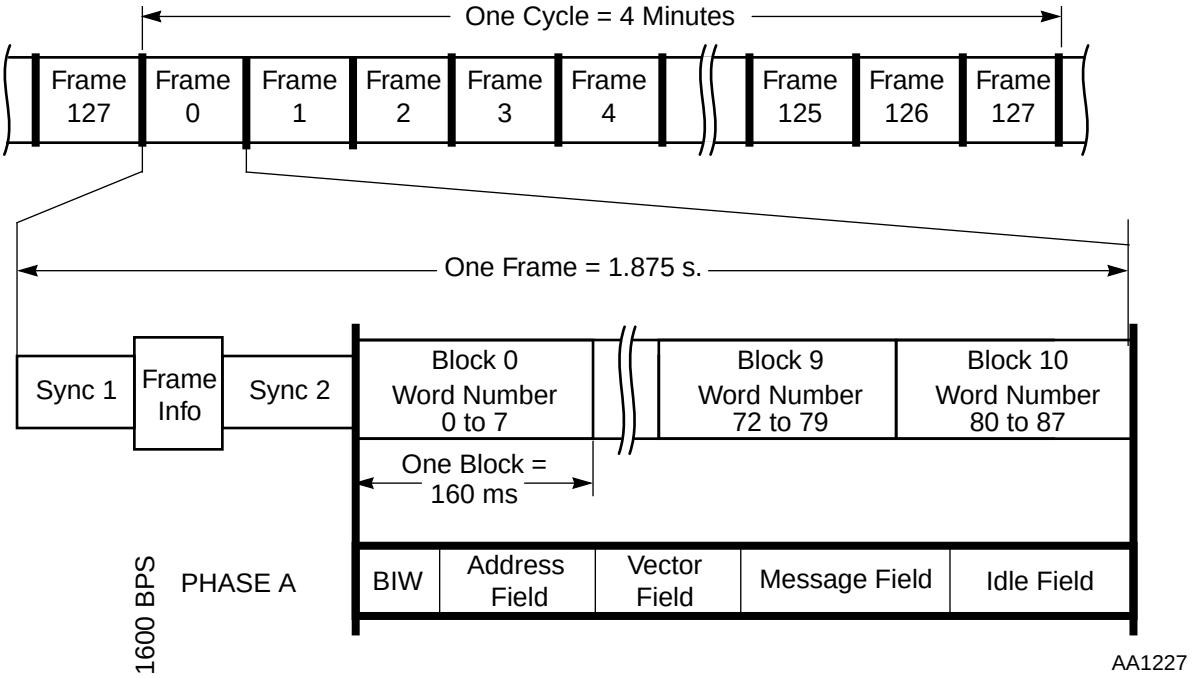


Figure A-2 FLEX™ Signal Structure for 1600 BPS

The 3200 bps rate is transmitted as two concurrent phases of information (A and C), as shown in **Figure A-3**, at either:

- 1600 symbols per second using 4-level FSK modulation, or
- 3200 symbols per second using 2-level FSK modulation.

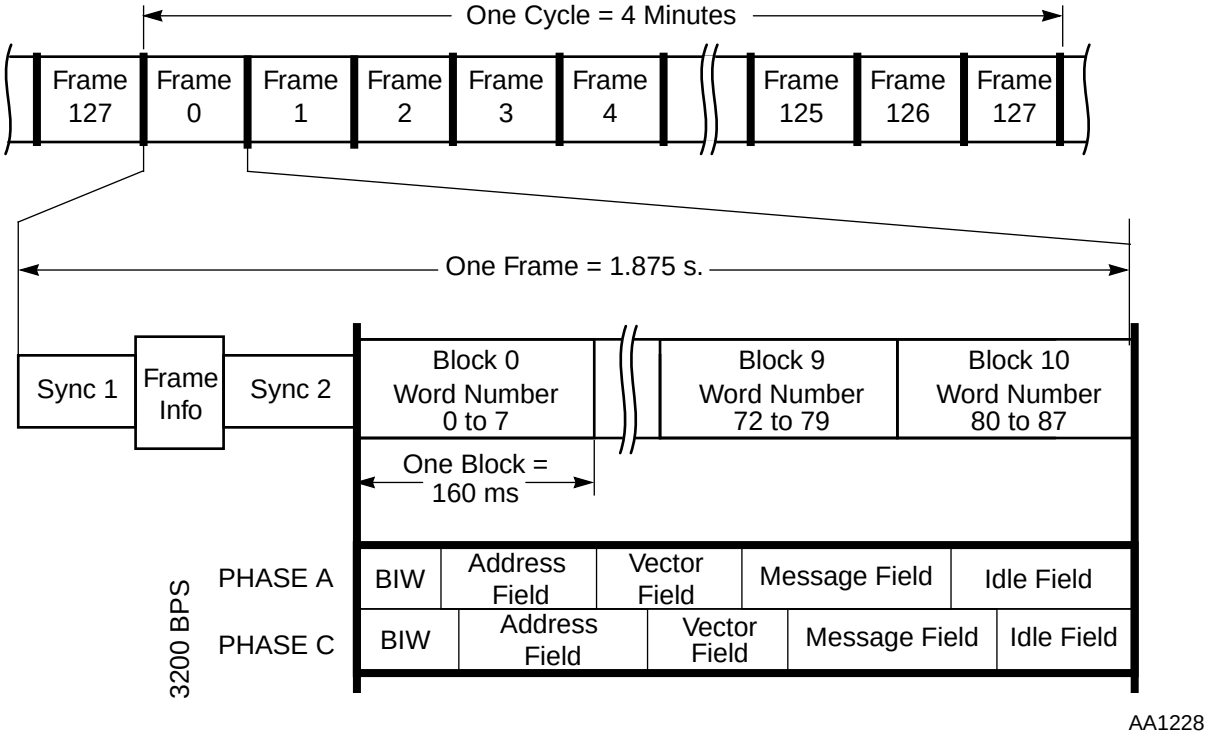


Figure A-3 FLEX™ Signal Structure for 3200 BPS

The 6400 bps rate is transmitted as four concurrent phases of information (A,B, C, and D), as shown in **Figure A-4**, at 3200 symbols per second using 4-level FSK modulation.

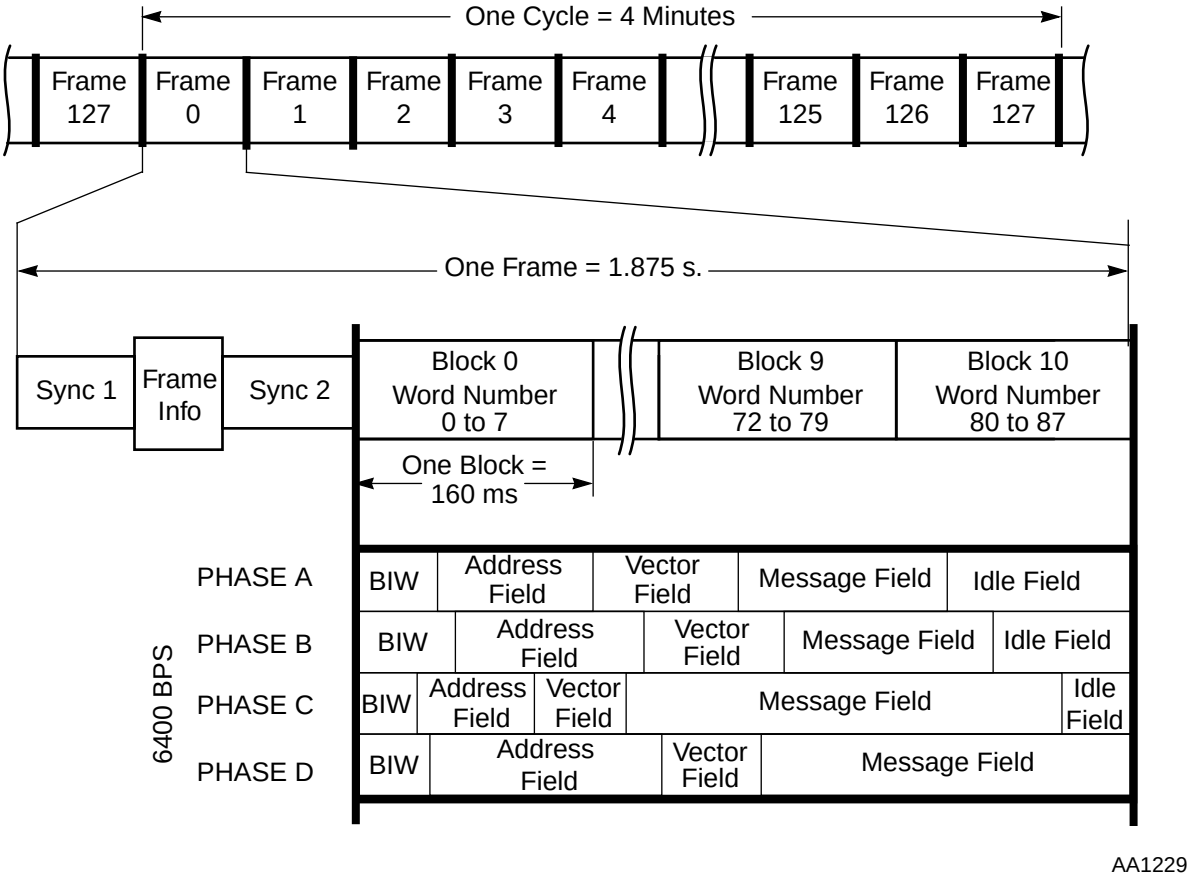


Figure A-4 FLEX™ Signal Structure For 6400 BPS

Frame Data Portion

As noted above, there are eleven data blocks following the frame synchronization portion of each frame. Each block has eight interleaved words per phase, numbered 0–87 contiguously for all eleven blocks, in every frame. Each word has information that allows for bit error correction and detection contained within an error correcting code.

Each of the eighty-eight words in each phase is organized into the following five fields:

- Block information field
- Address field
- Vector field
- Message field
- Idle field

The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

BLOCK INFORMATION FIELD

The block information field may contain information words for determining time and date information and certain paging system information.

ADDRESS FIELD

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. An address may be either a “short” one word address or a “long” two word address. Information in the FLEX signal may indicate that an address is a priority address. An address may be a “tone only” address, in which case there is no additional information associated with the address.

VECTOR FIELD

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information. If an address is not a tone only address, then there is an associated vector word in the vector field. Information in the FLEX signal indicates the location of the vector word. Short addresses have one associated vector word and long addresses two associated vector words. A pager may go to low power mode at the end of the address field if its address(es) is (are) not detected, thus resulting in battery savings.

MESSAGE FIELD

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, BCD, or binary depending upon the message type. The following sections provide a detailed description of the various types of information words that may be used in the message field.

IDLE FIELD

The idle field is used to separate blocks.

FLEX MESSAGE WORD DEFINITIONS

Numeric Data Message

The following tables describe the bit format of the numeric messages. The 4-bit numeric characters of the message are designated as lower case letters a, b, c, d, etc.

Table A-1 Standard (V = 011) or Special Format (V = 100) 4, 10, 15, 20, 25, 31, 36, or 41 Characters

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table A-2 Numbered (V = 111) 2, 8, 13, 18, 23, 29, 34, or 39 Numeric Characters

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

Table A-3 Numeric Message Bit Definitions

Symbol	Definition
K	**6-bit Message Check Character (First 4 bits are in the vector word)**—This check character is calculated by initializing the message check character (**K**) to 0 and summing the information bits of each code word in the message, (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising $\mathbf{i_0}$ through $\mathbf{i_7}$, the second group comprises bits $\mathbf{i_8}$ through $\mathbf{i_{15}}$, and the third group comprises bits $\mathbf{i_{16}}$ through $\mathbf{i_{20}}$. Bits $\mathbf{i_0}$, $\mathbf{i_8}$, and $\mathbf{i_{16}}$ are the LSBs of each group. The binary sum is calculated, and the result is shortened to the eight Least Significant Bits. The two Most Significant Bits are shifted 6 bits to the right and summed with the six Least Significant Bits to form a new sum. This resultant sum is one's complemented with the six LSBs of the result being transmitted as the message check character.
N	**Message Number**—When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at zero and progressing up to a maximum of sixty-three in consecutive order. The actual maximum roll over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (Message Retrieval Flag = 0), it is not to be included in the missed message calculation.

Table A-3 Numeric Message Bit Definitions (Continued)

Symbol	Definition
R	**Message Retrieval Flag**—When this bit is set to 1, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and shall not cause the pager to indicate that a message has been missed.
S	**Special Format**—In the numbered message format, this bit set to 1 indicates that a special display format should be used.

MESSAGE FILL RULES

For numeric messages of thirty-six characters or less (thirty-four characters if numbered), fewer than eight code words on the channel are required. Only code words containing the numeric message are to be transmitted. The space character (hexadecimal C) should be used to fill any unused 4-bit characters in the last word and zeros to fill any remaining partial characters. The check sum is correspondingly shortened to include only the code words comprising the shortened message along with the space and fill characters used to fill in the last word.

SPECIAL FORMAT NUMERIC

Spaces and dashes as specified by the host are inserted into the received message. This feature in certain markets saves the transmission of an additional word on the channel. As an example, in the U.S. market a 10-character string (area code plus telephone number) fits into two message words; if the dashes or parentheses are to be included in the message, a third message word on the channel is required. The actual placement can be programmed into the paging device and can vary between markets.

Hex/Binary Message

The following tables describe the bit format of the Hex/Binary messages. The data of the message is designated as lower case letters a, b, c, d, etc. Hex/binary messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period.

Table A-4 Vector Type V = 110 First Only Fragment

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	R_0	M_0	D_0	H_0	B_0	B_1	B_2	B_3	s_0	s_1	s_2	s_3	s_4	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
3rd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
4th	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
5th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
6th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-5 Vector Type V=110 All Other Fragments

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
3rd	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
4th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
5th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-6 Hex/Binary Message Bit Definitions

Symbol[1]	Definition
K	**12-bit Fragment Check Sum**—This check sum is calculated by initializing the Fragment Check Sum field (**K**) to 0 and calculating a sum over the information bits of each code word in the message fragment (including control information and termination characters/bits in the last fragment word). This sum requires that the information bits of each word be broken into three groups: the first is the 8 bits comprising $\mathbf{i_0}$ through $\mathbf{i_7}$, the second group comprises bits $\mathbf{i_8}$ through $\mathbf{i_{15}}$, and the third group comprises bits $\mathbf{i_{16}}$ through $\mathbf{i_{20}}$. Bits $\mathbf{i_0}$, $\mathbf{i_8}$, and $\mathbf{i_{16}}$ are the LSBs of each group. The binary sum is calculated over all code words in the fragment, the one's complement of the sum is determined, and the twelve LSBs of the result is placed into the Fragment Check Sum field to be transmitted at the beginning of the fragment.
C	**1-bit Message Continued Flag**—When set to 1, this flag indicates fragments of this message are to be expected in any or possibly all of the following frames until a fragment with C = 0 is found. The longest message that fits into a frame is eighty-four code words. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.
F	**2-bit Message Fragment Number**—This is a modulo 3 message fragment number that is incremented by 1 in successive message fragments. The initial fragment starts at 11 and each following fragment is incremented by 1 modulo 3, (11, 00, 01, 10, 00, 01, 10, 00, etc.). The 11 state (after the initial fragment) is skipped in this process to avoid confusion with the single fragment of a non-continued message. The final fragment is indicated by the Message Continued Flag being reset to 0.
N	**Message Number**—When the system supports message retrieval the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum roll over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers. An exception to this rule is the header message tied to a transparent message, each with the same message number.
R	**Message Retrieval Flag**—When this bit is set to 1, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with **R** = 0 is allowed to be out of order and not cause the pager to indicate that a message has been missed.
M	**1-bit Mail Drop Flag**—When set to 1, this bit indicates the message is to be stored in a special area in memory. It automatically writes over existing data in that memory space.

Table A-6 Hex/Binary Message Bit Definitions (Continued)

Symbol[1]	Definition
D	**1-bit Display Direction Field**— • **D** = 0—Display left to right • **D** = 1—Display right to left (valid only when data sent as characters (i.e., Blocking Length not equal 0001)).
H	**1-bit Header Message**— • **H** = 1—Indicates that this message is a header to a following transparent message of the same message number • **H** = 0—Implies message is not a header
B	**4-bit Blocking Length**—This bit field indicates the number of bits per character. • $\mathbf{B_3B_2B_1B_0}$ = 0001—1 bit per character (binary/transparent data) • $\mathbf{B_3B_2B_1B_0}$ = 1111—15 bits per character • $\mathbf{B_3B_2B_1B_0}$ = 0000—16 bits per character Data with blocking length other than 1 is assumed to be displayed on a character by character basis. (default value = 0001)
s	**5-bit Field Reserved for future use**—Default value = 00000
S	**8-bit Signature Field**—The signature is defined to be the one's complement of the binary sum over the total message taken 8 bits at a time prior to formatting into fragments. It would be equivalent to a binary sum starting with the first 8 bits directly following the signature field ($\mathbf{b_3b_2b_1b_0a_3a_2a_1a_0}$ + $\mathbf{d_3d_2d_1d_0c_3c_2c_1c_0}$ and so on) and continuing all the way to the last valid data bit in the last word of the last fragment. The 8 Least Significant Bits of the result are inverted (one's complement) and transmitted as the message signature.[2]

Notes:
1. Fields **R** through **S** are only in the first fragment of a message. The fields **K** through **N** make up the first word of every fragment in a long message.
2. This sum does not include any termination bits and should be calculated directly on the message as received by the terminal. The device generating the signature should be able to calculate before the fragmenting boundaries are determined.

MESSAGE CONTENT

Starting with the first character of the third word in the message (second word in the remaining fragments), each 4-bit field represents one of any of the sixteen possible combinations with no restrictions (data may be binary).

FRAGMENT TERMINATION

Unused bits in the last message word of a fragment are filled with all 0s or all 1s, depending on the last valid data bit. This choice is always the opposite polarity of the last valid data bit. For first fragments and inner fragments of a multi-fragment message, the message is interrupted (stopped) on the last full character boundary in the last code word in the fragment. Any unused bits follow the rule just stated. The final fragment follows the above rules except when the last character is all 1s or all 0s and it exactly fills the last code word. In this case, an additional word must be sent of

opposite polarity of all 1s or all 0s to signify the position of the last character, thus allowing that last character to be an all 1s or an all 0s character pattern.

Note: This is always the case when a binary message ends in the last bit of the last word.

MESSAGE HEADER

A message header is designated by setting the **H** bit to 1. This is a displayable tag associated with a transparent non-displayable data message. The tag and the associated message are complete in themselves. The pager associates the header message with the data file based on the two having the same message number and being sent in sequence (header first followed by data file).

Alphanumeric Message

The following tables describe the bit format of the alphanumeric messages. The 7-bit characters of the message are designated as lower case letters a, b, c, d, etc. Alphanumeric messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period.

Table A-7 Vector type V=101 First Only Fragment

Message Word	**i_0**	**i_1**	**i_2**	**i_3**	**i_4**	**i_5**	**i_6**	**i_7**	**i_8**	**i_9**	**i_{10}**	**i_{11}**	**i_{12}**	**i_{13}**	**i_{14}**	**i_{15}**	**i_{16}**	**i_{17}**	**i_{18}**	**i_{19}**	**i_{20}**
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	R_0	M_0
2nd	S_0	S_1	S_2	S_3	S_4	S_5	S_6	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6
3rd	c_0	c_1	c_2	c_3	c_4	c_5	c_6	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6
4th	f_0	f_1	f_2	f_3	f_4	f_5	f_6	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6
5th	i_0	i_1	i_2	i_3	i_4	i_5	i_6	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-8 Vector type V=101 Other Fragment

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	U_0	V_0
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-9 Alphanumeric Message Bit Definitions

Symbol	Definition
K	**10-bit Fragment Check Character**—This check character is calculated by initializing the fragment check character (**K**) to 0 and summing the information bits of each code word in the message fragment (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising $\mathbf{i_0}$ through $\mathbf{i_7}$, the second group comprises bits $\mathbf{i_8}$ through $\mathbf{i_{15}}$, and the third group comprises bits $\mathbf{i_{16}}$ through $\mathbf{i_{20}}$. Bits $\mathbf{i_0}$, $\mathbf{i_8}$, and $\mathbf{i_{16}}$ are the LSBs of each group. The binary sum is calculated, the one's complement of the sum is determined, and the ten LSBs of the result is transmitted as the message check character.
C	**1-bit Message Continued Flag**—When set, this flag indicates fragments of this message are to be expected in following frames. The longest message that fits into a frame is 84 code words total. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.
F	**2-bit Message Fragment Number**—This is a modulo 3 message fragment number that is incremented by 1 in successive message fragments. Initial fragments start at 11 and increment 1 for each successive fragment. The 11 state (after the start fragment) is skipped in this process to avoid confusion with an initial fragment of a non-continued message. The final fragment is indicated by Message Continued Flag being cleared.

Table A-9 Alphanumeric Message Bit Definitions (Continued)

Symbol	Definition
N	**Message Number**—When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum roll over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s), allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.
R	**Message Retrieval Flag**—When this bit is set, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with **R** = 0 is allowed to be out of order and not cause the pager to indicate that a message has been missed.
M	**1-bit Mail drop Flag**—When set, this flag indicates the message is to be stored in a special area in memory. It automatically writes over existing data in that memory space.
S	**7-bit Signature Field**—The signature is defined to be the one's complement of the binary sum over the total message (all fragments) taken 7 bits at a time (on alpha character boundary) starting with the first 7 bits directly following the signature field (a6a5a4a3a2a1a0, b6b5b4b3b2b1b0, etc.). The seven Least Significant Bits of the result are transmitted as the message signature.
U, **V**	**Fragmentation control bits**—This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (characters made up of 1, 2, or 3 ASCII characters) are transmitted using the Alphanumeric message type. The default value for the U, V pair is 0, 0. See **Enhanced Fragmentation Rules** on page A-16 for more information.

MESSAGE CONTENT

Starting with the second character of the second word in the message (1st character of the second word in all remaining fragments), each 7-bit field represents Standard ASCII (ISO 646-1983E) characters with options for certain International characters.

MESSAGE TERMINATION

The ASCII character ETX (03) should be used to fill any unused 7-bit characters in a word. In the case where symbolic characters are being transmitted, special rules for fragment and message termination are defined in the following information on Alphanumeric Message Rules for Symbolic Characters Sets.

ALPHANUMERIC MESSAGE RULES FOR SYMBOLIC CHARACTERS SETS

In the past, paging protocols have supported symbolic characters (e.g., Chinese, Kanji, etc.) using a 7-bit ASCII protocol. When the FLEX Alphanumeric mode is used to carry this same signaling format, special fragmenting rules are required to maintain character boundaries, so performance is optimized under poor signal conditions. The following rules allow character positions within a fragment to be determined when prior fragments are missing.

ENHANCED FRAGMENTATION RULES

- The pager must recognize <NUL> characters only at the end of fragments where they are used as fill characters. The pager must remove these characters so that the displayed message is not affected. In all other positions the NUL character must be considered a result of channel errors. (This provides a method to end each fragment with a complete character and does not disrupt the pager that is not capable of following all of the EF (Enhanced Fragmenting) rules.)
- The last fragment is to be completed by filling unused character positions with <ETX> characters or <NUL> characters. (Original FLEX alphanumeric message definition (<ETX>) plus the new <NUL> requirement.) When the message ends exactly in the last character position in the last BCH codeword, no additional <ETX> is required.
- The **U** and **V** bits in the message header are available in all fragments following the initial fragment to aid in decoding. In the first fragment, the pager must assume the message starts in the default Character mode. For the second and remaining fragments, the definition of the (**U,V**) field is as shown in the following table.

Table A-10 U and V Field Definition

U_0	V_0	Definition
0	0	EF not supported in controller
0	1	Reserved (for a second alternate character mode)
1	0	Default Character Mode—start position 1
1	1	Alternate Character Mode—start position 1

When the EF field is 00, the pager decodes messages, allowing characters to be split between fragments. When the **U, V** field is not 0, 0, each fragment starts on a character boundary with the character mode defined by the above table.

SECURE MESSAGE

The following tables describe the bit format of the secure messages. The 7-bit characters of the message are designated as lower case letters a, b, c, d, etc. Secure messages can be sent as fragments. The service provider has the option of dividing

the message into several pieces and sending the separate pieces at any time within a given time period.

Table A-11 Vector type V = 000 All Fragments

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	s_0	s_1
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-12 Secure Message Bit Definitions

Symbol	Definition
K	**10-bit Fragment Check Character**—This check character is calculated by initializing the fragment check character (**K**) to 0 and summing the information bits of each code word in the message fragment (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising $\mathbf{i_0}$ through $\mathbf{i_7}$, the second group comprises bits $\mathbf{i_8}$ through $\mathbf{i_{15}}$, and the third group comprises bits $\mathbf{i_{16}}$ through $\mathbf{i_{20}}$. Bits $\mathbf{i_0}$, $\mathbf{i_8}$, and $\mathbf{i_{16}}$ are the LSBs of each group. The binary sum is calculated, the one's complement of the sum is determined, and the ten LSBs of the result is transmitted as the message check character.
C	**1-bit Message Continued Flag**—When set, the Message Continued Flag indicates fragments of this message are to be expected in following frames. The longest message that fits into a frame is 84 code words total. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.
F	**2-bit Message Fragment Number**—This is a modulo 3 message fragment number that is incremented by 1 in successive message fragments. Initial fragments start at 11 and increment 1 for each successive fragment. The 11 state (after the start fragment) is skipped in this process to avoid confusion with an initial fragment of a non-continued message. The final fragment is indicated by Message Continued Flag being cleared.

Table A-12 Secure Message Bit Definitions

Symbol	Definition
N	**Message Number**—When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum roll over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.
s	**Spare Bit**—not used and set to 0

MESSAGE CONTENT

Starting with the first character of the second word in the message (and 1st character of all remaining fragments), each 7-bit field represents Standard ASCII (ISO 646-1983E) characters with options for certain International characters.

MESSAGE TERMINATION

The ASCII character ETX (03) should be used to fill any unused 7-bit characters in a word.

FLEX Encoding and Decoding Rules

The encoding and decoding rules identify the minimum requirements that must be met by the paging device, paging terminal, or other encoding equipment to properly format a FLEX data stream for RF transmission and to successfully decode it.

FLEX ENCODING RULES

- The stability of the encoder clock used to establish time positions of FLEX frames must be no worse than ±25 ppm (including worst case temperature and aging effects).
- A maximum of two occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multi-phase frame. For example, for decoding devices that support any-phase addressing, an any-phase address may appear at once in two different phases in a single multi-phase frame.
- Once an individual or radio group address is used to begin transmitting a fragmented message, that same address must not be used to start a new

fragmented transmission until the first fragmented transmission has been completed.

- For the duration of time that an individual or radio group address is being used to send a fragmented message, that same address must not appear more than once in any frame to send an unfragmented message.
- Once a specific dynamic group address (temporary address) is assigned to a group, it must not be reused until its associated message has been transmitted in its entirety. Given this constraint, the same dynamic group address can only appear once in any frame.
- A dynamic group address cannot be used to set up a second dynamic group.
- Messages using any of the three defined numeric vectors ($V_2V_1V_0$ = 011, 100, and 111) cannot be fragmented, and thus must be completely contained in a single frame.
- Fragments of the same message must be sent at a frequency of at least 1 every 32 frames (i.e., at least once a minute) or 1 every 128 frames (i.e., at least once every 4 minutes) as specified by the service provider.
- Enhanced message fragmenting for symbolic character transmission requires that the encoder track character boundaries within each fragment in order to avoid character splitting.
- Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.
- Message numbers must be assigned sequentially in ascending order.
- Message number sequences must be separately maintained for each individual and radio group address.
- Message numbers are not used (retrieval message number disabled) in conjunction with a dynamic group address.
- When a missed message is re-transmitted from message retrieval storage, the message must have R = 0 to avoid creating an out of sequence message that may cause the pager to indicate a missed message.

FLEX DECODING RULES

- FLEX decoding devices may implement either single-phase addressing or any-phase addressing.
- FLEX decoding devices that support the numeric vector type ($V_2V_1V_0$ = 011) must also support the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00.
- FLEX decoding devices that support the alphanumeric vector type ($V_2V_1V_0$ = 101) must support the numeric vector type ($V_2V_1V_0$ = 011) and the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00. FLEX paging devices that implement any-phase and support the alphanumeric

vector type ($V_2V_1V_0$ = 101) must also support the short instruction vector ($V_2V_1V_0$ = 001) with the instruction type ($i_2i_1i_0$) set to 000.

- FLEX decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode. They are: 1600 bps, 2 level; 3200 bps, 2 level; 3200 bps, 4 level; 6400 bps, 4 level.
- FLEX decoding devices must be designed to tolerate 4 minute fragment separation times.

FLEX Character Sets and Rules

ALPHANUMERIC CHARACTER SET

The following tables define the characters to be displayed in the FLEX Alphanumeric Message mode. Control characters that are not acted upon by the pager are ignored in the display process (do not require display space), but are stored in memory for possible download to an external device.

Table A-13 Alphanumeric Character Set

Least Significant 4 bits of character	Most Significant 3 bits of character							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	NUL	DLE	SP	0	@	P	‘	p
1	SOH	DC1	!	1	a	q	a	q
2	STX	DC2	“	2	b	r	b	r
3	ETX	DC3	#	3	c	s	c	s
4	EOT	DC4	$	4	d	t	d	t
5	ENQ	NAK	%	5	e	u	e	u
6	ACK	SYN	&	6	f	v	f	v
7	BEL	ETB	’	7	g	w	g	w
8	BS	CAN	(	8	h	x	h	x
9	TAB	EM	)	9	i	y	i	y
A	LF	SUB	*	:	j	z	j	z
B	VT	ESC	+	;	k	[	k	{
C	FF	FS	,	<	l	\	l	|

Table A-13 Alphanumeric Character Set (Continued)

Least Significant 4 bits of character	Most Significant 3 bits of character							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
D	CR	GS	–	=	m	]	m	}
E	SO	RS	.	>	n	^	n	~
F	SI	US	/	?	o	_	o	DEL

NUMERIC CHARACTER SET

The following tables define the characters to be displayed in the FLEX Numeric Message mode.

Table A-14 Standard Character Set (Peoples Republic of China Option Off)

Character	B_3	B_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
Spare	1	0	1	0
U	1	0	1	1
Space	1	1	0	0
-	1	1	0	1
]	1	1	1	0
[	1	1	1	1

Table A-15 Alternate Character Set (Peoples Republic of China Option On)

Character	B_3	B_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
Space	1	1	0	0
C	1	1	0	1
D	1	1	1	0
E	1	1	1	1

FLEX Local Time And Date

The FLEX protocol allows for systems to transmit time information in its Block Information Field. When a system provider supports local time transmissions, the system provider is required, at a minimum, to transmit at least one time related block information word in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of Sync 1 of Frame 0 of the current cycle. The information carried in the **s** bits of the block information word depend on the value of the **f** bits of the block information word. The following sections describe the bit definitions of the time related block information words.

MONTH/DAY/YEAR

Table A-16 Month / Day / Year Block Information Word Definition

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0
001	m_3 m_2 m_1 m_0 d_4 d_3 d_2 d_1 d_0 Y_4 Y_3 Y_2 Y_1 Y_0
Note:	**m = Month field**—0001 through 1100 (binary) correspond to January through December, respectively **d = Day field**—00001 through 11111 (binary) correspond to 1 through 31, respectively **Y = Year field**—This represents the year with modulo arithmetic. 00000 through 11111 (binary) representing 1994 through 2025, 2026 through 2057, etc.

SECOND/MINUTE/HOUR

Table A-17 Second / Minute / Hour Block Information Word Definition

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0
010	S_5 S_4 S_3 M_5 M_4 M_3 M_2 M_1 M_0 H_4 H_3 H_2 H_1 H_0
Note:	**S = Second field**—This represents a coarse value of the seconds field. These bits represent the seconds in eighth of a minute (7.5 second) increments. 000 through 111 (binary) correspond to 0 through 52.5 seconds, respectively **M = Minute field**—000000 through 111011 (binary) correspond to 0 through 59, respectively **H = Hour field**—00000 through 10111 (binary) correspond to 0 through 23, respectively.

ACCURATE SECONDS/DAYLIGHT SAVINGS TIME/TIME ZONE

Table A-18 System Message Block Information Word Definition

$f_2f_1f_0$	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	Description
101	S_2	S_1	S_0	x	L_0	z_4	z_3	z_2	z_1	z_0	0	1	0	X	System Message[1]

Notes:
1. When the $s_3\ s_2\ s_1\ s_0$ field is set to 0100 or 0101, the other s_4 through s_{13} are defined as above. The system messages with the $s_3\ s_2\ s_1\ s_0$ field set to some other value do not contain time related information.
2. **S = Accurate Seconds**—This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents how much time should be added to the coarse seconds in sixty-fourth of a minute increments.
   L = Daylight Savings Time—When this bit is set, the time being transmitted is local standard time. When it is clear, the time being transmitted is Daylight Savings Time.
   z = Time Zone—These bits indicate the time zone for which the time is being transmitted. The offset from GMT is the offset for local standard time. The following table describes the values for **z**.

Table A-19 Time Zone Values

$z_4z_3z_2z_1z_0$	Time Zone
00000	GMT
00001	GMT + 0100
00010	GMT + 0200
00011	GMT + 0300
00100	GMT + 0400
00101	GMT + 0500
00110	GMT + 0600
00111	GMT + 0700
01000	GMT + 0800
01001	GMT + 0900
01010	GMT + 1000

$z_4z_3z_2z_1z_0$	Time Zone
01011	GMT + 1100
01100	GMT + 1200
01101	GMT + 0330
01110	GMT + 0430
01111	GMT + 0530
10000	RESERVED
10001	GMT + 0545
10010	GMT + 0630
10011	GMT + 0930
10100	GMT – 0330
10101	GMT – 1100

$z_4z_3z_2z_1z_0$	Time Zone
10110	GMT – 1000
10111	GMT – 0900
11000	GMT – 0800
11001	GMT – 0700
11010	GMT – 0600
11011	GMT – 0500
11100	GMT – 0400
11101	GMT – 0300
11110	GMT – 0200
11111	GMT – 0100

FLEX CAPCODES

In order to send messages to a FLEX decoding device, the FLEX service provider must know the device's address, the address type (single-phase, any-phase, or all-phase), the address's assigned phase, the address's assigned frame, and the address's battery cycle. This information is typically included in a FLEX CAPCODE. The assignment of CAPCODEs is regulated to prevent duplication of addresses on a system. Check with your FLEX service provider or other appropriate regulatory body for FLEX CAPCODE assignments. The following paragraphs describe what these parameters define.

The device address consists of one or two 21-bit words. A one-word address is called a short address, while a two-word address is called a long address. Address words are separated into ranges according to the following table

Table A-20 Address Word Range Definition

Type	Hexadecimal Value
Idle Word (Illegal Address)	000000
Long Address 1	000001–008000
Short Address	008001–1E0000
Long Address 3	1E0001–1E8000
Long Address 4	1E8001–1F0000
Short Address (Reserved)	1F0001–1F27FF
Info Service Address	1F2800–1F67FF
Network Address	1F6800–1F77FF
Temporary Address	1F7800–1F780F
Operator Messaging Address	1F7810–1F781F
Short Address (Reserved)	1F7820–1F7FFE
Long Address 2	1F7FFF–1FFFFE
Idle Word (Illegal Address)	1FFFFF

Long addresses are grouped into the sets listed in **Table A-21**.

Table A-21 Long Address Sets

Long Address Set	First Word	Second Word
1–2	Long Address 1	Long Address 2
1–3	Long Address 1	Long Address 3
1–4	Long Address 1	Long Address 4
2–3	Long Address 2	Long Address 3
2–4	Long Address 2	Long Address 4

The address type indicates how messages on a particular address can be delivered in multi-phase FLEX frames. Messages sent on single-phase addresses can only be delivered in a particular phase (a, b, c, or d). Messages sent on any-phase addresses can be delivered in any phase, but a single message is limited to a single phase per frame. Messages sent on all-phase addresses can be delivered in any phase, and a single message can be spread across multiple phases in a single frame. All-phase messaging is a future feature of FLEX and has not been completely defined.

The assigned phase is required only for single-phase devices. It determines the phase (a, b, c, or d) in which the messages is sent.

The assigned frame and battery cycle determine the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The battery cycle is a number between 0 and 7 and defines how often the decoding device looks for messages on the FLEX channel. For a given battery cycle, b, the decoding device looks in every 2^b frames. Thus, an address with an assigned frame of 3 and a battery cycle of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e., frames 3, 35, 67, and 99).

The FLEX CAPCODE is defined to represent either a short or a long address. The short address is defined in the FLEX protocol as one code word on the RF channel and is represented by a 7-digit decimal field. The long address is defined in the FLEX protocol as two code words on the RF channel and is represented by a 9- or 10-digit decimal field. The long addresses in set 1–2 are represented by a 9-digit decimal field. The long addresses in sets 1–3, 1–4, 2–3, and 2–4 are represented by a 10-digit decimal field. An alphabetic character known as the “CAPCODE type” always precedes the 7-, 9-, or 10-digit decimal address field. The CAPCODE type indicates the type of address and distinguishes FLEX CAPCODEs from CAPCODEs of other paging protocols.

CAPCODE TYPE

Example CAPCODEs are shown in **Table A-22**. The CAPCODE type can be any of "A" through "L" or "U" through "Z". The CAPCODE types "A" through "L" indicate that the standard rules are used to derive the assigned frame and phase information from the address field. (See **Standard Frame and Phase Embedding Rules** on page A-28.) For these CAPCODE types, the battery cycle (indicated as a "b" in *Example 1*) is indicated by a single decimal digit "0" through "7" preceding the CAPCODE type. When the FLEX standard battery cycle of 4 (16-frame cycle) is used, the battery cycle digit is not required (see *Example 2* in **Table A-22**).

The CAPCODE types "U" through "Z" indicate that the standard frame and phase embedding rules were not used and additional information is required. The phase assignment can be derived from the CAPCODE type, as described in **Table A-23** on page A-28. The 3-digit decimal frame assignment "000" through "127" (indicated by "fff" in example 3) and single digit decimal battery cycle "0" through "7" (indicated as a "b" in *Example 3* in **Table A-22**) may precede this CAPCODE type. The frame and battery cycle fields are not required. When they are not included (see *Example 4* in **Table A-22**), the paging device or the subscriber database must be accessed to determine the assigned frame and battery cycle.

The extended CAPCODE is a regular CAPCODE with a 10-digit address field and preceded by an extra alphabetic character "P" through "S". These CAPCODEs are used to provide additional information required for roaming devices.

Table A-22 FLEX CAPCODE Examples

Example	Short	Long	Extended
1	**bA**1234567	**bA**123456789	**RbA**1234567890
2	**A**1234567	**A**123456789	**RA**1234567890
3	**fffbU**1234567	**fffbU**123456789	**RfffbU**1234567890
4	**U**1234567	**U**123456789	**RU**1234567890

By using the convention of 7 digits to represent short addresses, 9 digits to represent some of the long addresses in set 1–2, and 10 digits to represent the balance of long addresses, it is possible to differentiate between the different types of addresses. The range of the decimal address field consists of the numbers 1 through 5,370,810,366 where short and other single code word addresses fall below 2,031,615 and Long addresses are above 2,101,248. The goal in displaying a CAPCODE is to use the shortest form possible. Even though the non-standard form could represent a standard assignment, the standard form is chosen to indicate that it is a standard assignment. All CAPCODE forms, except *Example 4* in **Table A-22**, contain the information required to send a message to a subscriber unit.

STANDARD FRAME AND PHASE EMBEDDING RULES

Maximum battery life in a FLEX decoding device is achieved when all of the addresses assigned to a device are in the same frame. For single-phase decoding devices, it is a requirement for all assigned addresses to be in the same phase.

Normally, it is very desirable to spread the population of FLEX subscriber units on a system across all four phases of all 128 frames. Frame and phase spreading can be performed automatically as addresses are assigned sequentially by embedding that information into the 7-, 9-, and 10-digit decimal FLEX address.

The standard procedure for deriving the phase and frame values from the CAPCODE starts by separating the 7-, 9-, or 10-digit decimal address portion (field to the right of the CAPCODE type) and performing a decimal to binary conversion. The Least Significant Bit (LSB) is labeled bit “0”. The following bits “2 and 3" in order, specify phases 00, 01, 10, or 11 for phase 0,1,2,3 (a, b, c, d), and bits “4–10” represent frames “000” through “127”.

The frame and phase can also be derived from the 7-, 9-, or 10-digit decimal address by using modulo arithmetic (base 10) where:

Phase = (Integer (Addr / 4)) Modulo 4
Frame = (Integer (Addr / 16)) Modulo 128

When these rules are used, and addresses are assigned in order, the phase increments after four consecutive addresses are assigned, while the frame is incremented after sixteen addresses are assigned.

CAPCODE ALPHA CHARACTER DEFINITION

The alpha character in the FLEX CAPCODE indicates the type of decoding device to which the address is assigned. The types include single-phase, any-phase, or all-phase. It also indicates if the address is the first, second, third, or fourth address in the subscriber unit (when addresses are assigned in order and follow standard rules), and specifies the rules for determining in which phase and frame the address is active.

Table A-23 Alpha Character Codes

Standard Rules	No Rules (Non-Standard Form)
A—Single-phase Subtract 0	U—Single-phase, Phase 0
B—Single-phase Subtract 1	V—Single-phase, Phase 1
C—Single-phase Subtract 2	W—Single-phase, Phase 2
D—Single-phase Subtract 3	X—Single-phase, Phase 3

Table A-23 Alpha Character Codes (Continued)

Standard Rules	No Rules (Non-Standard Form)
E—Any-phase, Subtract 0	Y—Any-phase
F—Any-phase Subtract 1	—
G—Any-phase Subtract 2	—
H—Any-phase Subtract 3	—
I—All-phase Subtract 0	Z—All-phase
J—All-phase Subtract 1	—
K—All-phase Subtract 2	—
L—All-phase Subtract 3	—

The following rules apply:

- The character “A” represents a single-phase subscriber unit using the standard rules for embedding phase and frame. The character “B” is similar to “A”, except 1 is subtracted from the CAPCODE before applying the standard rule. Likewise, the characters “C” and “D” indicate that 2 or 3 is to be subtracted before applying the rule. Using these CAPCODE characters ensures that sequentially numbered CAPCODEs are assigned to a common phase and frame. These procedures modify the standard rules and are intended to simplify the order entry process for multiple address subscriber units. When addresses are assigned in order, the subtraction of 1, 2, or 3 ensures that the calculation for each additional address in a decoding device is referenced to the first address. Thus, all A, B, C, and D addresses are assigned to the same frame and phase.
- Alpha characters “E” through “H” and “I” through “L” represent any-phase and all-phase subscriber units where the subtract rule is modified to ensure that all addresses of a multiple address subscriber unit are in the same frame.
- For the cases where no rule is defined, the letters “U” through “X” indicate single-phase subscriber units assigned to phases 0 through 3 (phases a through d) with the frame and battery cycle explicitly displayed. “Y” and “Z” indicate non-standard addresses for any-phase and all-phase subscriber units.
- If the subscriber unit contains only a single individual address and the user is content with the recommended 30 second battery cycle, then the letter “A”, “E”, or “I” is added as a prefix to the 7-, 9- or 10-digit address, where “A” = single-phase device, “E” = any-phase device, and “I” = all-phase device.

- If the unit were to be a two address unit where both addresses are individual addresses, then “A”, “E”, or “I” would again preface the address field of the first address. “B”, “F”, or “J” would preface the second address. The “B”, “F”, or “J” indicates that the address is a second address and it is to have the properties of the first address. This rule eliminates the need for an administrative operator or a salesperson to calculate a starting address, which would allow standard rules to always apply.
- In other cases, especially where a group address is to be included, it is very likely that the “U” through “Z” forms of the CAPCODE will be used so that the frame can be explicitly chosen to provide best battery life, and the required “same phase” operation can be met in the case of the single-phase units.

CAPCODE TO BINARY CONVERSION

Short CAPCODE

To convert a short address CAPCODE, the number 32,768 is added to the 7-digit decimal CAPCODE address (or to any CAPCODE less than 2,031,615). The resultant number is then converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air.

Long CAPCODE 2,101,249 to 1,075,843,072

Long address set 1–2 is in this range. To convert a long address CAPCODE, the number 2,068,481 is subtracted from the CAPCODE address. The resultant number is then divided by 32,768 with the remainder, incremented by 1, being the 1st word of the long address. This is the same as calculating the ((CAPCODE – 2,068,481) modulo 32768) + 1. This value is converted to a 21-bit binary number, which becomes the information bits in the (31,21) BCH code word transmitted over the air as the 1st address word.

The second word of the long address is determined by first calculating the integer portion of the (CAPCODE – 2,068,481) divided by 32,768. This value is then subtracted from 2,097,151 (equivalent to the ones complement of the value in binary), and converted to a 21-bit binary number, which becomes the information bits in the (31, 21) BCH code word transmitted over the air as the second address word.

Long CAPCODE 1,075,843,073 to 3,223,326,720

Long address sets 1–3 and 1–4 are in this range. The 1st word of the long address is calculated following the same rules for the long addresses set 1–2. The second long address word is determined by subtracting 2,068,481 from the CAPCODE, the resultant number is divided by 32,768 with the integer portion added to 1,933,312. This value is converted to a 21-bit binary number, which becomes the (31,21) BCH code word transmitted over the air as the second address word.

Long CAPCODE 3,223,326,721 to 4,297,068,542

Long address set 2–3 is in this range. The first word is determined by subtracting 2,068,479 from the CAPCODE. The remainder of dividing by 32,768 is retained (i.e., modulo 32,768). This value is then added to 2,064,383 with the result converted to a 21-bit binary number, which becomes the information bits in the (31,21) BCH code word transmitted over the air as the 1st address word.

The second word is determined by subtracting 2,068,479 from the CAPCODE and finding the integer portion after dividing by 32,768. This value is then added to 1,867,776 and converted to a 21-bit binary number, which becomes the (31,21) BCH code word transmitted over the air as the second address word.

BINARY TO CAPCODE CONVERSION

With the address code word values that are transmitted over the air, the CAPCODE can be calculated by performing the inverse of the above-specified process. As an example, the short address code word is converted to decimal and the number 32,768 is subtracted to arrive at the 7-digit address portion of the CAPCODE. For the two word long address set 1–2, the address word 1 is first converted from binary to decimal. The second address word is then complemented, (or subtracted from 2,097,151 decimal) and converted to a decimal. This value is multiplied by 32,768, added to 2,068,480, and then added to address word 1. The result is the address portion of the FLEX CAPCODE.

CAPCODE ASSIGNMENTS

The following table defines the address usage assignment. All addresses not listed in this table are not defined and reserved for future use.

Table A-24 CAPCODE Assignment Table

CAPCODE Address Value	Description
0,000,000,000	Illegal
0,000,000,001 to 0,001,933,312	Short Addresses
0,001,933,313 to 0,001,998,848	Illegal
0,001,998,849 to 0,002,009,087	Reserved for Future Use
0,002,009,088 to 0,002,025,471	Information Service Addresses
0,002,025,472 to 0,002,029,567	Network Addresses
0,002,029,568 to 0,002,029,583	Temporary Addresses
0,002,029,584 to 0,002,029,599	Operator Messaging Addresses
0,002,029,600 to 0,002,031,614	Reserved for Future Use
0,002,031,615 to 0,002,101,248	Illegal
0,002,101,249 to 0,102,101,250	Long Address Set 1–2 Uncoordinated
0,102,101,251 to 0,402,101,250	Long Address Set 1–2 by Country[1]
0,402,101,251 to 1,075,843,072	Long Address Set 1–2 Global[2]
1,075,843,073 to 2,149,584,896	Long Address Set 1–3 Global[2]
2,149,584,897 to 3,223,326,720	Long Address Set 1–4 Global[2]
3,223,326,721 to 3,923,326,750	Long Address Set 2–3 by Country[1]
3,923,326,751 to 4,280,000,00	Long Address Set 2–3 Reserved
4,280,000,001 to 4,285,000,000	Long Address Set 2–3 Info Service[3] Global[2]
4,285,000,001 to 4,290,000,000	Long Address Set 2–3 Info Service[3] by Country[1]
4,290,000,001 to 4,291,000,000	Long Address Set 2–3 Info Service[3] World-Wide Use[4]
4,291,000,001 to 4,297,068,542	Reserved for Future Use

Notes:
1. "by Country"—The addresses are coordinated within each country and with countries along borders.
2. "Global"—The address is coordinated to be unique world–wide.
3. "Info Service"—Rules governing the use of these addresses are not currently defined.
4. "World Wide Use"—One thousand addresses are assigned to each country for world-wide use.

APPENDIX B

SPI PACKETS

All data communicated between the FLEXchip IC and the host MCU is transmitted on the SPI in 32-bit packets. Each packet consists of an 8-bit ID followed by 24 bits of information. The FLEXchip IC uses the SPI bus in Full Duplex mode. In other words, whenever a packet communication occurs, the data in both directions is valid packet data.

The SPI consists of a $\overline{\text{READY}}$ pin and four SPI pins ($\overline{\text{SS}}$, SCK, MOSI, and MISO).The $\overline{\text{SS}}$ is used as a chip select for the FLEXchip IC. The SCK is a clock supplied by the host MCU. The data from the host is transmitted on the MOSI line. The data from the FLEXchip IC is transmitted on the MISO line.

PACKET COMMUNICATION INITIATED BY THE HOST

When the host sends a packet to the FLEXchip IC, it performs the following steps (see **Figure B-1**):

1. Select the FLEXchip IC by driving the $\overline{\text{SS}}$ pin low.
2. Wait for the FLEXchip IC to drive the $\overline{\text{READY}}$ pin low.
3. Send the 32-bit packet.
4. De-select the FLEXchip IC by driving the $\overline{\text{SS}}$ pin high.
5. Repeat steps 1 through 4 for each additional packet.

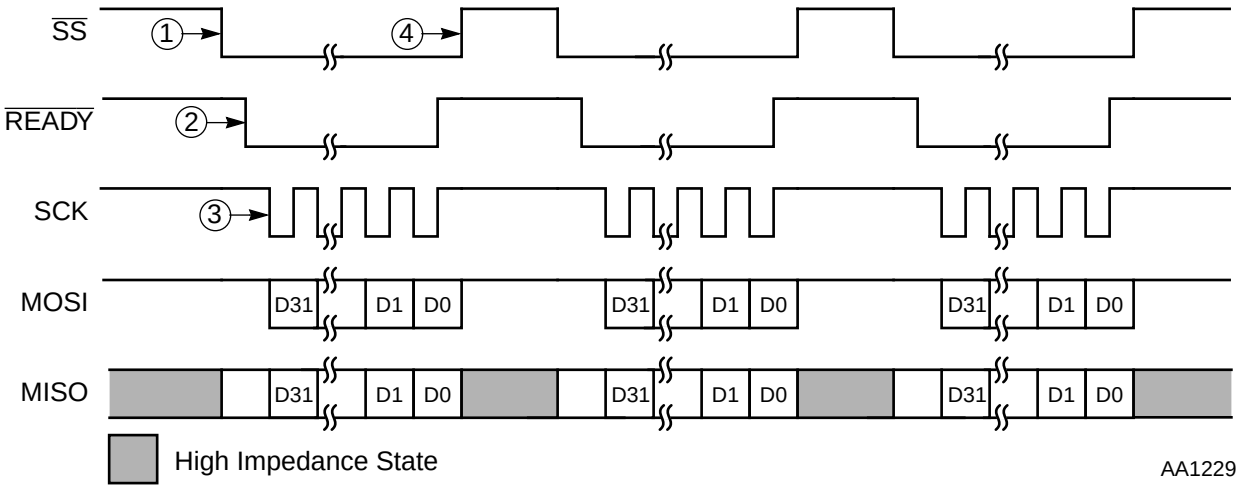


Figure B-1 Typical Multiple Packet Communications Initiated by the Host

When the host sends a packet, it will also receive a valid packet from the FLEXchip IC. If the FLEXchip IC is enabled (See **Checksum Packet** on page B-6.) and has no other packets waiting to be sent, the FLEXchip IC will send a status packet. The host must transition the $\overline{SS}$ pin from high to low to begin each 32-bit packet. The FLEXchip IC must see a negative transition on the $\overline{SS}$ pin in order for the host to initiate each packet communication.

PACKET COMMUNICATION INITIATED BY THE FLEXCHIP IC

When the FLEXchip IC has a packet for the host to read, the following occurs (see **Figure B-2**):

1. The FLEXchip IC drives the $\overline{READY}$ pin low.
2. If the FLEXchip IC is not already selected, the host selects the FLEXchip IC by driving the $\overline{SS}$ pin low.
3. The host receives (and sends) a 32-bit packet.
4. The host de-selects the FLEXchip IC by driving the $\overline{SS}$ pin high (optional).

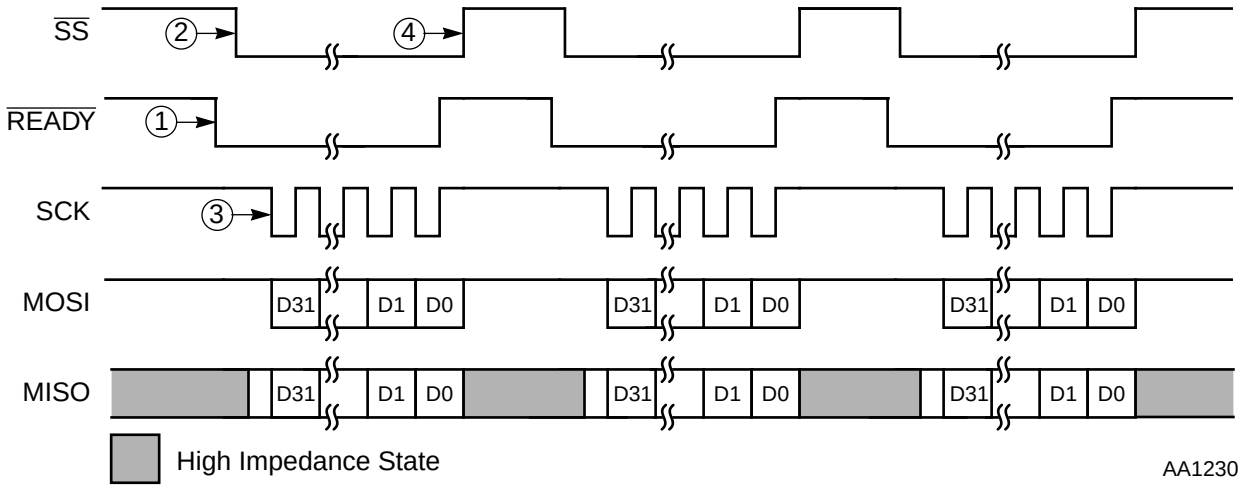


Figure B-2 Typical Multiple Packet Communications Initiated by the FLEXchip IC

When the host is reading a packet from the FLEXchip IC, it must send a valid packet to the FLEXchip IC. If the host has no data to send, it is suggested that the host send a Checksum Packet with all of the data bits set to 0 in order to avoid disabling the FLEXchip IC. (See **Checksum Packet** on page B-6.)

Figure B-3 on page B-3 illustrates that it is not necessary to de-select the FLEXchip IC between packets when the packets are initiated by the FLEXchip IC.

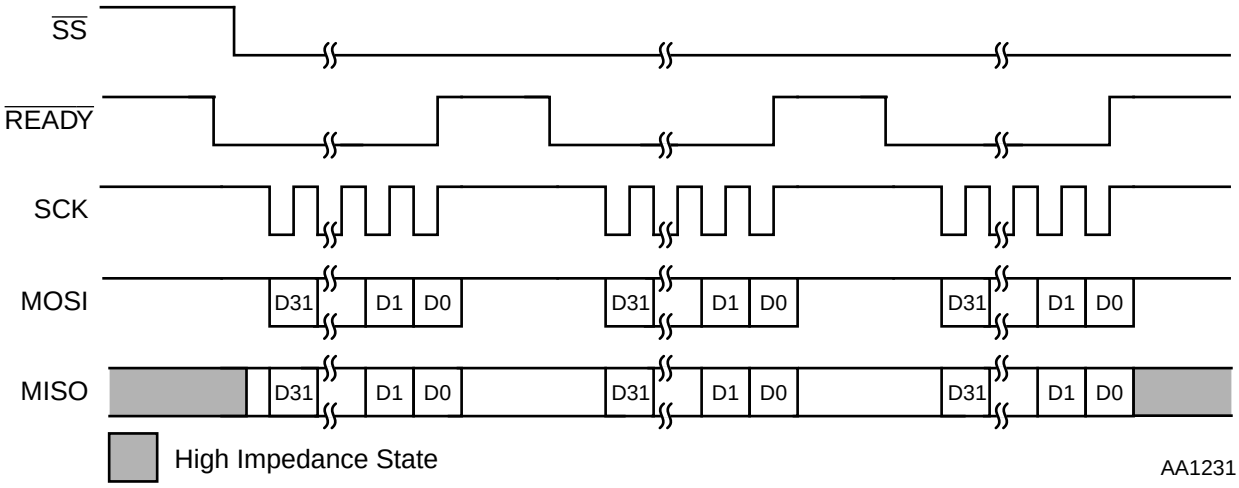


Figure B-3 Multiple Packet Communications Initiated by the FLEXchip IC with No De-select

HOST-TO-DECODER PACKET MAP

The upper 8 bits of a packet comprise the packet ID. The following table describes the packet ID's for all of the packets that can be sent to the FLEXchip IC from the host.

Table B-1 Host-to-Decoder Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Checksum
01	Configuration
02	Control
03	All Frame Mode
04–0E	Reserved (Host should never send)
0F	Receiver Line Control
10	Receiver Control Configuration (Off Setting)
11	Receiver Control Configuration (Warm Up 1 Setting)
12	Receiver Control Configuration (Warm Up 2 Setting)
13	Receiver Control Configuration (Warm Up 3 Setting)
14	Receiver Control Configuration (Warm Up 4 Setting)

Table B-1 Host-to-Decoder Packet ID Map (Continued)

Packet ID (Hexadecimal)	Packet Type
15	Receiver Control Configuration (Warm Up 5 Setting)
16	Receiver Control Configuration (3200sps Sync Setting)
17	Receiver Control Configuration (1600sps Sync Setting)
18	Receiver Control Configuration (3200sps Data Setting)
19	Receiver Control Configuration (1600sps Data Setting)
1A	Receiver Control Configuration (Shut Down 1 Setting)
1B	Receiver Control Configuration (Shut Down 2 Setting)
1C–1F	Special (Ignored by FLEXchip IC)
20	Frame Assignment (Frames 112 through 127)
21	Frame Assignment (Frames 96 through 111)
22	Frame Assignment (Frames 80 through 95)
23	Frame Assignment (Frames 64 through 79)
24	Frame Assignment (Frames 48 through 63)
25	Frame Assignment (Frames 32 through 47)
26	Frame Assignment (Frames 16 through 31)
27	Frame Assignment (Frames 0 through 15)
28–77	Reserved (Host should never send)
78	User Address Enable
79–7F	Reserved (Host should never send)
80	User Address Assignment (User address 0)
81	User Address Assignment (User address 1)
82	User Address Assignment (User address 2)
83	User Address Assignment (User address 3)
84	User Address Assignment (User address 4)
85	User Address Assignment (User address 5)

Table B-1 Host-to-Decoder Packet ID Map (Continued)

Packet ID (Hexadecimal)	Packet Type
86	User Address Assignment (User address 6)
87	User Address Assignment (User address 7)
88	User Address Assignment (User address 8)
89	User Address Assignment (User address 9)
8A	User Address Assignment (User address 10)
8B	User Address Assignment (User address 11)
8C	User Address Assignment (User address 12)
8D	User Address Assignment (User address 13)
8E	User Address Assignment (User address 14)
8F	User Address Assignment (User address 15)
90–FF	Reserved (Host should never send)

DECODER-TO-HOST PACKET MAP

The following table describes the packet ID's for all of the packets that can be sent to the host from the FLEXchip IC.

Table B-2 Decoder-to-Host Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Block Information Word
01	Address
02–57	Vector or Message (ID is word number in frame)
58–7E	Reserved
7F	Status
80–FE	Reserved
FF	Part ID

HOST-TO-DECODER PACKET DESCRIPTIONS

The following sections describe the packets of information sent from the host to the FLEXchip IC. In all cases the packets should be sent MSB first (Bit 7 of byte 3 = Bit 31 of the packet = MSB).

Checksum Packet

The Checksum Packet is used to ensure proper communication between the host and the FLEXchip IC. The FLEXchip IC exclusive-ORs the 24 data bits of every packet it receives (except the Checksum Packet and the special packet ID's 1C through 1F hexadecimal) with an internal checksum register. Upon reset and whenever the host writes a packet to the FLEXchip IC, the FLEXchip IC is disabled from sending any information to the host processor until the host processor sends a Checksum Packet with the proper Checksum Value (CV) to the FLEXchip IC. When the FLEXchip IC is disabled in this way, it prompts the host to read the Part ID Packet. Note that all other operation continues normally when the FLEXchip IC is "disabled". The FLEXchip IC is only disabled in the sense that the data can not be read from the FLEXchip IC, all other operations continue to function.

When the FLEXchip IC is reset, it is disabled and the internal checksum register is initialized to the 24-bit part ID defined in the Part ID Packet. (See **Part ID Packet** on page B-34.) Every time a packet other than the Checksum Packet and the special packets 1C through 1F is sent to the decoder IC, the value sent in the 24 information bits is exclusive-ORed with the internal checksum register, the result is stored back to the checksum register, and the FLEXchip IC is disabled. If a Checksum Packet is sent and the CV bits match the bits in the checksum register, the FLEXchip IC is enabled. If a Checksum Packet is sent when the FLEXchip IC is already enabled, the packet is ignored by the FLEXchip IC, in which case a null packet having the ID and data bits set to 0 is suggested. If a packet other than the Checksum Packet is sent when the FLEXchip IC is enabled, the decoder IC will be disabled until a Checksum Packet is sent with the correct CV bits.

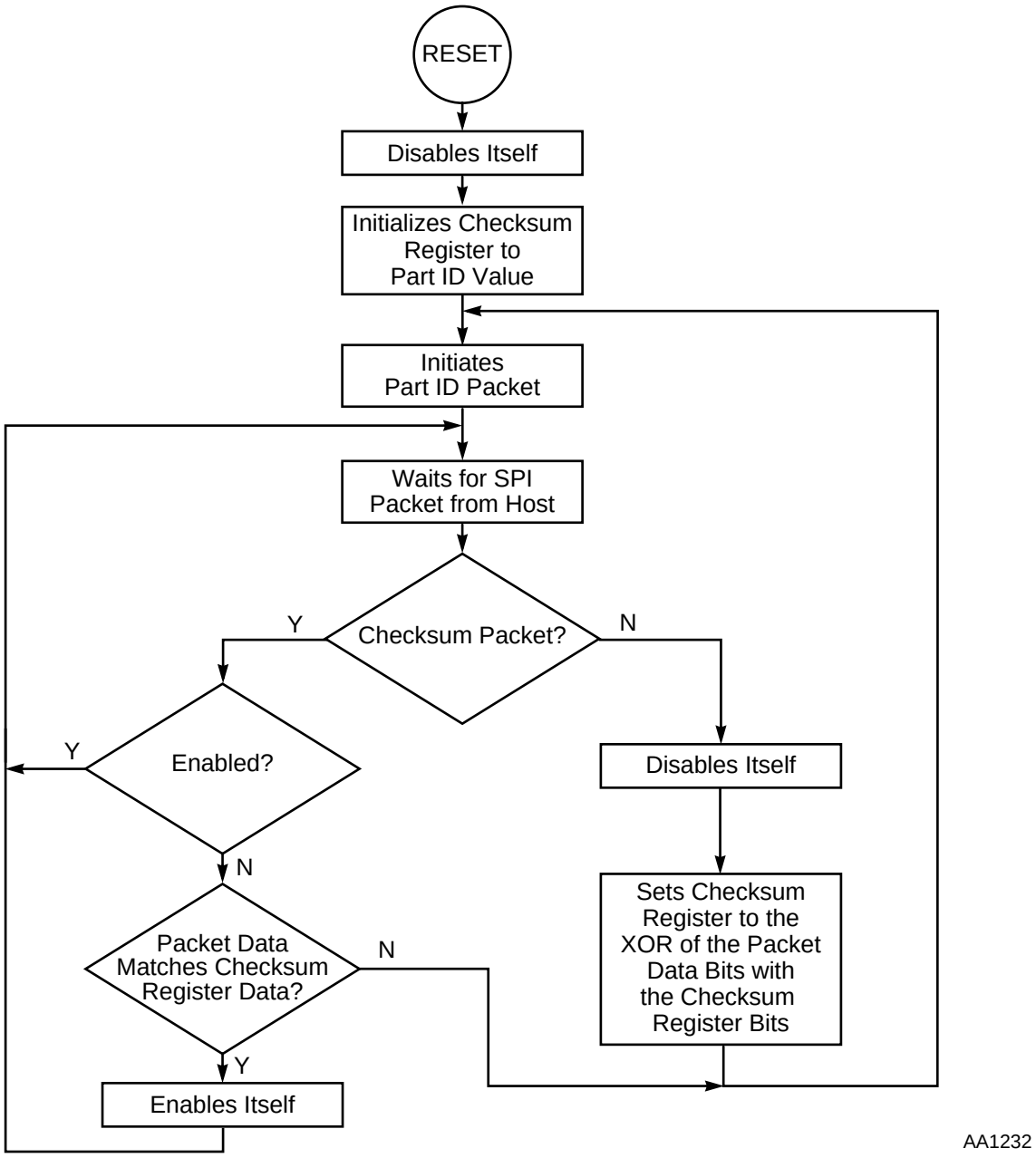


Figure B-4 FLEXchip IC Checksum Flow Chart

When the host reads a packet out of the FLEXchip IC but has no data to send, the Checksum Packet should be sent so the FLEXchip IC will not be disabled. The data in the Checksum Packet could be a null packet, 32-bit stream of all 0s, since a Checksum Packet will not disable the FLEXchip IC. When the host re-configures the FLEXchip IC, the FLEXchip IC will be disabled from sending any packets other than the Part ID Packet until the FLEXchip IC is enabled with a Checksum Packet having the proper data. The ID of the Checksum Packet is 0.

Table B-3 Checksum Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	0	0	0	0
2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0
Note: CV = Checksum Value								

Configuration Packet

The Configuration Packet defines a number of different configuration options for the FLEXchip IC. The FLEXchip IC ignores this packet when decoding is enabled (i.e., the ON bit in the Control Packet is set). The ID of the Configuration Packet is 1.

Table B-4 Configuration Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	OFD_1	OFD_0
1	0	0	0	0	0	0	SP_1	SP_0
0	SME	MOT	COD	MTE	LBP	0	0	0

OSCILLATOR FREQUENCY DIFFERENCE (OFD)

These bits describe the maximum difference in the frequency of the 76.8 kHz oscillator crystal with respect to the frequency of the transmitter. These limits should be the worst case difference in frequency due to all conditions, including but not limited to aging, temperature, and manufacturing tolerance. Using a smaller frequency difference in this packet will result in lower power consumption due to higher receiver battery save ratios. Note that this value is not the absolute error of the oscillator frequency provided to the FLEXchip IC. The absolute error of the clock used by the FLEX transmitter must be taken into account. (If the transmitter tolerance is ±25 ppm and the 76.8 kHz oscillator tolerance is ±140 ppm, the oscillator frequency difference is ±165 ppm and OFD should be set to 0.) The value after reset = 0. **Table B-5** on page B-9 summarizes the bit definitions.

Table B-5 OFD Bits Description

OFD_1	OFD_0	Frequency Difference
0	0	±300 ppm
0	1	±150 ppm
1	0	±75 ppm
1	1	±0 ppm

SIGNAL POLARITY (SP)

These bits set the polarity of EXTS1 and EXTS0 input signals. The value after reset = 0. The polarity of the EXTS0 and EXTS1 bits will be determined by the receiver design.

Table B-6 SP Bit Definition

SP_1	SP_0	Signal Polarity EXTS1	Signal Polarity EXTS0
0	0	Normal	Normal
0	1	Normal	Inverted
1	0	Inverted	Normal
1	1	Inverted	Inverted

FSK Modulation @ SP = 0,0	EXTS1	EXTS0
+ 4800 Hz	1	0
+1600 Hz	1	1
–1600 Hz	0	1
–4800 Hz	0	0

SYNCHRONOUS MODE ENABLE (SME)

When this bit is set, a Status Packet will be automatically sent whenever the **SMU** (Synchronous Mode Update) bit in the Status Packet is set. The host can use the **SM** (Synchronous Mode) bit in the Status Packet as an in-range / out-of-range indication. The value after reset = 0.

MAXIMUM OFF TIME (MOT)

When this bit is clear, the FLEXchip IC assumes that there can be at most 4 minutes between transmitted frames on the paging system. When this bit is set, the FLEXchip IC assumes that there can be at most 1 minute between transmitted frames on the paging system. This setting is determined by the service provider. The value after reset = 0.

CLOCK OUTPUT DISABLE (COD)

When this bit is clear, a 38.4 kHz signal will be output on the CLKOUT pin. When this bit is set, the CLKOUT pin will be driven low. Note that setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4 kHz period. Also note that when the clock output is enabled, the CLKOUT pin will always output

the 38.4 kHz signal even when the FLEXchip IC is in reset (as long as the FLEXchip IC oscillator is seeing clocks). The value after reset = 0.

MINUTE TIMER ENABLE (MTE)

When this bit is set, a Status Packet will be sent at one minute intervals with the MT (Minute Time-out) bit in the Status Packet set. When this bit is clear, the internal one-minute timer stops counting. The internal one-minute timer is reset when this bit is changed from 0 to 1 or when the MTC (Minute Timer Clear) bit in the Control Packet is set. The value after reset = 0.

LOW BATTERY POLARITY (LBP)

This bit defines the polarity of the FLEXchip ICs LOBAT pin. The LB bit in the Status Packet is initialized to the inverse value of this bit when the FLEXchip IC is turned on (by setting the ON bit in the Control Packet). When the FLEXchip IC is turned on, a low battery update is sent to the host in the Status Packet when a low battery condition is detected on the LOBAT pin. Setting this bit means that a high on the LOBAT pin indicates a low voltage condition. The value after reset = 0.

Control Packet

The Control Packet defines a number of different control bits for the FLEXchip IC. The ID of the Control Packet is 2.

Table B-7 Control Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	0	0	1	0
2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
1	0	SPM	PS_1	PS_0	0	0	0	0
0	0	SBI	0	MTC	0	0	0	ON

FORCE FRAME (FF) 0–7

These bits enable and disable forcing the FLEXchip IC to look in frames 0 through 7. When an FF bit is set, the FLEXchip IC will decode the corresponding frame. Unlike the AF bits in the Frame Assignment Packets, the system collapse of a FLEX system will not affect frames assigned using the FF bits. (Where as setting AF_0 to 1 when the system collapse is 5 will cause the decoder to decode frames 0, 32, 64, and 96, setting FF_0 to 1 when the system collapse is 5 will only cause the decoder to decode frame 0.) This may be useful for acquiring transmitted time information. The value after reset = 0.

SINGLE PHASE MODE (SPM)

When this bit is set, the FLEXchip IC will decode only one phase of the transmitted data. When this bit is clear, the FLEXchip IC will decode all of the phases it receives. A change to this bit while the FLEXchip IC is on, will not take affect until the next block 0 of a frame. The value after reset = 0.

PHASE SELECT (PS)

When the SPM bit is set, these bits define what phase the FLEXchip IC should decode according to the following table. This value is determined by the service provider. A change to these bits while the FLEXchip IC is on, will not take affect until the next block 0 of a frame. The value after reset = 0.

Table B-8 Phase Select Bit Definition

PS Value		Phase Decoded (based on FLEX Data Rate)		
PS_1	PS_0	1600 bps	3200 bps	6400 bps
0	0	a	a	a
0	1	a	a	b
1	0	a	c	c
1	1	a	c	d

SEND BLOCK INFORMATION (SBI) WORDS 2-4

When this bit is set, any errored or time-related block information words 2–4 will be sent to the host. The value after reset = 0.

MINUTE TIMER CLEAR (MTC)

Setting this bit will cause the one minute timer to restart from 0.

TURN ON DECODER (ON)

Set if the FLEXchip IC should be decoding FLEX signals. Clear if signal processing should be off (Very Low Power mode). The value after reset = 0.

All Frame Mode Packet

The All Frame Mode Packet is used to decrement temporary address enable counters by one, decrement the all frame mode counter by one, and/or enable or disable forcing All Frame mode. If All Frame mode is enabled, the FLEXchip IC will attempt to decode every frame and send a Status Packet with the EOF (End-Of-Frame) bit set at the end of every frame. All Frame mode is enabled if any temporary address enable counter is non-zero, or, the All Frame mode counter is non-zero, or, the force All Frame Mode bit is set. Both the All Frame mode counter and the temporary address enable counters can only be incremented internally by the FLEXchip IC and can only be decremented by the host. The FLEXchip IC will increment a temporary address enable counter whenever a short instruction vector is received assigning the corresponding temporary address. The FLEXchip IC will increment the All Frame mode counter whenever an alphanumeric, HEX / binary, or secure vector is received. When the host determines that a message associated with a temporary address, or a fragmented message has ended, then the appropriate temporary address counter or All Frame mode counter should be decremented by writing an All Frame Mode Packet to the FLEXchip IC in order to exit the All Frame mode, thereby improving battery life. Neither the temporary address enable counters nor the All Frame mode counter can be incremented past the value 127 or decremented past the value 0 (i.e., it will not roll over). The temporary address enable counters and the All Frame mode counter are initialized to 0 at reset and when the decoder is turned off. The ID of the All Frame Mode Packet is 3.

Table B-9 All Frame Mode Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	0	0	1	1
2	DAF	FAF	0	0	0	0	0	0
1	DTA_{15}	DTA_{14}	DTA_{13}	DTA_{12}	DTA_{11}	DTA_{10}	DTA_9	DTA_8
0	DTA_7	DTA_6	DTA_5	DTA_4	DTA_3	DTA_2	DTA_1	DTA_0

DECREMENT ALL FRAME (DAF) COUNTER

Setting this bit decrements the All Frame mode counter by one. If a packet is sent with this bit clear, the All Frame mode counter is not affected. The value after reset = 0.

FORCE ALL FRAME (FAF) MODE

Setting this bit forces the FLEXchip IC to enter All Frame mode. If this bit is clear, the FLEXchip IC may or may not be in All Frame mode depending on the status of the All Frame mode counter and the temporary address enable counters. This may be useful in acquiring transmitted time information. The value after reset = 0.

DECREMENT TEMPORARY ADDRESS (DTA) ENABLE COUNTER

When a bit in this word is set, the corresponding temporary address enable counter is decremented by 1. When a bit is cleared, the corresponding temporary address enable counter is not affected. When a temporary address enable counter reaches 0, the temporary address is disabled.The value after reset = 0.

Receiver Line Control Packet

This packet gives the host control over the settings on the receiver control lines (S0–S7) in all modes except reset. In reset, the receiver control lines are in high impedance settings. The ID for the Receiver Line Control Packet is 15 (decimal).

Table B-10 Receiver Line Control Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	1	1	1	1
2	0	0	0	0	0	0	0	0
1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

FORCE RECEIVER SETTING (FRS)

Setting a bit to one will cause the corresponding CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line (S0–S7). Clearing a bit gives control of the corresponding receiver control lines (S0–S7) back to the FLEXchip IC. The value after reset = 0.

CONTROL LINE SETTING (CLS)

If the corresponding FRS bit was set in this packet, these bits define what setting should be applied to the corresponding receiver control lines. The value after reset = 0.

Receiver Control Configuration Packets

These packets allow the host to configure:

- what setting is applied to the receiver control lines S0–S7,
- how long to apply the setting, and,
- when to read the value of the LOBAT input pin.

For a more detailed description of how the FLEXchip IC uses these settings see **Receiver Control Configuration Packets** on page B-14 .

The FLEXchip IC defines twelve different receiver control settings. The FLEXchip IC ignores these packets when decoding is enabled (i.e., the ON bit in the Control Packet is set). The IDs for these packets range from 16 to 27 (decimal).

Table B-11 Receiver Off Setting Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	1	0	0	0	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

LOW BATTERY CHECK (LBC)

If this bit is set, the FLEXchip IC will check the status of the **LOBAT** port just before leaving this receiver state. The value after reset = 0.

CONTROL LINE SETTING (CLS)

This is the value to be output on the receiver control lines (S0–S7) for this receiver state. The value after reset = 0.

STEP TIME (ST)

This is the time the FLEXchip IC is to keep the receiver off before applying the first warm up state's receiver control value to the receiver control lines. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01) to 159.375 ms
(ST = FF in hexadecimal). (The value after reset = 625 µs)

Receiver Warm Up Setting Packets

Table B-12 Receiver Warm Up Setting Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

SETTING NUMBER (s)

These bit define the receiver control setting for which this packet's values are to be applied. The following truth table shows the names of each of the values for s that apply to this packet.

Table B-13 Setting Number Bit Combinations

s_3	s_2	s_1	s_0	Setting Name
0	0	0	1	Warm Up 1
0	0	1	0	Warm Up 2
0	0	1	1	Warm Up 3
0	1	0	0	Warm Up 4
0	1	0	1	Warm Up 5

STEP ENABLE (SE)

The receiver setting is enabled when the bit is set. If a step in the warm up sequence is disabled, all steps following the disabled step will be ignored. The value after reset = 0.

LOW BATTERY CHECK (LBC)

If this bit is set, the FLEXchip IC will check the status of the LOBAT port just before leaving this receiver state. The value after reset = 0.

CONTROL LINE SETTING (CLS)

This is the value to be output on the receiver control lines (S0–S7) for this receiver state. The value after reset = 0.

STEP TIME (ST)

This is the time the FLEXchip IC is to wait before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01) to 79.375 ms (ST = 7F in hexadecimal) (The value after reset = 625 µs).

3200 sps Sync Setting Packets

Table B-14 3200 sps Sync Setting Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	1	0	1	1	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

LOW BATTERY CHECK (LBC)

If this bit is set, the FLEXchip IC will check the status of the LOBAT port just before leaving this receiver state. The value after reset = 0.

CONTROL LINE SETTING (CLS)

This is the value to be output on the receiver control lines (S0–S7) for this receiver state. The value after reset = 0.

STEP TIME (ST)

This is the time the FLEXchip IC is to wait before expecting good signals on the EXTS1 and EXTS0 signals after warming up. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01) to 79.375 ms (ST = 7F in hexadecimal). (The value after reset = 625 µs.)

Receiver On Setting Packets

Table B-15 Receiver On Setting Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	0	0	0	0	0	0

SETTING NUMBER (s)

These bits define the receiver control setting for which this packet's values are to be applied. The following truth table shows the names of each of the values for "s" that apply to this packet.

Table B-16 Setting Number Bit Definitions

s_3	s_2	s_1	s_0	Setting Name
0	1	1	1	1600 sps Sync
1	0	0	0	3200 sps Data
1	0	0	1	1600 sps Data

LOW BATTERY CHECK (LBC)

If this bit is set, the FLEXchip IC will check the status of the LOBAT port just before leaving this receiver state. The value after reset = 0.

CONTROL LINE SETTING (CLS)

This is the value to be output on the receiver control lines (S0–S7) for this receiver state. The value after reset = 0.

Receiver Shut Down Setting Packets

Table B-17 Receiver Shut Down Setting Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	1	1	0	1	s
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

SETTING NUMBER (s)

These bits define the receiver control setting for which this packet's values are to be applied. The following truth table shows the names of each of the values for "**s"** that apply to this packet.

Table B-18 Setting Number Bit Definitions

s	Setting Name
0	Shut Down 1
1	Shut Down 2

STEP ENABLE (SE)

The receiver setting is enabled when the bit is set. If a step in the shut down sequence is disabled, all steps following the disabled step will be ignored. The value after reset = 0.

LOW BATTERY CHECK (LBC)

If this bit is set, the FLEXchip IC will check the status of the LOBAT port just before leaving this receiver state. The value after reset = 0.

CONTROL LINE SETTING (CLS)

This is the value to be output on the receiver control lines (S0–S7) for this receiver state. The value after reset = 0.

STEP TIME (ST)

This is the time the FLEXchip IC is to wait before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625us. Valid values are 625 µs (ST = 01) to 39.375 ms (ST = 3F in hexadecimal).
(The value after reset = 625 µs.)

Frame Assignment Packets

The FLEX protocol defines that each address of a FLEX pager is assigned a home frame and a pager collapse. This information is determined by the service provider. The FLEXchip IC must be configured so that a frame that is assigned by one or more of the addresses' home frames and pager collapses has its corresponding configuration bit set. For example, if the FLEXchip IC has one enabled address and it is assigned to frame 3 with a battery cycle of 4, the AF bits for frames 3, 19, 35, 51, 67, 83, 99, and 115 should be set and the AF bits for all other frames should be cleared. There are 8 Frame Assignment Packets. The IDs for these packets range from 32 to 39 (decimal).

Table B-19 Frame Assignment Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	1	0	0	f_2	f_1	f_0
2	0	0	0	0	0	0	0	0
1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

FRAME RANGE (f)

This value determines which sixteen frames correspond to the sixteen AF bits in the packet according to the following table. At least one of these bits must be set when the FLEXchip IC is turned on by setting the ON bit in the control packet. The value after reset = 0.

Table B-20 Frame Range Bit Definition

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	Frame 127	Frame 112
0	0	1	Frame 111	Frame 96
0	1	0	Frame 95	Frame 80
0	1	1	Frame 79	Frame 64
1	0	0	Frame 63	Frame 48
1	0	1	Frame 47	Frame 32
1	1	0	Frame 31	Frame 16
1	1	1	Frame 15	Frame 0

ASSIGNED FRAME (AF)

If a bit is set, the FLEXchip IC will consider the corresponding frame to be assigned via an address's home frame and pager collapse. The value after reset = 0.

User Address Enable Packet

The User Address Enable Packet is used to enable and disable the 16 user address words. Although the host is allowed to change the user address words while the FLEXchip IC is decoding FLEX signals, the host must disable a user address word before changing it. The ID of the User Address Enable Packet is 120 (decimal).

Table B-21 User Address Enable Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	1	1	1	1	0	0	0
2	0	0	0	0	0	0	0	0
1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_{9}	UAE_{8}
0	UAE_{7}	UAE_{6}	UAE_{5}	UAE_{4}	UAE_{3}	UAE_{2}	UAE_{1}	UAE_{0}

When a User Address Enable (UAE) bit is set, the corresponding user address word is enabled. When it is cleared, the corresponding user address word is disabled. UAE_0 corresponds to the user address word configured using a packet ID of 128, and UAE_{15} corresponds to the user address word configured using a packet ID of 143. In some instances, if an invalid FLEX messaging address is programmed, it will not be detected even when the address is enabled. The value after reset = 0.

User Address Assignment Packets

The FLEXchip IC has sixteen user address words. Each word can be programmed to be a short address or part of a long address. The addresses are configured using the Address Assignment Packets. Each user address can be configured as long or short and tone-only or regular. Although the host is allowed to send these packets while the FLEXchip IC is on, the host must disable the user address word by clearing the corresponding UAE bit in the User Address Enable Packet before changing any of the bits in the corresponding User Address Assignment Packet. This method allows for easy reprogramming of user addresses without disrupting normal operation. The IDs for these packets range from 128 to 143 (decimal).

Table B-22 User Address Assignment Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	1	0	0	0	a_3	a_2	a_1	a_0
2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

USER ADDRESS WORD NUMBER (a_0–a_3)

This specifies which address word is being configured. Having all 0s in this field corresponds to Address Index zero (AI = 0) in the Address Packet received from the FLEXchip IC when an address is detected. (See **Address Packet** on page B-23.)

LONG ADDRESS (LA)

When this bit is set, the address is considered a long address. Both words of a long address must have this bit set. The first word of a long address must have an even user address word number and the second word must be in the address index immediately following the first word. Long addresses of the 2-3 and 2-4 set (See **FLEX CAPCODES** on page A-21) must be programmed to higher user address word numbers than long addresses of the 1-2, 1-3, and 1-4 set.

TONE-ONLY ADDRESS (TOA)

When this bit is set, the FLEXchip IC will consider this address a tone-only address and will not decode a vector word when the address is received. If the TOA bit of a long address word is set, the TOA bit of the other word of the long address must also be set.

ADDRESS WORD (A_0–A_{20})

This is the 21-bit value of the address word. Valid FLEX messaging addresses must be used. In some instances, if an invalid FLEX messaging address is programmed, it will not be detected even when the address is enabled.

DECODER-TO-HOST PACKET DESCRIPTIONS

The following sections describe the packets of information that will be sent from the FLEXchip IC to the host. In all cases the packets are sent MSB first (Bit 7 of byte 3 = Bit 31 of the packet = MSB). The FLEXchip IC decides what data should be sent to the host. If the FLEXchip IC is disabled through the checksum feature (see **Checksum Packet** on page B-6), the Part ID Packet will be sent. Data Packets relating to data received over the air are buffered in the 32 packet transmit buffer. The Data Packets include Block Information Word Packets, Address Packets, Vector Packets, and Message Packets. If the FLEXchip IC is enabled and there is data in the transmit buffer, a packet from the transmit buffer will be sent. If the FLEXchip IC is enabled and no Data Packet or Part ID Packet is pending, the FLEXchip IC will send the Status Packet (which is not buffered). In the event of a buffer overflow, the FLEXchip IC will automatically stop decoding and clear the buffer information.

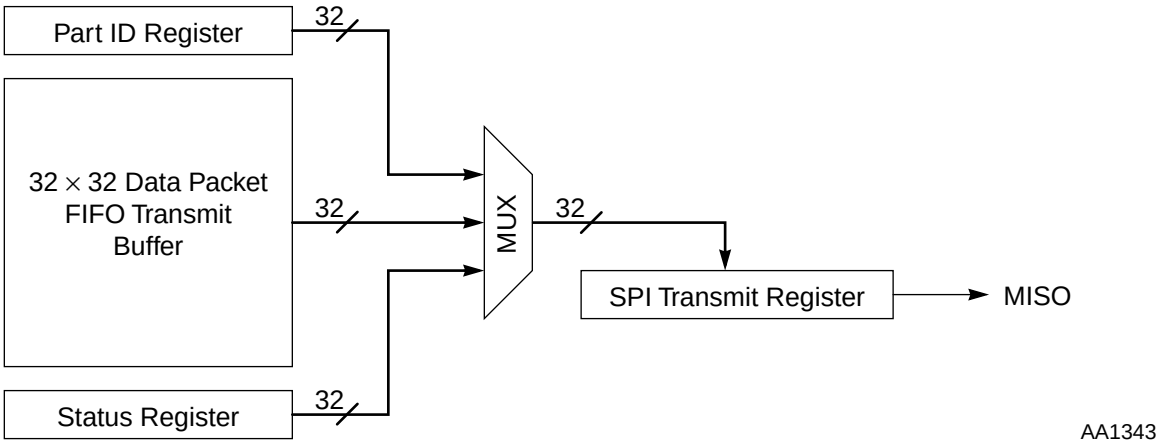


Figure B-5 FLEXchip IC SPI Transmit Functional Block Diagram

Block Information Word Packet

The Block Information Field is the first field following the synchronization codes of the FLEX protocol (see **Appendix A**). This field contains information about the frame, such as number of addresses and messages, as well as information about current time. The first block information word of each phase is used internally to the FLEXchip IC and is never transmitted to the host.

All time and date block information words (f = 001, 010, or 101) can be optionally sent to the host by setting the SBI bit in the control packet. (see **Control Packet** on page B-10.) When the SBI bit is set and a block information word is received with an uncorrectable number of bit errors, the FLEXchip will send the block information word to the host with the **e** bit set regardless of the value of the “f” field in the block information word. The FLEXchip IC does not support decoding of the vector and

message words associated with the Data/System Message block info word (f = 101). The ID of a Block Information Word Packet is 0 (decimal).

Table B-23 Block Information Word Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	0	0	0	0
2	e	p_1	p_0	x	x	f_2	f_1	f_0
1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

Note: e—set if more than 2 bit errors are detected in the word or if the check character calculation fails after error correction has been performed
p—phase on which the block information word was found (0=a, 1=b, 2=c, 3=d)
x—unused bits; the value of these bits is not guaranteed
f—Word Format Type; the value of these bits modify the meaning of the s bits in this packet as described in the following table; if the e bit is not set, this field will be one of 001, 010, or 101
s—These are the information bits of the block information word. The definition of these bits depend on the f bits in this packet. **Table B-24** describes the block information words that the FLEXchip IC decodes. Refer to **Appendix A** for detailed information about these block information words.

Table B-24 Block Information Word Definitions

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
001	m_3 m_2 m_1 m_0 d_4 d_3 d_2 d_1 d_0 Y_4 Y_3 Y_2 Y_1 Y_0	Month, Day, Year
010	S_2 S_1 S_0 M_5 M_4 M_3 M_2 M_1 M_0 H_4 H_3 H_2 H_1 H_0	Second, Minute, Hour
101	z_9 z_8 z_7 z_6 z_5 z_4 z_3 z_2 z_1 z_0 A_3 A_2 A_1 A_0	System Message

Address Packet

The Address Field follows the Block Information Field in the FLEX protocol. See **Appendix A** for additional information. It contains all of the addresses in the frame. If less than three bit errors are detected in a received address word and it matches an enabled address assigned to the FLEXchip IC, an Address Packet will be sent to the host processor. The Address Packet contains assorted data about the address and its associated vector and message. The ID of an Address Packet is 1 (decimal).

Table B-25 Address Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	0	0	0	0	0	0	1
2	PA	p_1	p_0	LA	x	x	x	x
1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

PRIORITY ADDRESS (PA)

This bit is set if the address was received as a priority address.

PHASE (p)

These bits identify the phase on which the address was detected (0 = a, 1 = b, 2 = c, 3 = d).

LONG ADDRESS TYPE (LA)

This bit is set if the address was programmed in the FLEXchip IC as a long address.

ADDRESS INDEX (AI)

Valid values are 0 through 15 and 128 through 143. The index identifies which of the addresses was detected. Values 0 through 15 will correspond to the sixteen programmable address words. Values 128 through 143 will correspond to the sixteen temporary addresses. For long addresses, the address detect packet will only be sent once and the index will refer to the second word of the address.

TONE ONLY ADDRESS (TOA)

This bit is set if the address was programmed in the FLEXchip IC as a tone-only address. No vector word will be sent for tone-only addresses.

WORD NUMBER (WN) OF VECTOR (2–87)

These bits describe the location in the frame of the vector word for the detected address. This value is invalid for this packet if the TOA bit is set.

UNUSED BITS (X)

The value of these bits is not guaranteed.

Vector Packet

The Vector Field follows the Address Field (see **Appendix A**). Each Vector Packet must be matched to its corresponding Address Packet. The ID of the vector packet is the word number where the vector word was received in the frame. This value corresponds to the WN bits sent in the associated address packet. The phase information must also match in both the Address Packet and the Vector Packet. It is important to note for long addresses, the first message word will be transmitted in the word location immediately following the associated vector.The word number (identified by b_6 to b_0) in the Vector Packet will indicate the message start of the second message word if the message is longer than 1 word.

There are several types of vectors:

- Short Message/Tone Only Vector
- Three types of Numeric Vectors
- Hex/Binary Vector
- Alphanumeric Vector
- Secure Message Vector
- Short Instruction Vector

Each is described in the following pages. A detailed description of the FLEX software protocol requirements is provided in **Appendix A**.

Four of the vectors (Hex/Binary, Alphanumeric, Secure Message, and Short Instruction) enable the FLEXchip IC to begin the All Frame mode. This mode is required to allow for the decoding of temporary addresses and/or fragmented messages. The host disables the All Frame mode after the proper time by writing to the decoder via the All Frame Mode Packet. For any Address Packet sent to the host (except tone-only addresses), a corresponding Vector Packet will always be sent. If more than two bit errors are detected (via BCH calculations, parity calculations, check character calculations, or value validation) in the vector word the **e** bit will be set and the message words will not be sent.

The Numeric, Hex/Binary, Alphanumeric, and Secure Message Vector Packets have associated Message Word Packets in the message field. The host must use the **n** and **b** bits of the vector word to calculate what message word locations are associated with the vector. Both the message word locations and the phase must match.

The Short Instruction Vector is used for assigning temporary addresses that may be associated with a group call.

SHORT MESSAGE / TONE ONLY VECTOR

Table B-26 Short Message / Tone Only Vector Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

Notes: 1. V: = 010 for a Short Message / Tone Only Vector
WN—Word number of vector (2–87 decimal); describes the location of the vector word in the frame
e—Set if more than 2 bit errors are detected in the word or, if after error correction, the check character calculation fails
p—Phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d)
d—Data bits whose definition depend on the value of t in this packet according to the following table
2. If this vector is received on a long address and the e bit in this packet is not set, the decoder will send a Message Packet from the word location immediately following the Vector Packet. Except for the short message on a non-network address (t = 0), all message bits in the Message Packet are unused and should be ignored

Table B-27 Short Message / Tone Only Vector Definitions

t_1t_0	d_{11}	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	Description
00	c_3	c_2	c_1	c_0	b_3	b_2	b_1	b_0	a_3	a_2	a_1	a_0	First 3 numeric chars[1]
01	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	S_2	S_1	S_0	8 sources (S) and 9 unused bits (s)
10	s_1	s_0	R_0	N_5	N_4	N_3	N_2	N_1	N_0	S_2	S_1	S_0	8 sources (S), message number (N), message retrieval flag (R)[2], and 2 unused bits (s)
11													spare message type

Notes: 1. For long addresses, an extra 5 characters are sent in the Message Packet immediately following the Vector Packet.
2. For a description of the R and N bits see the description of the same bits for numeric messages in **Appendix A**.
3. t = Message type—These bits define the meaning of the “d” bits in this packet.
x = Unused bits—The value of these bits is not guaranteed.

NUMERIC VECTOR PACKET

Table B-28 Numeric Vector Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

Vector Type Identifier (V)

Table B-29 Numeric Vector Definitions

$V_2V_1V_0$	Name	Description
011	Standard Numeric Format	No special formatting of characters is specified.
100	Special Format Numeric Vector	Formatting of the received characters is predetermined by special rules in the host. See **FLEX Message Word Definitions** on page A-7.
111	Numbered Numeric Vector	The received information has been numbered by the service provider to indicate all messages have been properly received.

Additional Bit Descriptors

Table B-30 Additional Bit Descriptor Definitions for Numeric Vector Packets

Designator	Definition
WN	This is the Word Number of vector (2–87 decimal) that describes the location of the vector word in the frame.
e	This bit is set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.
p	These bits define the phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d).
K	These are the beginning check bits of the message.

Table B-30 Additional Bit Descriptor Definitions for Numeric Vector Packets

Designator	Definition
n	These bits define the number of words in the message including the second vector word for long addresses (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is located in the word location that immediately follows the associated vector.
b	These bits define the word number of the message start in the message field (3–87 decimal). For long addresses, the word number indicates the location of the second message word.
x	These are unused bits. The value of these bits is not guaranteed.

HEX / BINARY, ALPHANUMERIC, AND SECURE MESSAGE VECTOR

Table B-31 HEX / Binary, Alphanumeric, and Secure Message Vector Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	n_6	n_5	n_4	n_3	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

Vector Type Identifier (V)

Table B-32 Vector Type Identifier Definition

$V_2V_1V_0$	Type
000	Secure
101	Alphanumeric
110	Hex / Binary

Additional Bit Descriptors

Table B-33 Additional Bit Descriptor Definitions for Numeric Vector Packets

Designator	Definition
WN	This is the Word Number of vector (2–87 decimal) and it describes the location of the vector word in the frame.
e	This bit is set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.
p	These bits define the phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d)
n	These bits define the number of message words in this frame including the first Message word that immediately follows a long address vector. Valid values are 1–85 decimal.
b	Word number of message starts in the message field. Valid values are 3–87 decimal. Note: For long addresses, the first Message Packet is sent from the word location immediately following the word location of the Vector Packet. The **b** bits indicate the second message word in the message field if one exists.
x	These are unused bits. The value of these bits is not guaranteed.

SHORT INSTRUCTION VECTOR

Table B-34 Short Instruction Vector Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

Table B-35 Short Instruction Vector Packet Bit Descriptions

Designator	Description
V	V = 001 for a Short Instruction Vector
WN	This indicates the Word Number of the vector (2–87 decimal) and describes the location of the vector word in the frame.
e	This bit is set if more than 2 bit errors are detected in the word or, if after error correction, the check character calculation fails.
p	These bits define the phase on which the vector was found . (0 = a, 1 = b, 2 = c, 3 = d)
d	These are data bits whose definition depend on the “i” bits in this packet according to the **Table B-36**. Note that if this vector is received on a long address and the “e” bit in this packet is not set, the decoder will send a Message Packet immediately following the Vector Packet. All message bits in the message packet are unused and should be ignored.

Table B-36 Short Instruction Vector Definition

$i_2i_1i_0$	d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	Description
000	a_3 a_2 a_1 a_0 f_6 f_5 f_4 f_3 f_2 f_1 f_0	Temporary address assignment[1]
001		Reserved
010		Reserved
011		Reserved
100		Reserved
101		Reserved

Table B-36 Short Instruction Vector Definition

$i_2 i_1 i_0$	d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	Description
110		Reserved
111		Reserved for test

Notes:
1. Assigned temporary address (a) and assigned frame (f). See **Appendix C** for additional information.
2. **i** = Instruction type—These bits define the meaning of the **d** bits in this packet.
   x = Unused bits—The value of these bits is not guaranteed.

Message Packet

The Message Field follows the Vector Field in the FLEX protocol. It contains the message data, checksum information, and may contain fragment numbers and message numbers. See **Appendix A** for additional information. If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in Message Packets. The ID of the Message Packet is the word number where the message word was received in the frame.

Table B-37 Message Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	WN6	WN5	WN4	WN3	WN2	WN1	WN0
2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

Note: **WN** = Word number of message word (3–87 decimal)—Describes the location of the message word in the frame
e is set if more than 2 bit errors are detected in the word.
p = Phase on which the message word was found (0 = a, 1 = b, 2 = c, 3 = d)
i = information bits of the message word—The definitions of these bits depend on the vector type and which word of the message is being received. See **Appendix A** for a detailed description of these bits.

Status Packet

The Status Packet contains various types of information that the host may require. The Status Packet will be sent to the host whenever the FLEXchip IC is polled and has no other data to send. The FLEXchip IC can also prompt the host to read the Status Packet due to events for which the FLEXchip IC was configured to send it (see **Configuration Packet** on page B-8 and **Control Packet** on page B-10 for a detailed description of the bits). The FLEXchip IC prompts the host to read a Status Packet if one of the following is true:

- The SMU bit in the Status Packet and the SME bit in the Configuration Packet are set.
- The MT bit in the Status Packet and the MTE bit in the Configuration Packet are set.
- The EOF bit in the Status Packet is set.
- The LBU bit in the Status Packet is set.
- The BOE bit in the Status Packet is set.

The ID of the Status Packet is 127 (decimal).

Table B-38 Status Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	0	1	1	1	1	1	1	1
2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
1	SM	LB	x	x	c_3	c_2	c_1	c_0
0	SMU	LBU	x	MT	x	EOF	x	BOE

FRAME INFO VALID (FIV)

The FIV bit is set when a valid frame info word has been received since becoming synchronous to the system and the f and c fields contain valid values. If this bit is clear, no valid frame info words have been received since the FLEXchip IC became synchronous to the system. This value will change from 0 to 1 at the end of block 0 of the frame in which the 1st frame info word was properly received. It will be cleared when the FLEXchip IC goes into Asynchronous mode. This bit is initialized to 0 when the FLEXchip IC is reset and when the FLEXchip IC is turned off by clearing the ON bit in the Control Packet.

CURRENT FRAME NUMBER (f)

This value is updated every frame regardless of whether the FLEXchip IC needs to decode the frame. This value will change to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SYNCHRONOUS MODE (SM)

This bit is set when the FLEXchip IC is synchronous to the system. The FLEXchip IC will set this bit when the first synchronization words are received. It will clear this bit when synchronization to the FLEX signal is lost. This bit is initialized to 0 when the FLEXchip IC is reset and when it is turned off by clearing the ON bit in the Control Packet.

LOW BATTERY (LB)

The LB bit is set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the Receiver Control Packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the Configuration Packet when the FLEXchip IC is turned on by setting the ON bit in the Control Packet.

CURRENT SYSTEM CYCLE NUMBER (c)

This value is updated every frame regardless of whether the FLEXchip IC needs to decode the frame.This value will change to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SYNCHRONOUS MODE UPDATE (SMU)

The SM bit is set if the SM bit has been updated in this packet. When the FLEXchip IC is turned on, this bit will be set when the first synchronization words are found (SM changes to 1) or when the first synchronization search window after the FLEXchip IC is turned on expires (SM stays 0). The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial A search window expires. After the initial Synchronous mode update, the SMU bit will be set whenever the FLEXchip IC transitions from / to Synchronous mode. Cleared when read. Changes in the SM bit due to turning off the FLEXchip IC will not cause the SMU bit to be set.This bit is initialized to 0 when the FLEXchip IC is reset.

LOW BATTERY UPDATE (LBU)

The LBU bit is set if the value on two consecutive reads of the LOBAT pin yielded different results and is cleared when read. The host controls when the LOBAT pin is read via the Receiver Control Packets. Changes in the LB bit due to turning on the FLEXchip IC will not cause the LBU bit to be set. This bit is initialized to 0 when the FLEXchip IC is reset.

MINUTE TIME-OUT (MT)

The MT bit is set if one minute has elapsed. The bit is cleared when read. This bit is initialized to 0 when the FLEXchip IC is reset.

END OF FRAME (EOF)

The EOF bit is set when the FLEXchip IC is in All Frame mode and the end of frame has been reached. The FLEXchip IC is in All Frame mode if the All Frames mode enable counter is non-zero, if any temporary address enabled counter is non-zero, or if the FAF bit in the All Frame Mode Packet is set. The bit is cleared when read. This bit is initialized to 0 when the FLEXchip IC is reset.

BUFFER OVERFLOW ERROR (BOE)

The BOE bit is set when information has been lost due to slow host response time. When the SPI transmit buffer on the FLEXchip IC overflows, the FLEXchip IC clears the transmit buffer, turns off decoding by clearing the ON bit in the Control Packet, and sets this bit. The bit is cleared when read. This bit is initialized to 0 when the FLEXchip IC is reset.

UNUSED BITS (x)

The value of these bits is not guaranteed.

Part ID Packet

The Part ID Packet is sent by the FLEXchip IC whenever the FLEXchip IC is disabled due to the checksum feature (see **Checksum Packet** on B-6). Since the FLEXchip IC is disabled after reset, this is the first packet that will be received by the host after reset. The ID of the Part ID Packet is 255 (decimal)**.**

Table B-39 Part ID Packet Bit Assignments

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	1	1	1	1	1	1	1	1
2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

MODEL (MDL)

This identifies the FLEXchip model. Current value is 0.

COMPATIBILITY ID (CID)

This value describes what other parts with the same model number are compatible with this part. Current value is 1. Any future versions of FLEXchip that have MDL set to 0 and CID_0 set to 1 will be 100% compatible to this version.

REVISION (REV)

This identifies the revision and manufacturer of the FLEXchip. Currently defined values are as follows.

Table B-40 FLEXchip Revisions

REV	Description
0	Pre-production Parts
1	Reserved
2	Motorola Semiconductor Products Sector Production Parts
3	Reserved
4	Motorola Semiconductor Products Sector Samples

APPENDIX C
APPLICATION NOTES

RECEIVER CONTROL

Introduction

The FLEXchip IC has eight programmable receiver control lines (S0–S7). The host has control of the receiver warm up and shut down timing, as well as all of the various settings on the control lines through configuration registers on the FLEXchip IC. The configuration registers for most settings allow the host to configure:

1. what setting is applied to the control lines,
2. how long to apply the setting, and
3. if the LOBAT input pin is polled before changing from the setting.

With this programmability, the FLEXchip IC is able to interface with many off-the-shelf receiver ICs, such as the MC13150 and MC3374. For details on the configuration of the receiver control settings, see **Receiver Control Configuration Packets** on page B-14.

Receiver Settings at Reset

The receiver control ports are three-state outputs that are set to the high-impedance state when the FLEXchip IC is reset and until the corresponding FRS bit in the Receiver Line Control Packet is set, or until the FLEXchip IC is turned on by setting the ON bit in the Control Packet. This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the FLEXchip IC. When the FLEXchip IC is turned on, the receiver control ports are driven to the settings configured by the Receiver Control Configuration Packets until the FLEXchip IC is reset again.

Normal Receiver Warm Up Sequence

The FLEXchip IC allows for up to six steps associated with warming up the receiver. When the FLEXchip IC turns on the receiver while decoding, it starts the warm up sequence 160 ms before it requires valid signals at the EXTS0 and EXTS1 input pins. The first step of the warm up sequence involves leaving the receiver control lines in the “Off” state for the amount of time programmed for “Warm Up Off Time”. At the end of the “Warm Up Off Time”, the first warm up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm up setting is applied to the receiver control lines for their corresponding time until a disabled warm up setting is found. At the end of the last used warm up setting, the “1600 sps Sync Setting” or the “3200 sps Sync Setting” is applied to the receiver control lines depending on the current state of the FLEXchip IC. The sum total of all of the used warm up times and the “Warm Up Off Time” must not exceed 160 ms. If it exceeds 160 ms, the FLEXchip IC will execute the receiver shut down sequence at the end of the 160 ms warm up period. **Figure C-1** below shows the receiver warm up sequence while decoding when all warm up settings are enabled.

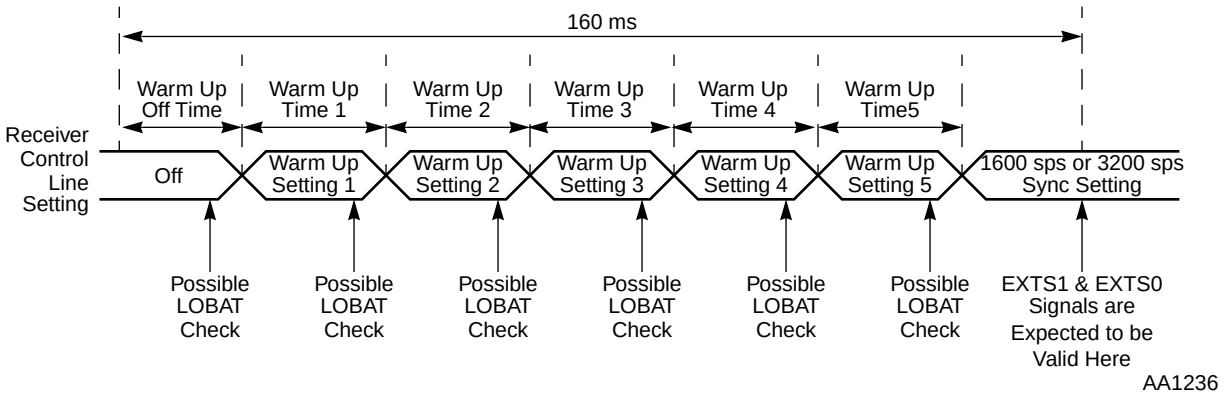


Figure C-1 Receiver Warm Up Sequence While Decoding.

First Receiver Warm Up Sequence

When the FLEXchip IC is turned on by setting the ON bit in the Control Packet, the first warm up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm up setting is applied to the receiver control lines for their corresponding time until a disabled warm up setting is found. Once a disabled warm up setting is found, the “3200 sps Sync Setting” is applied to the receiver control lines and the decoder does not expect valid signal until after the “3200 sps Sync Warm Up Time” has expired. **Figure C-2** on page C-3 below shows the receiver warm up sequence when the FLEXchip IC is first turned on and when all warm up settings are enabled.

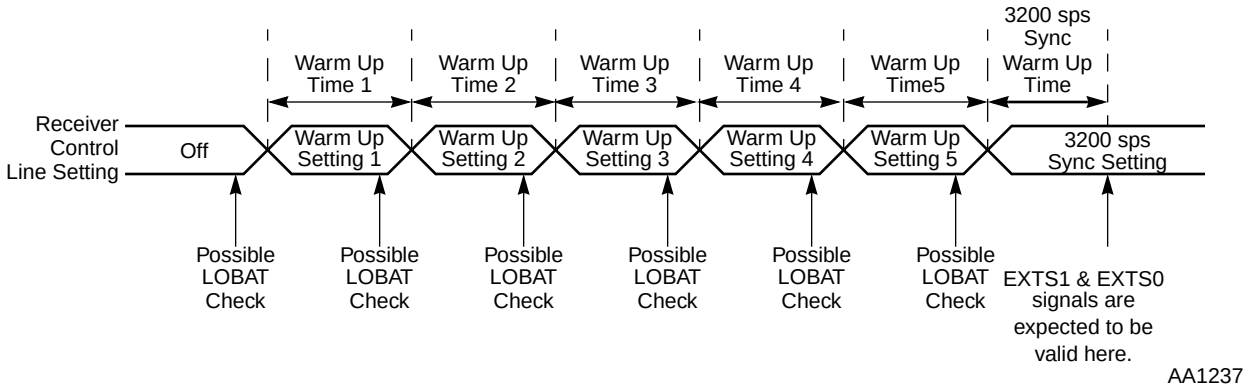


Figure C-2 Receiver Warm Up Sequence When Decoding Turned On

Receiver Shut Down Sequence

The FLEXchip IC allows for up to three steps associated with shutting down the receiver. When the FLEXchip IC decides to turn off the receiver, the first shut down setting, if enabled, is applied to the receiver control lines for the corresponding shut down time. At the end of the last used shut down time, the “Off” setting is applied to the receiver control lines. If the first shut down setting is not enabled, the FLEXchip IC will transition directly from the current “On” setting to the “Off” setting. **Figure C-3** shows the receiver turn off sequence when all shut down settings are enabled.

If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the Control Packet), the FLEXchip IC will execute the receiver shutdown sequence. If the FLEXchip IC is executing the shut down sequence when the FLEXchip IC is turned on (by setting the ON bit in the Control Packet), the FLEXchip IC will complete the shut down sequence before starting the warm up sequence.

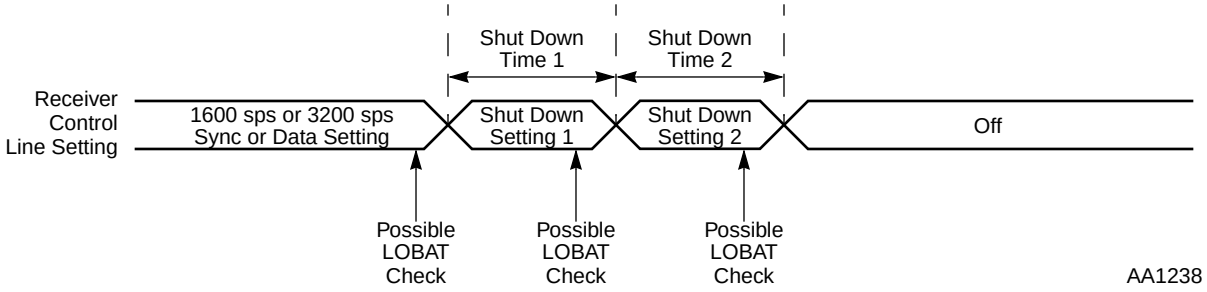


Figure C-3 Receiver Shut Down Sequence

Miscellaneous Receiver States

In addition to the Warm Up and Shut Down states, the FLEXchip IC has four other receiver states. When these settings are applied to the receiver control lines, the FLEXchip IC will be decoding the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the data the FLEXchip IC decodes. Because of this, there is no time setting associated with these settings. The four settings are as follows:

- **1600 sps Sync Setting**—This setting is applied when the FLEXchip IC is searching for a 1600 symbols per second signal.
- **3200 sps Sync Setting**—This setting is applied when the FLEXchip IC is searching for a 3200 symbols per second signal.
- **1600 sps Data Setting**—This setting is applied after the FLEXchip IC has found the C or $\overline{C}$ sync word in a 1600 symbols per second frame.
- **3200 sps Data Setting**—This setting is applied after the FLEXchip IC has found the C or $\overline{C}$ sync word in a 3200 symbols per second frame.

Figure C-4 below shows some examples of how these settings will be used in the FLEXchip IC.

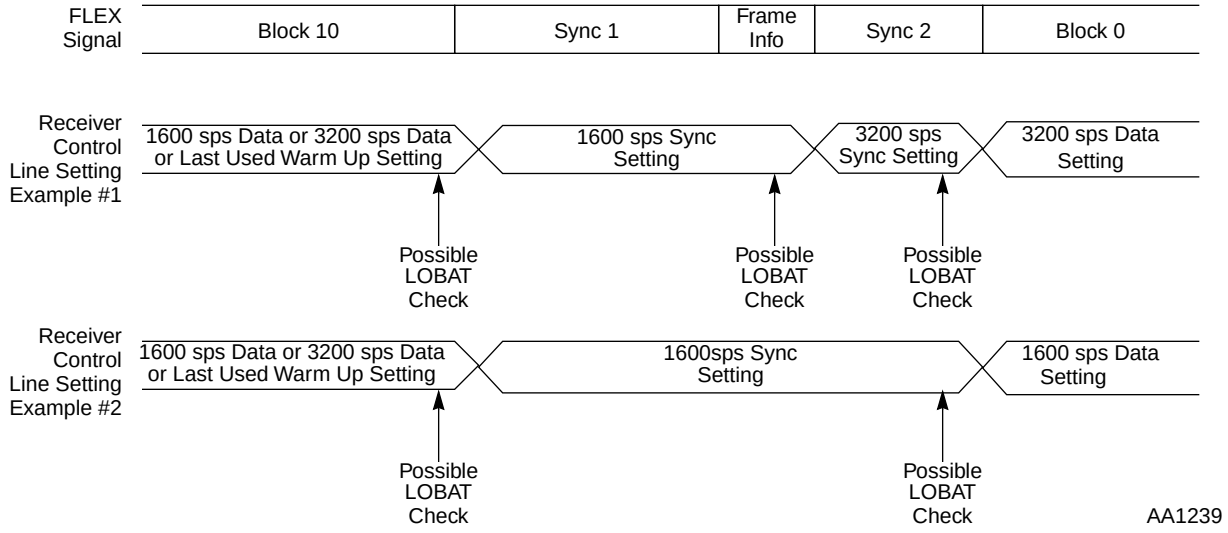


Figure C-4 Examples of Receiver Control Transitions

Low Battery Detection

The FLEXchip IC can be configured to poll the LOBAT input pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin will be read just before the FLEXchip IC changes the receiver control lines from that setting to another setting. The FLEXchip IC will send a Status Packet whenever the value on two consecutive reads of the LOBAT pin yields different results.

MESSAGE BUILDING

A simple message consists of an Address Packet followed by a Vector Packet indicating the word numbers of associated Message Packets.The tables below show a more complex example of receiving three Messages and two Block Information Word Packets in the first two blocks of a 2 phase 3200 bps, FLEX frame.

Note: The messages shown may be portions of fragmented or group messages. Furthermore, in the case of a 6400 bps FLEX signal, there would be four phases: A, B, C and D, and in the case of a 1600 bps signal there would be only a single phase A.

Table C-1 shows the block number, Word Number (WN) and word content of both phases A and C. Note contents of words not meant to be received by the host are left blank. Each phase begins with a block information word (WN 0), that is not sent to the host. The first message is in phase A and has an address (WN 3), vector (WN 7), and three message words (WN 9–11). The second message is also in phase A and has an address (WN 4), a vector (WN 8), and four message words (WN 12–15). The third message is in phase C and has a 2 word long address (WN 5–6) followed by a vector (WN 10) and three message words. Since the third message is sent on a long address, the first message word (WN 11) begins immediately after the vector. The vector indicates the location of the second and third message words (WN 14–15).

Table C-1 FLEX SIGNAL

BLOCK	Word Number	PHASE A	PHASE C
0	0	BIW1	BIW1
	1		BIW
	3	ADDRESS 1	BIW
	4	ADDRESS 2	
	5		LONG ADDRESS 3 WORD 1
	6		LONG ADDRESS 3 WORD 2
	7	VECTOR 1	
1	8	VECTOR 2	
	9	MESSAGE 1, 1	
	10	MESSAGE 1, 2	VECTOR 3
	11	MESSAGE 1, 3	MESSAGE 3, 1
	12	MESSAGE 2, 1	
	13	MESSAGE 2, 2	
	14	MESSAGE 2, 3	MESSAGE 3, 2
	15	MESSAGE 2, 4	MESSAGE 3, 3

Table C-2 shows the sequence of packets received by the host. The FLEXchip processes the FLEX signal one block at a time, and one phase at a time. Thus, the address and vector information in block 0 phase A is packetized and sent to the host in packets 1–3. Then information in block 0 phase C, two block information words and one long address, is packetized and sent to the host in packets 4–6. Packets 7–18 correspond to information in block 1, processed in phase A first and phase C second.

Table C-2 FLEXchip PACKET SEQUENCE

PACKET	PACKET TYPE	PHASE	WORD NUMBER	COMMENT
1st	ADDRESS	A	N.A. (7)	Address 1 has a vector located at WN 7.
2nd	ADDRESS	A	N.A. (8)	Address 2 has a vector located at WN 8.
3rd	VECTOR	A	7	Vector for Address 1: Message Words located at WN = 9 to 11, phase A
4th	BIW	C	N.A.	If BIWs enabled, then BIW packet sent
5th	BIW	C	N.A.	If BIWs enabled, then BIW packet sent
6th	LONG ADDRESS	C	N.A. (10)	Long Address 3 has a vector beginning in word 10 of phase C.
7th	VECTOR	A	8	Vector for Address 2: Message Words located at WN = 12 to 15, phase A
8th	MESSAGE	A	9	Message information for Address 1
9th	MESSAGE	A	10	Message information for Address 1
10th	MESSAGE	A	11	Message information for Address 1
11th	MESSAGE	A	12	Message information for Address 2
12th	MESSAGE	A	13	Message information for Address 2
13th	MESSAGE	A	14	Message information for Address 2
14th	MESSAGE	A	15	Message information for Address 2
15th	VECTOR	C	10	Vector for Long Address 3: Message Words located at WN = 14 - 15, phase C
16th	MESSAGE	C	11	Second word of Long Vector is first message information word of Address 3.
17th	MESSAGE	C	14	Message information for Address 3
18th	MESSAGE	C	15	Message information for Address 3

The first message is built by relating packets 1, 3, and 8–10. The second message is built by relating packets 2, 7, and 11–14. The third message is built by relating packets 6 and 15–18. Additionally, the host may process block information in packets 4 and 5 for time setting information.

BUILDING A FRAGMENTED MESSAGE

The longest message that will fit into a frame is eighty-four code words total of message data. Three alpha characters per word yields a maximum message of 252 characters in a frame assuming no other traffic. Messages longer than this value must be sent as several fragments.

Additional fragments can be expected when the “continue bit” in the 1st Message Word is set. This causes the pager to examine every following frame for an additional fragment until the last fragment with the continue bit reset is found. The only requirement relating to the placement in time of the remaining fragments is that no more than thirty-two frames (1 minute) or 128 frames (4 minutes) as indicated by the service provider may pass between fragment receptions.

Each fragment contains a check sum character to detect errors in the fragment, a fragment number 0, 1, or 2 to detect missing fragments, a message number to identify which message the fragment is a part, and the continue bit, which either indicates that more fragments are in queue or that the last fragment has been received. All of this information is described in **FLEX Message Word Definitions** on A-7.

The following describes the sequence of events between the host and the FLEXchip IC required to handle a fragmented message:

1. The host receives a vector indicating one of the following types:

Table C-3 Message Type Definition

$V_2V_1V_0$	Type
000	Secure
101	Alphanumeric
110	Hex / Binary

2. The FLEXchip IC increments the All Frame mode counter inside the FLEXchip IC and begin to decode all of the following frames.
3. The host receives the Message Packet(s) contained within that frame, followed by a Status Packet. The host must decide based on the Message Packet to return to normal decoding operation. If the message is indicated as fragmented by the Message Continued Flag “C” being set in the Message Packet for a Secure, Alphanumeric or Hex /Binary Message, then the host does not decrement the All Frame mode counter at this time. The host decrements the counter if the Message Continued Flag “C” is clear by writing the All Frame Mode Packet to the FLEXchip IC with the “DAF” bit = 1. If no other fragments, temporary addresses are pending or the FAF bit is clear in

the All Frame Mode Register, then the FLEXchip IC returns to normal operation.

4. The FLEXchip IC continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of the frame. If the message is indicated as fragmented by the Message Continued Flag "C" in the Message Packet for a Secure, Alphanumeric or Hex/Binary Message then the host remains in the Receive mode expecting more information from the FLEXchip IC.
5. After the host receives the second and subsequent fragment with the Message Continued Flag "C" = 1, it should decrement the All Frame mode counter by sending an All Frame Mode Packet to the FLEXchip IC with the "DAF" bit = 1. Alternatively, the host may choose to decrement the counter at the end of the entire message by decrementing the counter once for each fragment received.
6. When the host receives a Message Packet with the Message Continued Flag "C" = 0, it will send two All Frame Mode Packets to the FLEXchip IC with the "DAF" bit = 1. The two packets decrement the count for the first fragment and the last fragment. This decrements the All Frame mode counter to zero, if no other fragmented messages, or temporary addresses are pending or the FAF bit is clear in the All Frame Mode Register, and returns the FLEXchip IC to normal operation.
7. The above process must be repeated for each occurrence of a fragmented message. The host must keep track of the number of fragmented messages being decoded and insure the all frame mode counter decrements after each fragment or after each fragmented message.

Table C-4 Alphanumeric Message Without Fragmentation

PACKET	PACKET TYPE	PHASE	All Frame Counter	COMMENT
1st	ADDRESS 1	A	0	Address 1 is received
2nd	VECTOR 1	A	1	Vector = Alphanumeric Type
3rd	MESSAGE	A	1	Message Word received "C" bit = 0; No more fragments are expected.
4th	TBD		0	Host writes All Frame Mode Packet to the FLEXchip IC with the "DAF" Bit = 1

Note: TBD—Host Initiated Packet. The FLEXchip IC returns a packet according to **Decoder-to-Host Packet Descriptions** on page B-22.

Table C-5 Alphanumeric Message with Fragmentation

PACKET	PACKET TYPE	PHASE	All Frame Counter	COMMENT
1st	ADDRESS 1	A	0	Address 1 is received
2nd	VECTOR 1	A	1	Vector = Alphanumeric Type
3rd	MESSAGE	A	1	Message Word received "**C**" bit = 1, Message is fragmented, more expected
4th	STATUS		1	End of Frame Indication (**EOF** = 1)
5th	ADDRESS 1	B	1	Address 1 is received
6th	VECTOR 1	B	2	Vector = Alphanumeric Type
7th	MESSAGE	B	2	Message Word received "**C**" bit = 1, Message is fragmented, more expected.
8th	TBD		1	Host writes All Frame Mode Packet to the FLEXchip IC with the "**DAF**" bit = 1
9th	STATUS		1	End of Frame Indication (**EOF** = 1)
10th	ADDRESS 1	A	1	Address 1 is received
11th	VECTOR 1	A	2	Vector = Alphanumeric type
12th	MESSAGE	A	2	Message Word received "**C**" bit = 0, No more fragments are expected.
13th	TBD		1	Host writes All Frame Mode Packet to the FLEXchip IC with the "**DAF**" bit = 1
14th	TBD		0	Host writes All Frame Mode Packet to the FLEXchip IC with the "**DAF**" bit = 1

Note: TBD—Host Initiated Packet. The FLEXchip IC returns a packet according to **Decoder-to-Host Packet Descriptions** on page B-22.

OPERATION OF A TEMPORARY ADDRESS

Group Messaging

The FLEX protocol allows for a dynamic group call for the purpose of sending a common message to a group of paging devices. The dynamic group call approach assigns a “Temporary Address”, using the personal address and the short instruction vector. The temporary address must be disabled by the host after the message is completed.

The FLEX protocol specifies sixteen addresses for the dynamic group call, which may be temporarily activated in a specific future frame (If the designated frame is equal to the present frame, the host is to interpret this as the next occurrence of this frame 4 minutes in the future.) The temporary address is valid for one message starting in the specified frame and remaining valid throughout the following frames to the completion of the message. If the message is not found in the specified frame (frame defined by a full 7-bit frame number), the host must disable the assigned temporary address.

The following describes the sequence of events between the Host and the FLEXchip IC required to handle a temporary address:

1. Following an Address Packet, the host will receive a Vector Packet with $V_2V_1V_0 = 001$ and $i_2i_1i_0 = 000$ for a Short Instruction Vector indicating a temporary address has been assigned to this pager. The vector packet will indicate which temporary address is assigned and the frame in which the temporary address is expected.
2. The FLEXchip IC will increment the corresponding temporary address counter and begin to decode all of the following frames.
3. The FLEXchip IC continues to decode all of the frames and passes any address information, vector information, and message information to the host, followed by a status packet indicating the end of each frame and the current frame number.
4. There are several scenarios that may occur with temporary addresses.
    a. The temporary address is not found in the frame assigned and therefore the host must terminate the Temporary Address mode by sending an All Frame Mode Packet to the FLEXchip IC with the “DTA” bit of the particular temporary address set.
    b. The temporary address is found in the frame it was assigned and was not a fragmented message. Again, the host must terminate the Temporary Address mode by sending an All Frame Mode Packet to the FLEXchip IC with the “DTA” bit of the particular temporary address set.

c. The temporary address is found in the assigned frame and it is a fragmented message. In this case, the host must follow the rules for Operation of a Fragmented Message and determine the proper time to stop the All Frame mode operation. In this case, the host must write to the "DAF" bit with a "1" and the appropriate "DTA" bit with a "1" in the All Frame Mode Register in order to terminate both the fragmented message and the temporary address.

5. The above operation is repeated for every temporary address.

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