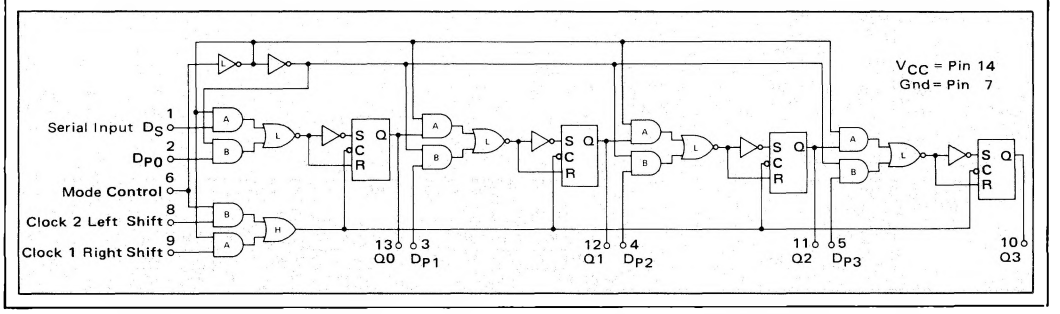
MC5495 • MC7495

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for To-116 plastic package (Case 605) MC7495 only.

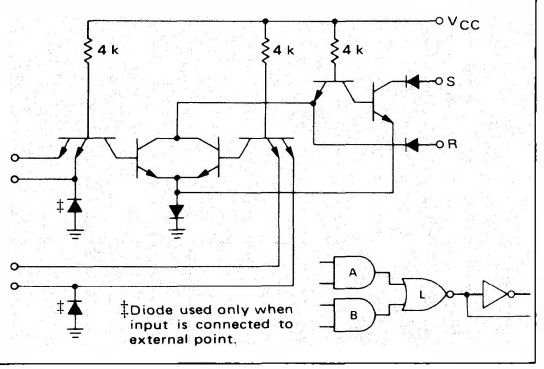
Input Loading Factor:
Mode Control = 2
Other Inputs = 1
Output Loading Factor = 10
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = 25 ns typ
Maximum Shift Frequency = 31 MHz typ

The MC5495/7495 performs as a right-shift or left-shift register, or a parallel-in/parallel-out storage register, depending on the logic level present at the Mode Control input.

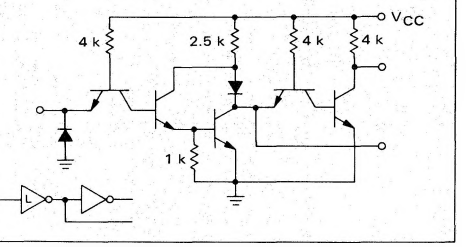
The device consists of R-S master-slave flip-flops, high and low-level gates and inverters interconnected as shown by the logic diagram.



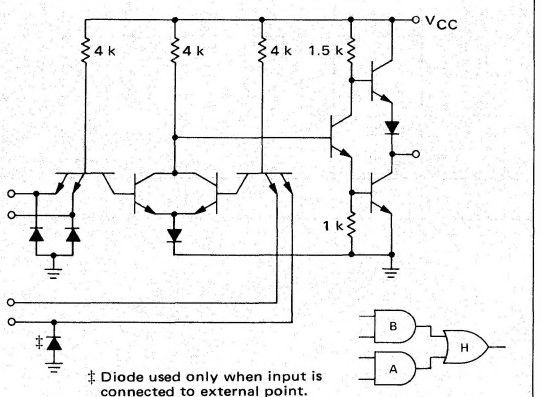
LOW-LEVEL "AND-OR-INVERT" GATE WITH INVERTER DRIVER



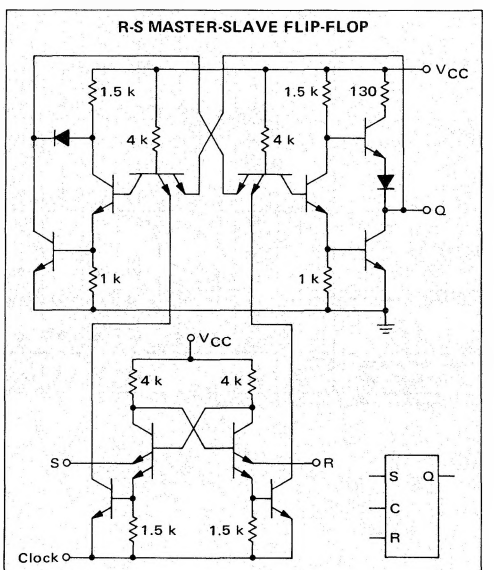
LOW-LEVEL INVERTER



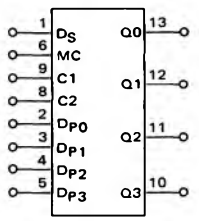
HIGH-LEVEL "AND-OR" GATE



R-S MASTER-SLAVE FLIP-FLOP



ELECTRICAL CHARACTERISTICS

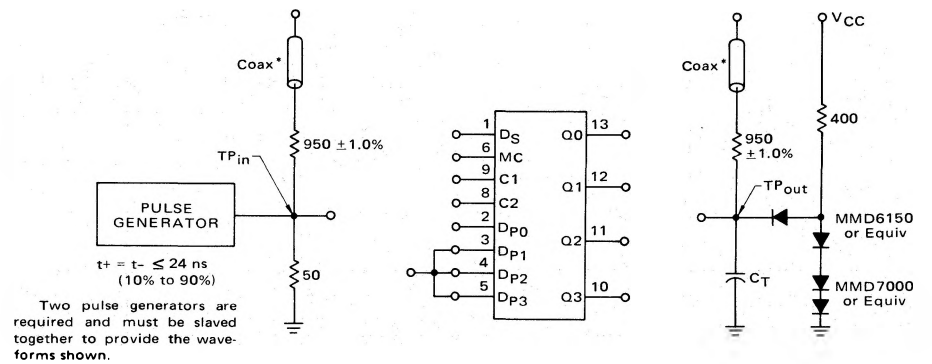


	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA		Volts								
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5495	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5
MC7495	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5495 Test Limits −55 to +125°C Min	Max	Unit	MC7495 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																					
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	1	–	–	–	–	–	–	–	14	–	6,7
		2	–			–			–	–	2	–	–	6	–	–	–	–		–	7
		3	–			–			–	–	3	–	–		–	–	–	–		–	
		4	–			–			–	–	4	–	–		–	–	–	–		–	
		5	–			–			–	–	5	–	–		–	–	–	–		–	
		6	–	-3.2		–	-3.2		–	–	6	–	–	8	–	–	–	–		–	
		8	–	-1.6		–	-1.6		–	–	8	–	–	6	–	–	–	–		–	
		9	–	-1.6		–	-1.6		–	–	9	–	–	–	–	–	–	–		–	6,7
Leakage Current	I_{R1}	1	–	40	μAdc	–	40	μAdc	–	–	–	1	–	6	–	–	–	–	14	–	7
		2	–			–			–	–	–	2	–	–	–	–	–	–		–	6,7
		3	–			–			–	–	–	3	–	–	–	–	–	–		–	
		4	–			–			–	–	–	4	–	–	–	–	–	–		–	
		5	–			–			–	–	–	5	–	–	–	–	–	–		–	
		6	–	80		–	80		–	–	–	6	–	–	–	–	–	–		–	7
		8	–	40		–	40		–	–	–	8	–	–	–	–	–	–		–	6,7
		9	–	40		–	40		–	–	–	9	–	6	–	–	–	–		–	7
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	1	6	–	–	–	–	14	–	7
		2	–			–			–	–	–	–	2	–	–	–	–	–		–	6,7
		3	–			–			–	–	–	–	3	–	–	–	–	–		–	
		4	–			–			–	–	–	–	4	–	–	–	–	–		–	
		5	–			–			–	–	–	–	5	–	–	–	–	–		–	
		6	–			–			–	–	–	–	6	–	–	–	–	–		–	7
		8	–			–			–	–	–	–	8	–	–	–	–	–		–	6,7
		9	–			–			–	–	–	–	9	6	–	–	–	–		–	7
Output																					
Output Voltage	V_{OL}	10	–	0.4	Vdc	–	0.4	Vdc	10	–	–	–	–	–	–	2,3,4,5	–	14	–	8	7
		11	–			–			11	–	–	–	–	–	–	1,6	–		–		
		12	–			–			12	–	–	–	–	–	–	2,3,4,5	–		–		
		13	–			–			13	–	–	–	–	–	–	1,6	–		–		
		13	–			–			13	–	–	–	–	–	–	1,6	–		–	9	
	V_{OH}	10	2.4	–	Vdc	2.4	–	Vdc	–	10	–	–	–	–	2,3,4,5,6	–	–	14	–	8	7
		11	–			–			–	11	–	–	–	–		–	–		–		
		12	–			–			–	12	–	–	–	–		–	–		–		
		13	–			–			–	13	–	–	–	–		–	–		–		
		13	–			–			–	13	6	–	–	–		–	–		–	9	
Short-Circuit Current	I_{SC} †	10	-18	-57	mAdc	-18	-57	mAdc	–	–	–	3,4,5,6	–	–	–	–	–	–	14	8	7,10
		11	–			–			–	–	–		–	–	–	–	–	–			7,11
		12	–			–			–	–	–		–	–	–	–	–	–			7,12
		13	–			–			–	–	–		–	–	–	–	–	–			7,13
Power Requirements																					
Power Supply Drain	I_{PD}	14	–	72	mAdc	–	82	mAdc	–	–	2,3,4,5	6	–	–	–	–	14	–	–	8,9	7

†Only one output should be shorted at a time.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

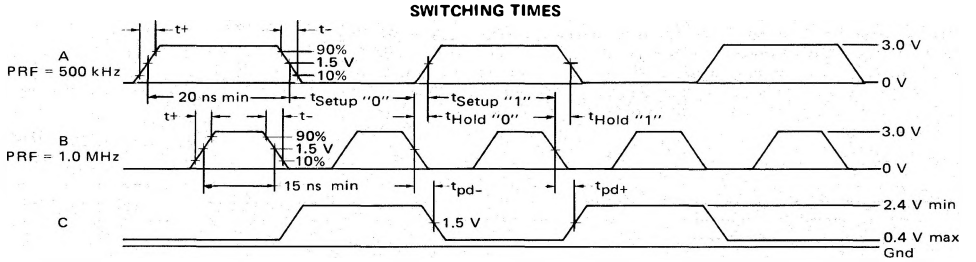


Two pulse generators are required and must be slaved together to provide the waveforms shown.

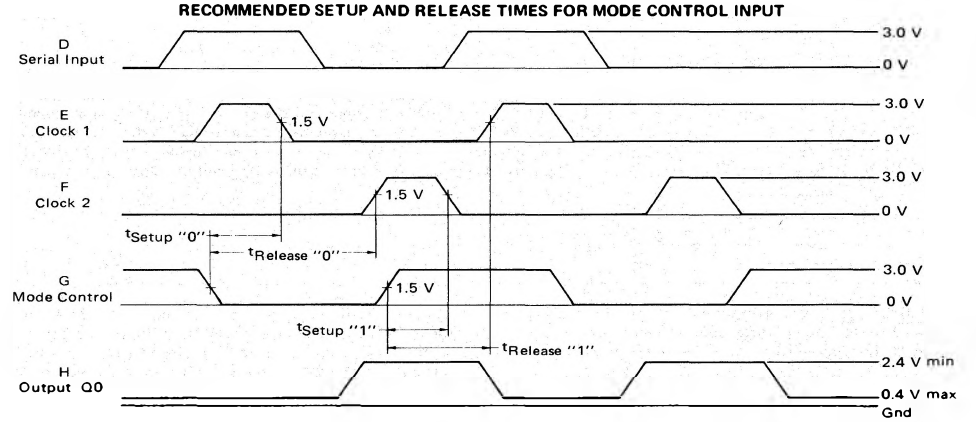
* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

SWITCHING TIMES



RECOMMENDED SETUP AND RELEASE TIMES FOR MODE CONTROL INPUT



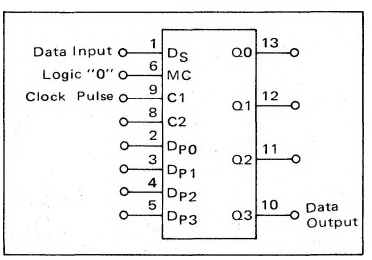
SWITCHING TIME TEST PROCEDURES (T_A = 25°C)
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT					OUTPUT	VALUE			
		D_S Pin 1	D_{P0}, D_{P1}, D_{P2} or D_{P3} Pin 2, 3, 4, or 5	MC Pin 6	C2 Pin 8	C1 Pin 9	Q0, Q1, Q2 or Q3 Pin 13, 12, 11, or 10	Min	Typ	Max	Unit
Propagation Delay Time Clock to Output	t_{pd+}	A	–	0.4 V	Gnd	B	C	–	26	35	ns
		–	A	2.4 V	B	Gnd	C	–	26	35	ns
	t_{pd-}	A	–	0.4 V	Gnd	B	C	–	26	35	ns
		–	A	2.4 V	B	Gnd	C	–	26	35	ns
Maximum Shift Frequency	f_{max}	Tested during t_{pd} tests.						20	31	–	MHz
Setup Time, Serial or Parallel Inputs	t_{Setup}							–	10	20	ns
Hold Time, Serial or Parallel Inputs	t_{Hold}							–	-10	0	ns
			D_{P0}				Q0				
Setup Time, Mode Control Clock 1	t_{Setup}	D	0.4 V	G	0.4 V	E	H	–	–	20	ns
Clock 2		D	0.4 V	G	F	0.4 V	H	–	–	20	ns
Release Time, Mode Control Clock 1	$t_{Release}$	D	0.4 V	G	0.4 V	E	H	–	–	10	ns
Clock 2		D	0.4 V	G	F	0.4 V	H	–	–	10	ns

OPERATING CHARACTERISTICS

FIGURE 1 – SERIAL RIGHT-SHIFT OPERATION

For serial right-shift operation, the Mode Control input is held at a logic "0". This enables the "A" AND gates and inhibits the "B" gates, coupling the output of each flip-flop to the input of the succeeding flip-flop, and inhibiting all four parallel data inputs and Clock 2. Serial data is entered at D_S and the clock pulse applied at Clock 1. The input information shifts one output to the right on each negative edge of the clock pulse.



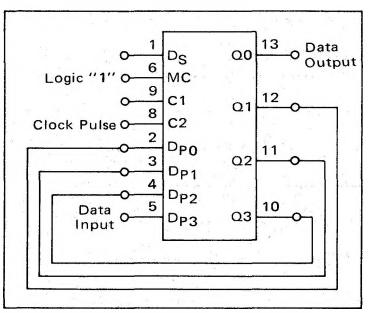


FIGURE 2 – SERIAL LEFT-SHIFT OPERATION

For serial left-shift operation, the Mode Control input is held at a logic "1". This enables the "B" AND gates and inhibits the "A" AND gates, decoupling the output of each flip-flop from the input of the succeeding flip-flop. The output of each flip-flop must be externally connected to the parallel data input of the preceding flip-flop. Serial data is entered at input D_{P3} and the clock pulse applied at Clock 2.

A parallel-in/parallel-out storage register is obtained by applying a logic "1" level to the Mode Control input, applying parallel data at inputs D_{P0}, D_{P1}, D_{P2}, and D_{P3}, and a clock pulse at Clock 2.

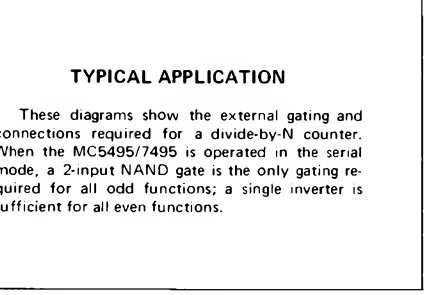
In either mode, information is transferred to the outputs of the device on the negative transition of the clock pulse.

The Mode Control must be in a logic "0" state 20 ns (t_{Setup} "0") prior to the negative transition of the Clock 1 pulse, and in a logic "1" state 20 ns (t_{Setup} "1") prior to the negative transition of the Clock 2 pulse. The Mode control must also be in a logic "0" state 10 ns ($t_{Release}$ "0") prior to the positive transition of the Clock 2 pulse, and in a logic "1" state 10 ns ($t_{Release}$ "1") prior to the positive transition of the Clock 1 pulse.

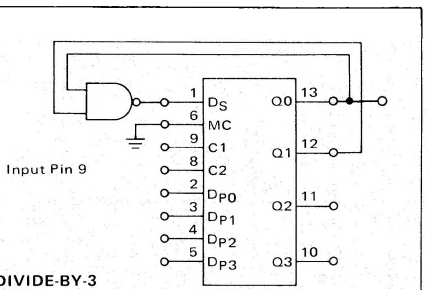
Clock 1 must be high when the Mode Control goes from high to low. Clock 2 must be high when the Mode Control goes from low to high.

TYPICAL APPLICATION

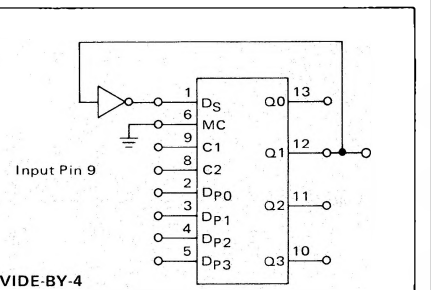
These diagrams show the external gating and connections required for a divide-by-N counter. When the MC5495/7495 is operated in the serial mode, a 2-input NAND gate is the only gating required for all odd functions; a single inverter is sufficient for all even functions.



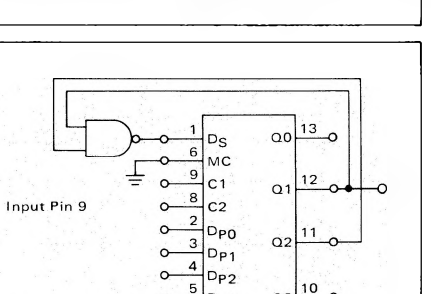
DIVIDE-BY-2



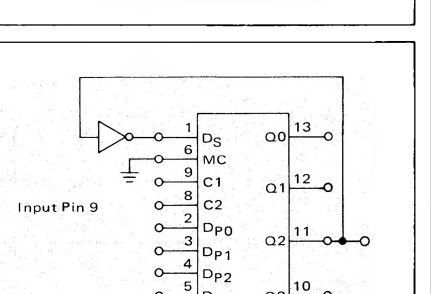
DIVIDE-BY-3



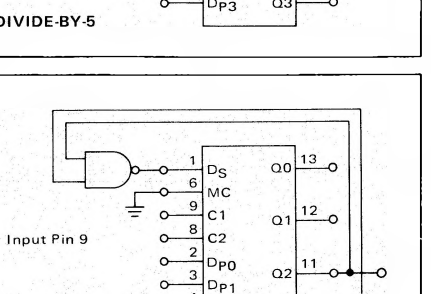
DIVIDE-BY-4



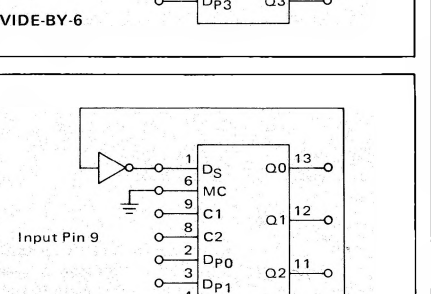
DIVIDE-BY-5



DIVIDE-BY-6



DIVIDE-BY-7



DIVIDE-BY-8