

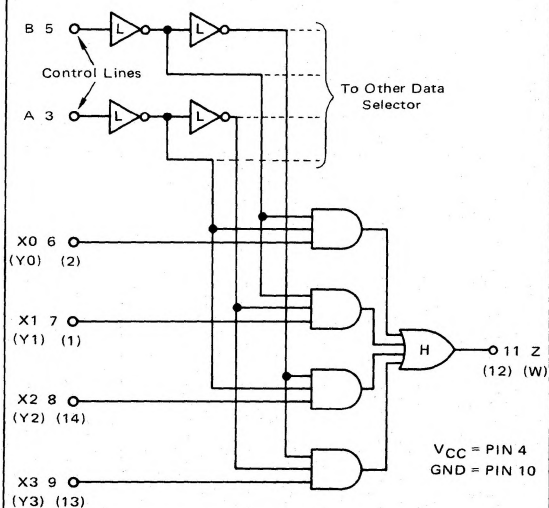
DUAL 4-CHANNEL DATA SELECTOR

MC4300/MC4000 series

MC4300F,L*
MC4000F,L,P*

1/2 OF DEVICE SHOWN

(Numbers and symbols in parenthesis are for other half of device.)



$$Z = ABX0 + \bar{A}\bar{B}X1 + \bar{A}BX2 + A\bar{B}X3$$

$$W = ABY0 + \bar{A}\bar{B}Y1 + \bar{A}BY2 + A\bar{B}Y3$$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg

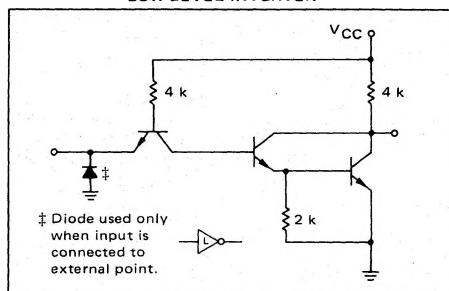
This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR gates and low-level inverters. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the output.

Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

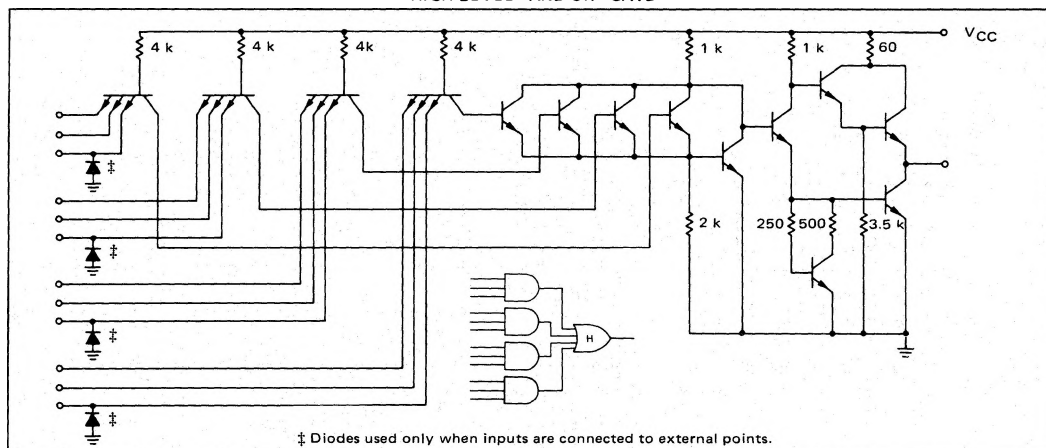
TYPICAL PROPAGATION DELAY TIMES (ns) T_A = 25°C

INPUT	Z	CONDITIONS
A	18	X0 = X2 = X3 = logic "0", X1 = logic "1". A and B are defined by the logic equations.
B	15	
X1	11	

LOW-LEVEL INVERTER



HIGH-LEVEL "AND-OR" GATE

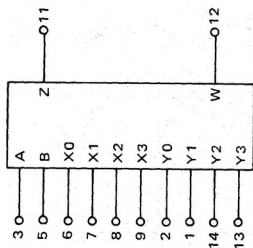


*F suffix = TO-86 ceramic flat package (Case 607).

L suffix = TO-116 ceramic dual in-line package (Case 632).

P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

[illegible]

MC4300F,L, MC4000F,L,P (continued)

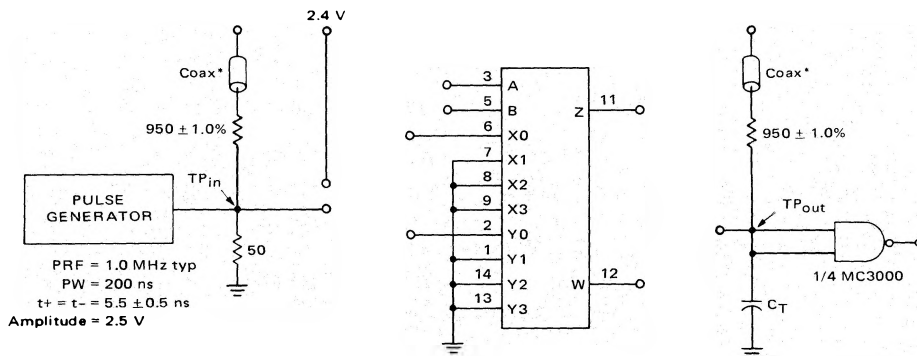
INPUT AND OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

FAMILY	MC4300 INPUT LOADING FACTOR	MC4300 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.23	12.3
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15 *	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

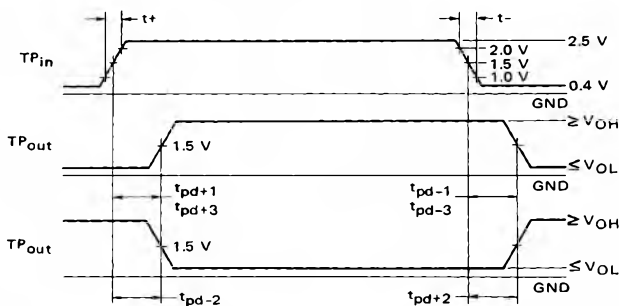
SWITCHING TIME TEST CIRCUIT



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS



MC4300F,L, MC4000F,L,P (continued)

TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 – FOUR-GATE DELAY versus TEMPERATURE

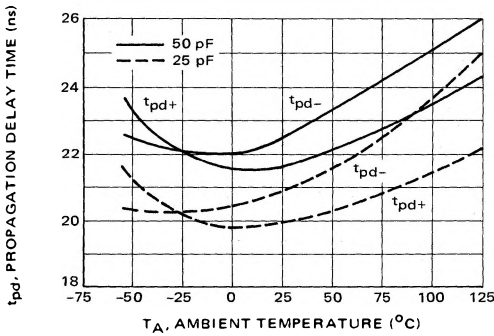


FIGURE 2 – THREE-GATE DELAY versus TEMPERATURE

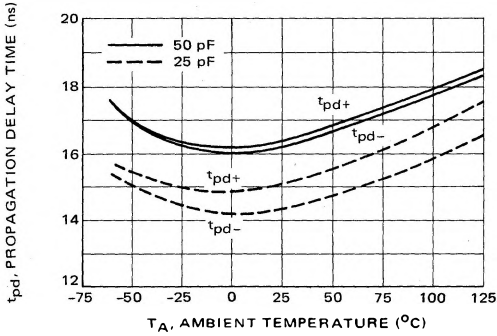


FIGURE 3 – TWO-GATE DELAY versus TEMPERATURE

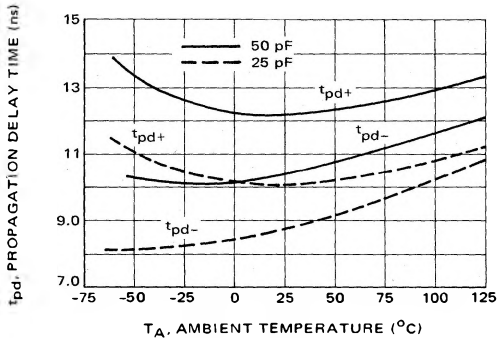


FIGURE 4 – DELAY versus LOAD CAPACITANCE

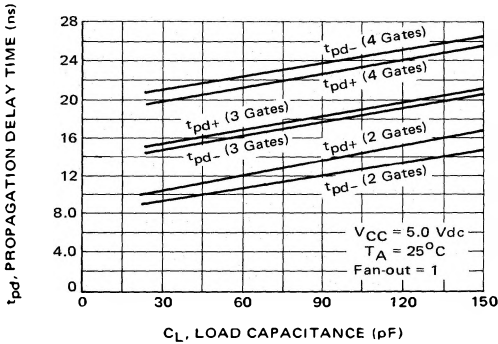
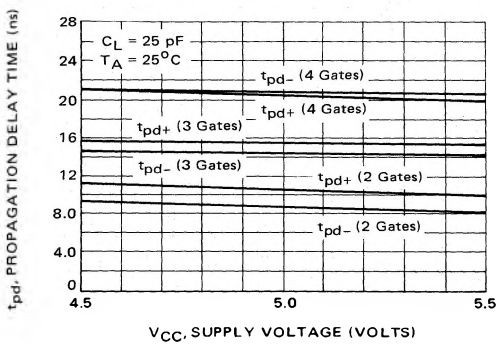
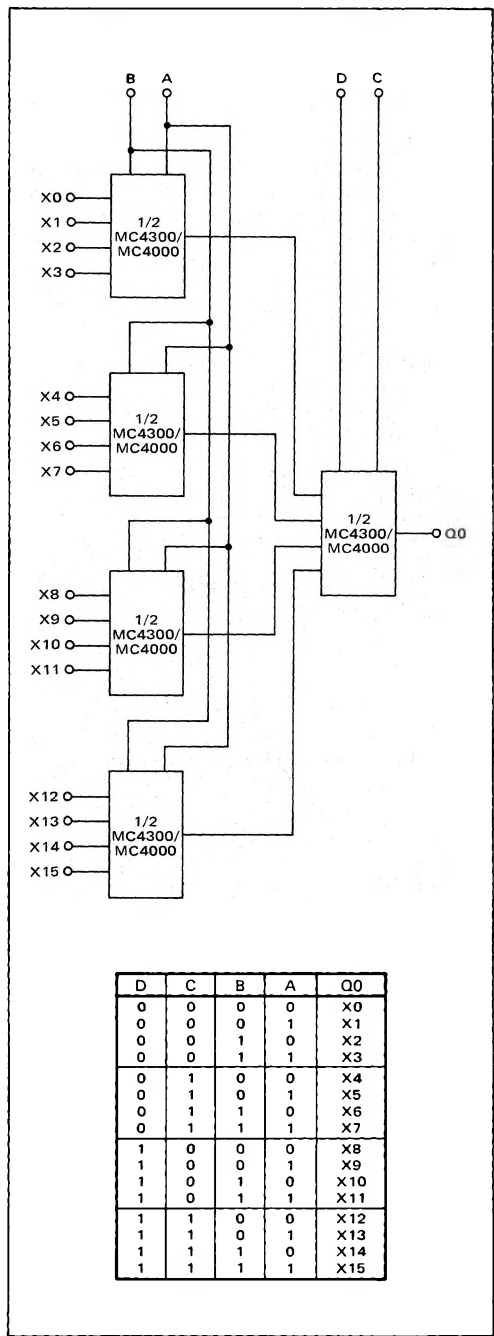


FIGURE 5 – DELAY versus SUPPLY VOLTAGE



MC4300F,L, MC4000F,L,P (continued)

FIGURE 6 – 1-BIT 16-LINE DATA SELECTOR



TYPICAL APPLICATIONS

Data selection from one of sixteen inputs can be accomplished by using multiple MC4300/4000 data selector units, as shown in Figure 6.

An N-bit data selector network may be realized by paralleling N/2 data selectors as shown in Figure 7. Each bit is selected from its own group of four different inputs; therefore from each dual data selector we can obtain two bits. Thus, for N bits we need N/2 dual 4-line selectors.

FIGURE 7 – N-BIT 4-LINE DATA SELECTOR

