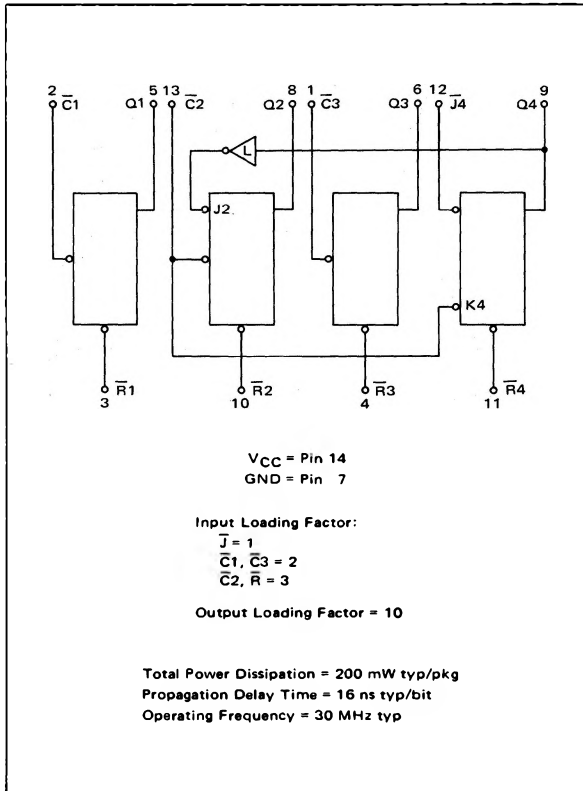


4-BIT UNIVERSAL COUNTER

MC4300/MC4000 series

MC4023F, L, P*

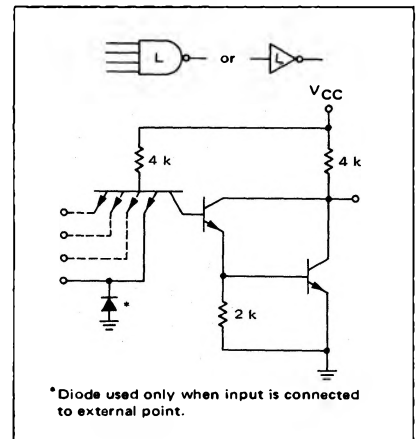
ADVANCE INFORMATION/NEW PRODUCT



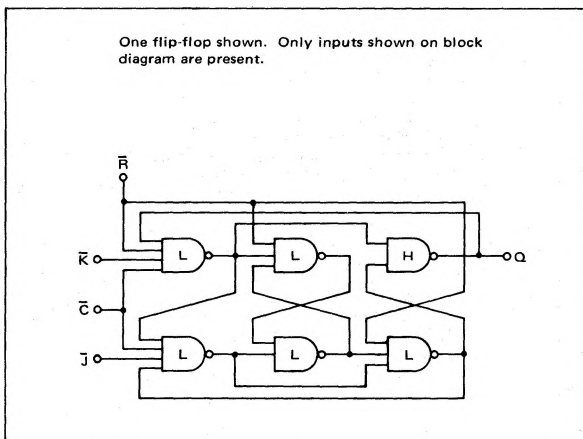
This device is a 4-bit counter with internally connected feedback. Inputs and outputs can be connected to count to any number between two and twelve except seven and eleven. Reset inputs are provided on each flip-flop to allow direct setting of the Q outputs to zero any time during the counting cycle.

Each flip-flop in the counter is built from high and low-level gates as shown by the logic diagram. The flip-flops and the feedback inverter are connected as shown by the block diagram to provide minimum power dissipation and maximum drive capability.

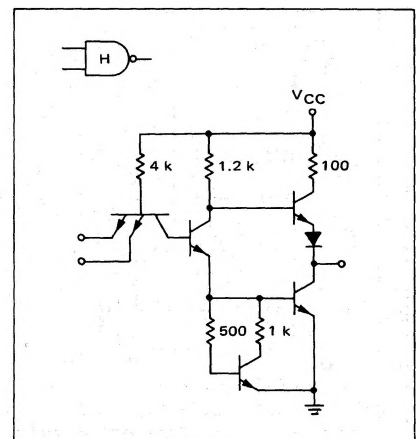
LOW-LEVEL GATE



LOGIC DIAGRAM



HIGH-LEVEL GATE



* F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

MC4023F, L, P (continued)

INPUT LOADING and OUTPUT DRIVING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT DRIVE FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family

** Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS
(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input Forward Current – J C1, C3 C2, R J C1, C3 C2, R	I _{F1}	-1.6 mA _{dc} max	V _{in} = 0.4 V _{dc} , V _{CC} = 5.25 V _{dc}
		-3.2 mA _{dc} max	
		-4.8 mA _{dc} max	
	I _{F2}	-1.4 mA _{dc} max -2.8 mA _{dc} max -4.2 mA _{dc} max	V _{in} = 0.4 V _{dc} , V _{CC} = 4.75 V _{dc}
Leakage Current – J C1, C3 C2, R	I _R	40 µA _{dc} max 80 µA _{dc} max 120 µA _{dc} max	V _{in} = 2.5 V _{dc} , V _{CC} = 5.25 V _{dc}
Breakdown Voltage	BV _{in}	5.5 V _{dc} max	I _{in} = 1.0 mA _{dc} , V _{CC} = 5.25 V _{dc} , T _A = 25°C
Clamp Voltage	V _D	-1.5 V _{dc} max	I _D = -10 mA _{dc} , V _{CC} = 4.75 V _{dc} , T _A = 25°C
Threshold Voltage	V _{th} "1"	2.0 V _{dc} 1.8 V _{dc}	T _A = 0°C T _A = +25°C, or T _A = 75°C
	V _{th} "0"	1.1 V _{dc} 0.9 V _{dc}	T _A = 0°C, or T _A = +25°C T _A = +75°C
Output Output Voltage	V _{OL}	0.4 V _{dc} max 0.4 V _{dc} max	I _{OL} = 16 mA _{dc} , V _{CC} = 4.75 V _{dc} I _{OL} = 17.6 mA _{dc} , V _{CC} = 5.25 V _{dc}
	V _{OH}	2.5 V _{dc} max	I _{OH} = -1.6 mA _{dc} , V _{CC} = 4.75 V _{dc}
Short-Circuit Current	I _{SC}	-20 to -65 mA _{dc}	V _{out} = 0 V _{dc} , V _{CC} = 5.0 V _{dc}

MC4023F, L, P (continued)

COUNTING SEQUENCES

DIVIDE BY 3

C2	Q2	Q4
0	0	0
1	1	0
2	0	1

DIVIDE BY 4

C1	Q1	Q3
0	0	0
1	1	0
2	0	1
3	1	1

DIVIDE BY 6

C1	Q1	Q2	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1

DIVIDE BY 12

C3	Q3	Q1	Q2	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1

DIVIDE BY 2: Use flip-flop 1 or 3.

DIVIDE BY 3: Use flip-flops 2 and 4, connected as shown. The input signal is applied to C2; the output is taken from Q4.

DIVIDE BY 4: Use flip-flops 1 and 3; connect Q1 to C3. Apply the input signal to C1.

DIVIDE BY 6: In addition to the connection for divide by 3, connect Q1 to C2. Apply the input signal to C1.

DIVIDE BY 12: In addition to the connections for divide by 6, connect Q3 to C1. Apply the input signal to C3.

DIVIDE BY 5

C2	Q2	Q3	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

DIVIDE BY 8

C1	Q1	Q2	Q3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

DIVIDE BY 10

C1	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

DIVIDE BY 5: Connect flip-flops 2, 3, and 4 as shown. The input signal is applied to C2; the output is taken from Q4.

DIVIDE BY 8: Connect flip-flops 2 and 3 as shown for divide by 5, but do not connect Q3 to J4. Connect Q1 to C2. The input signal is applied to C1; the output is taken from Q3.

DIVIDE BY 10: In addition to the connections for divide by 5, connect Q1 to C2. Apply the input signal to C1.

DIVIDE BY 9

C2	Q2	Q3	Q1	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

DIVIDE BY 9: The input signal is applied to C2; the output is taken from Q4.