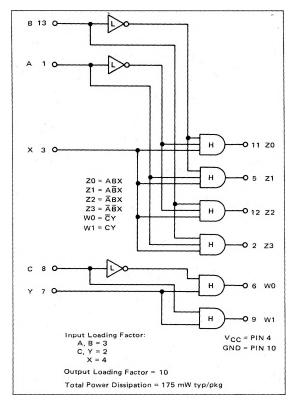
DUAL DATA DISTRIBUTOR

### MC4002F, L, P\*



#### **ADVANCE INFORMATION/NEW PRODUCT**

This device consists of two data distributors constructed from high-level AND gates and low-level inverters. One distributes information present at the input line to one of four output lines; the other distributes information present at the input to one of two output lines. The routing path is selected by the logic signals at the control lines A, B or C.

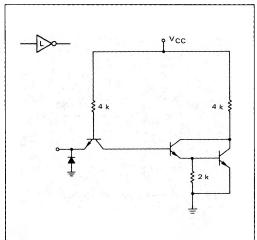
Data distributors are useful in applications where digital data is to be routed from a single register or location to one of several registers or locations for processing.

# TYPICAL PROPAGATION DELAY TIMES (ns) $T_{\text{A}} = 25^{\text{O}}\text{C}$

INPUT	20	Z1	Z2	Z3
А	14.5	10.5	14.5	10.5
8	14.5	14.5	10.5	10.5
X	10.5	10.5	10.5	10.5

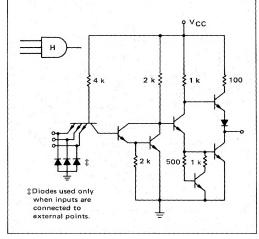
INPUT	wo	W1	
С	14.5	10.5	
Y	10.5	10.5	

#### LOW-LEVEL INVERTER



\*F suffix = TO-86 ceramic flat package (Case 607). L suffix = TO-116 ceramic dual in-line package (Case 632).

### HIGH-LEVEL "AND" GATE



P suffix = TO-116 plastic dual in-line package (Case 605).

## INPUT and OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000 MC400	1.0	10 10
MC2000	0.67	6
MC3000 MC7400	0.7 1.0	8 10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

#### DC ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — A, B		-4.8 mAdc max	
C, Y	<sup>1</sup> F1	-3.2 mAdc max	V <sub>in</sub> = 0.4 Vdc, V <sub>CC</sub> = 5.25 Vdc
<u>x</u>		-6.4 mAdc max	
A, B		-4.2 mAdc max	
C, Y	IF2	-2.8 mAdc max	V <sub>in</sub> = 0.4 Vdc, V <sub>CC</sub> = 4.75 Vdc
x		-5.6 mAdc max	
Leakage Current – A, B		120 µAdc max	
C, Y	¹R	80 µAdc max	V <sub>in</sub> = 2.5 Vdc, V <sub>CC</sub> = 5.25 Vdc
x		160 µAdc max	
Breakdown Voltage	BVin	5.5 Vdc max	I <sub>in</sub> = 1.0 mAdc, V <sub>CC</sub> = 5.25 Vdc, T <sub>A</sub> = 25 <sup>o</sup> C
Clamp Voltage	V <sub>D</sub>	-1.5 Vdc max	$I_D = -10 \text{ mAdc}, V_{CC} = 4.75 \text{ Vdc}, T_A = 25^{\circ}\text{C}$
Threshold Voltage	V <sub>th</sub> "1"	2.0 Vdc	T <sub>A</sub> = 0°C
1		1.8 Vdc	$T_A = +25^{\circ}C$ , or $T_A = +75^{\circ}C$
Ī	V <sub>th</sub> "0"	1.1 Vdc	$T_A = 0^{\circ}C$ , or $T_A = +25^{\circ}C$
		0.9 Vdc	T <sub>A</sub> = +75 <sup>o</sup> C
Output			
Output Voltage	VOL	0.4 Vdc max	I <sub>OL</sub> = 16 mAdc, V <sub>CC</sub> = 4.75 Vdc t
		0.4 Vdc max	1 <sub>OL</sub> = 17.6 mAdc, V <sub>CC</sub> = 5.25 Vdc †
	VOH	2.5 Vdc min	I <sub>OH</sub> = -1.6 mAdc, V <sub>CC</sub> = 4.75 Vdc t
Short-Circuit Current	¹sc	-20 to -65 mAdc	V <sub>CC</sub> = 5.0 Vdc, output grounded †

<sup>&</sup>lt;sup>†</sup>These tests are performed according to the logic equations with a true input equal to  $V_{th}$  "1" and a false input equal to  $V_{th}$  "0".

<sup>\*\*</sup>Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.