MC33364

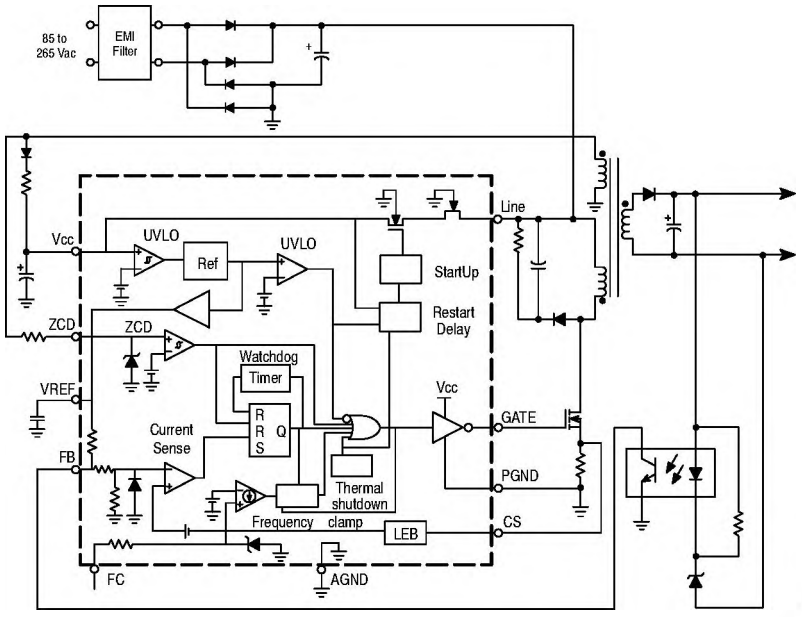
Critical Conduction GreenLine™ SMPS Controller

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Integration of the high voltage startup saves approximately 0.7 W of power compared to the value of the resistor bootstrapped circuits.

Each MC33364 features an on–board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, a CMOS driver and cycle–by–cycle current limiting.

The MC33364D1 has an internal 126 kHz frequency clamp. The MC33364D2 is available without an internal frequency clamp. The MC33364D has an internal 126 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance.

- Lossless Off–Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Operating Temperature Range –25° to +125°C
- Shutdown Capability
- Over Temperature Protection
- Optional/Adjustable Frequency Clamp to Limit EMI



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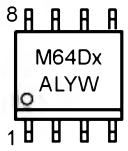
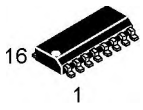
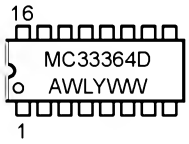
MARKING DIAGRAMS

SO–8
D1, D2 SUFFIX
CASE 751





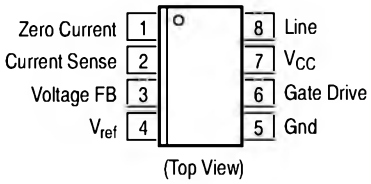
SO–16
D SUFFIX
CASE 751B



x = 1 or 2
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

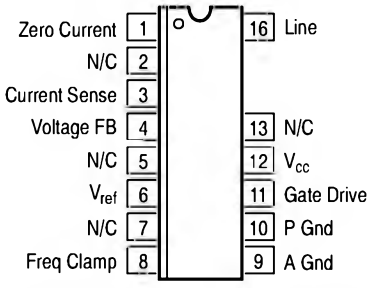
PIN CONNECTIONS

MC33364D1
MC33364D2



(Top View)

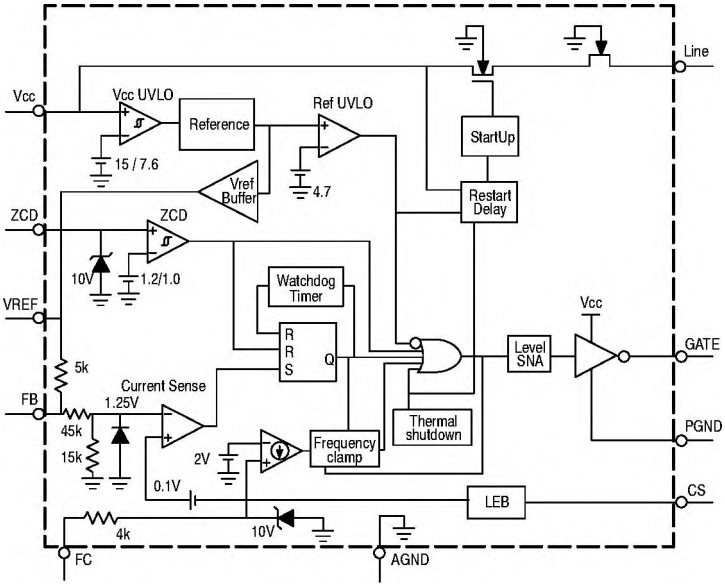
MC33364D



(Top View)

ORDERING INFORMATION

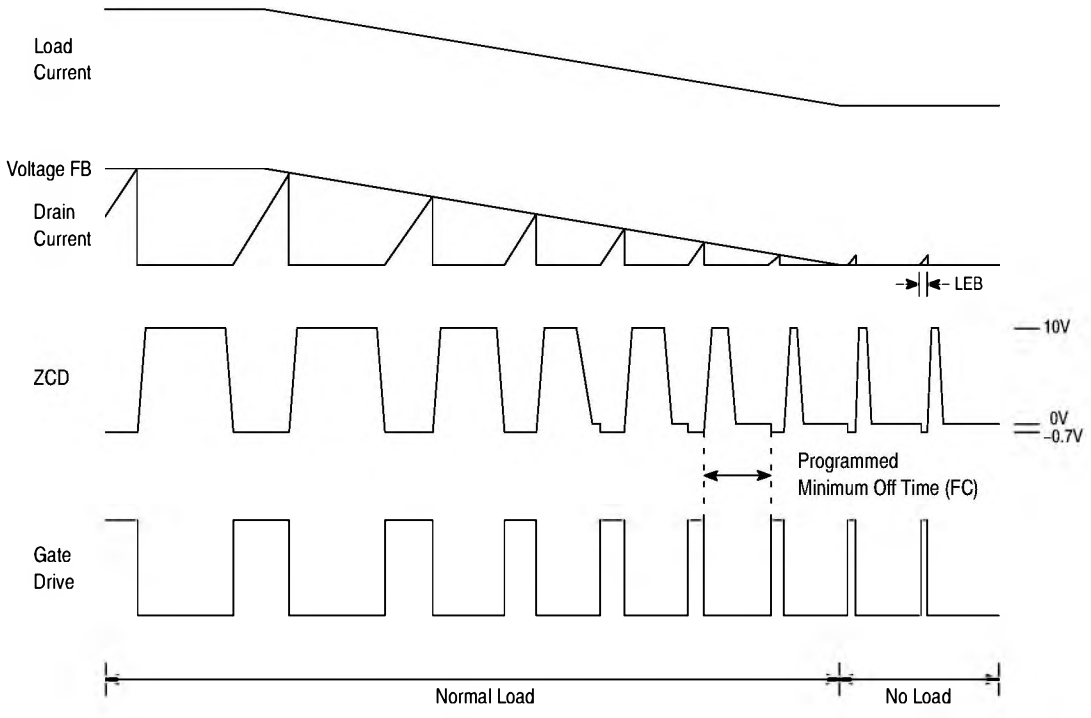
See detailed ordering and shipping information in the package dimensions section on page 1019 of this data sheet.



This device contains 335 active transistors.

Figure 1. Representative Block Diagram

Timing Diagrams



PIN DESCRIPTION

Pin	Function	Description
1 (1)	Zero Current Detect	The ZCD Pin ensures critical conduction mode. ZCD monitors the voltage on the auxiliary winding, during the demagnetization phase of the transformer, comparing it to an internal reference. The ZCD sets the latch for the output driver.
3 (2)	Current Sense	The Current Sense Pin monitors the current in the power switch by measuring the voltage across a resistor. Leading Edge Blanking is utilized to prevent false triggering. The voltage is compared to a resistor divider connected to the Voltage Feedback Pin. A 110 mV voltage off–set is applied to compensate the natural optocoupler saturation voltage.
4 (3)	Voltage Feedback	The Voltage Feedback Pin is typically connected to the collector of the optocoupler for feedback from the isolated secondary output. The Feedback is connected to the V_{ref} Pin via a 5 k resistor providing bias for the external optocoupler.
6 (4)	V_{ref}	The V_{ref} Pin is a buffered internal 5.0 V reference with Undervoltage Lockout.
8 (NA)	Frequency Clamp	The Frequency Clamp Pin ensures a minimum off–time value, typically 6.9 μs. It prevents the MOSFET from restarting within a fixed (33364D1) or adjustable (33364D) delay. The minimum off–time is disabled in the 33364D2. Therefore the maximum switching frequency cannot exceed $1/(T_{ON} + T_{OFFmin})$.
9 (5)	A GND	This pin is the ground for the internal circuitry excluding the gate drive stage.
10 (5)	P GND	This pin is the ground for the gate drive stage.
11 (6)	Gate Drive	The gate drive is the output to drive the gate of the power MOSFET.
12 (7)	V_{CC}	Provides the voltage for all internal circuitry including the gate drive stage and V_{ref}. This pin has Undervoltage Lockout with hysteresis.
16 (8)	Line	The Line Pin provides the initial power to the V_{CC} pins. Internally the line pin is a high voltage current source, eliminating the need for an external startup network.

For further information please refer to the following Application Notes;
AN1594: Critical Conduction Mode, Flyback Switching Power Supply Using the MC33364.
AN1681: How to keep a Flyback Switch–Mode Power Supply Stable with a Critical–Mode Controller.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Operating)	V_{CC}	16	V
Line Voltage	V_{Line}	700	V
Current Sense, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage	V_{in1}	–1.0 to +10	V
Zero Current Detect Input	I_{in}	±5.0	mA
Restart Diode Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics			
D1 and D2 Suffix, Plastic Package Case 751			
Maximum Power Dissipation @ T_A = 70°C	P_D	450	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
D Suffix, Plastic Package Case 751B–05			
Maximum Power Dissipation @ T_A = 70°C	P_D	550	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +125	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_J = –25 to 125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REFERENCE					
Reference Output Voltage (I_{Out} = 0 mA, T_J = 25°C)	V_{ref}	4.90	5.05	5.20	V
Line Regulation (V_{CC} = 10 V to 20 V)	Reg_{line}	–	2.0	50	mV
Load Regulation (I_{Out} = 0 mA to 5.0 mA)	Reg_{load}	–	0.3	50	mV
Maximum V_{ref} Output Current	I_O	–	5	–	mA
Reference Undervoltage Lockout Threshold	V_{th}	–	4.5	–	V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Decreasing)	V_{th}	0.9	1.0	1.1	V
Hysteresis (V_{in} Decreasing)	V_H	–	200	–	mV
Input Clamp Voltage High State (I_{DET} = 3.0 mA) Low State (I_{DET} = –3.0 mA)	 V_{IH} V_{IL}	 9.0 –1.1	 10.33 –0.75	 12 0.5	V
CURRENT SENSE COMPARATOR					
Input Bias Current (V_{CS} = 0 to 2.0 V)	I_{IB}	–0.5	0.02	0.5	μA
Built In Offset	V_{IO}	50	108	170	mV
Feedback Pin Input Range	V_{FB}	1.1	1.24	1.4	V
Feedback Pin to Output Delay	t_{DLY}	100	232	400	ns
DRIVE OUTPUT					
Source Resistance (Drive = 0 V, V_{Gate} = V_{CC} – 1.0 V) Sink Resistance (Drive = V_{CC}, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	10 5	36 11	70 25	Ω Ω
Output Voltage Rise Time (25% – 75%) (C_L = 1.0 nF)	t_r	–	67	150	ns
Output Voltage Fall Time (75% – 25%) (C_L = 1.0 nF)	t_f	–	28	50	ns
Output Voltage in Undervoltage (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UV)}$	–	0.01	0.03	V
LEADING EDGE BLANKING					
Delay to Current Sense Comparator Input (V_{FB} = 2.0 V, V_{CS} = 0 V to 4.0 V step, C_L = 1.0 nF)	$t_{PHL(in/out)}$	–	250		ns
TIMER					
Watchdog Timer	t_{DLY}	200	360	700	μs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	14	15	16	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	6.5	7.6	8.5	V
FREQUENCY CLAMP					
Internal FC Function (pin open)	f_{max}	104	126	145	kHz
Internal FC Function (pin grounded)	f_{max}	400	564	800	kHz
Frequency Clamp Input Threshold	$V_{th(FC)}$	1.89	1.95	2.01	V
Frequency Clamp Control Current Range (Sink)	$I_{Control}$	30	70	110	μA
Dead Time (FC pin = 1.7 V)	T_d	3.5	5.0	6.5	μs
TOTAL DEVICE					
Line Startup Current (V_{Line} = 50 V) (V_{CC} = $V_{th(on)}$ – 1.0 V) Restart Delay Time	I_{Line} t_{DLY}	5.0	8.5 100	12	mA ms
Line Pin Leakage (V_{Line} = 500 V)	I_{Line}	0.5	32	70	μA
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{Line}	6.0	10	12	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF)	I_{CC}	1.5	2.75	4.5	mA
V_{CC} Off State Consumption (V_{CC} = 11 V)	$I_{CC\ Off}$	300	544	800	μA

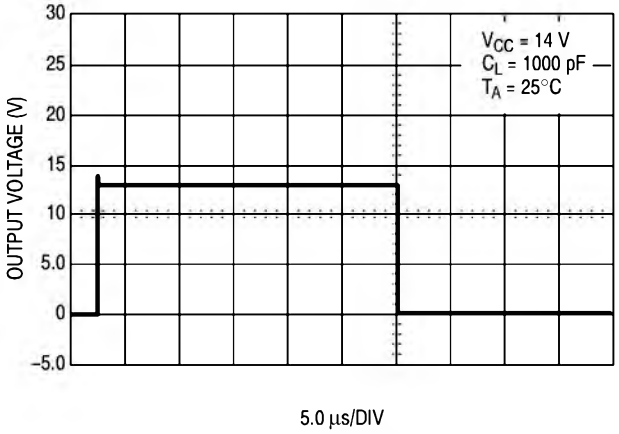


Figure 2. Drive Output Waveform

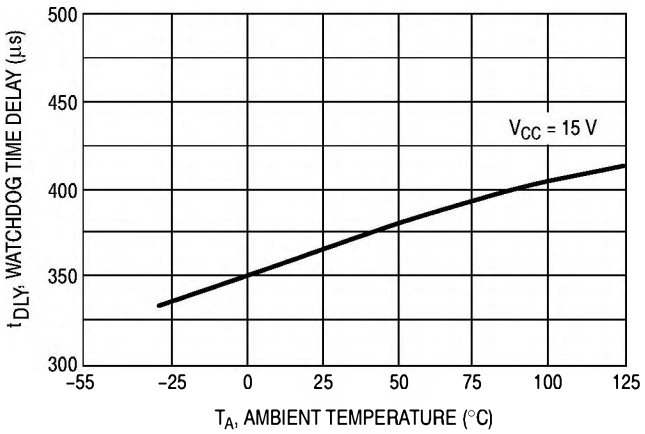


Figure 3. Watchdog Timer Delay versus Temperature

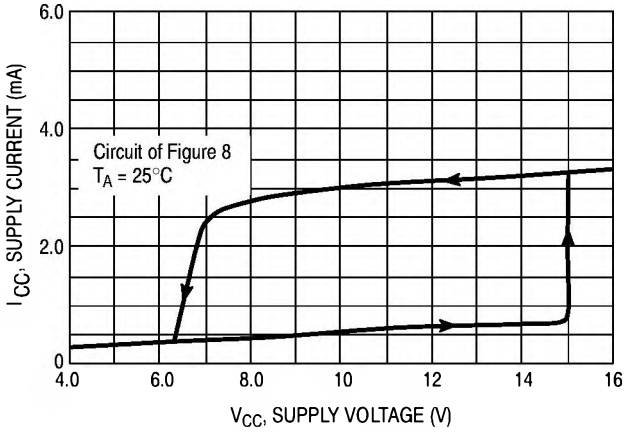


Figure 4. Supply Current versus Supply Voltage

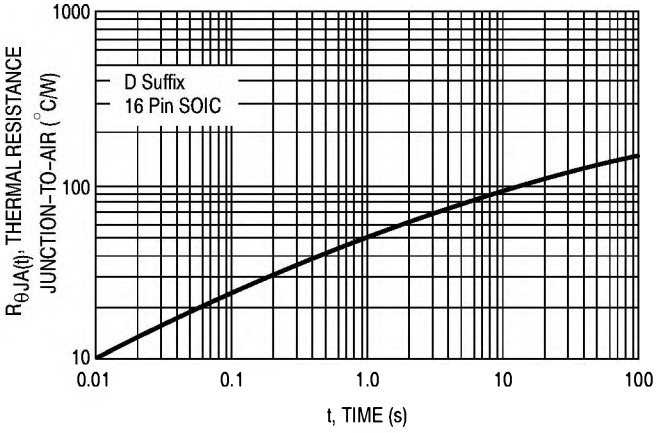


Figure 5. Transient Thermal Resistance

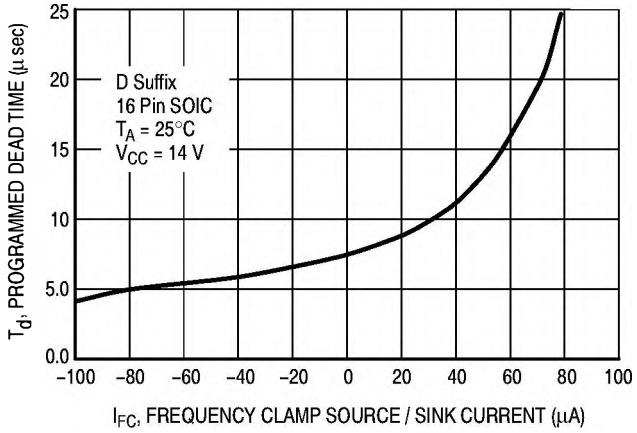


Figure 6. Dead Time versus Frequency Clamp Source / Sink Current

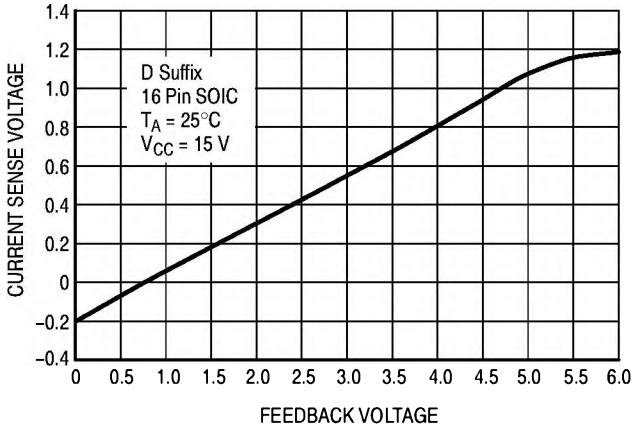
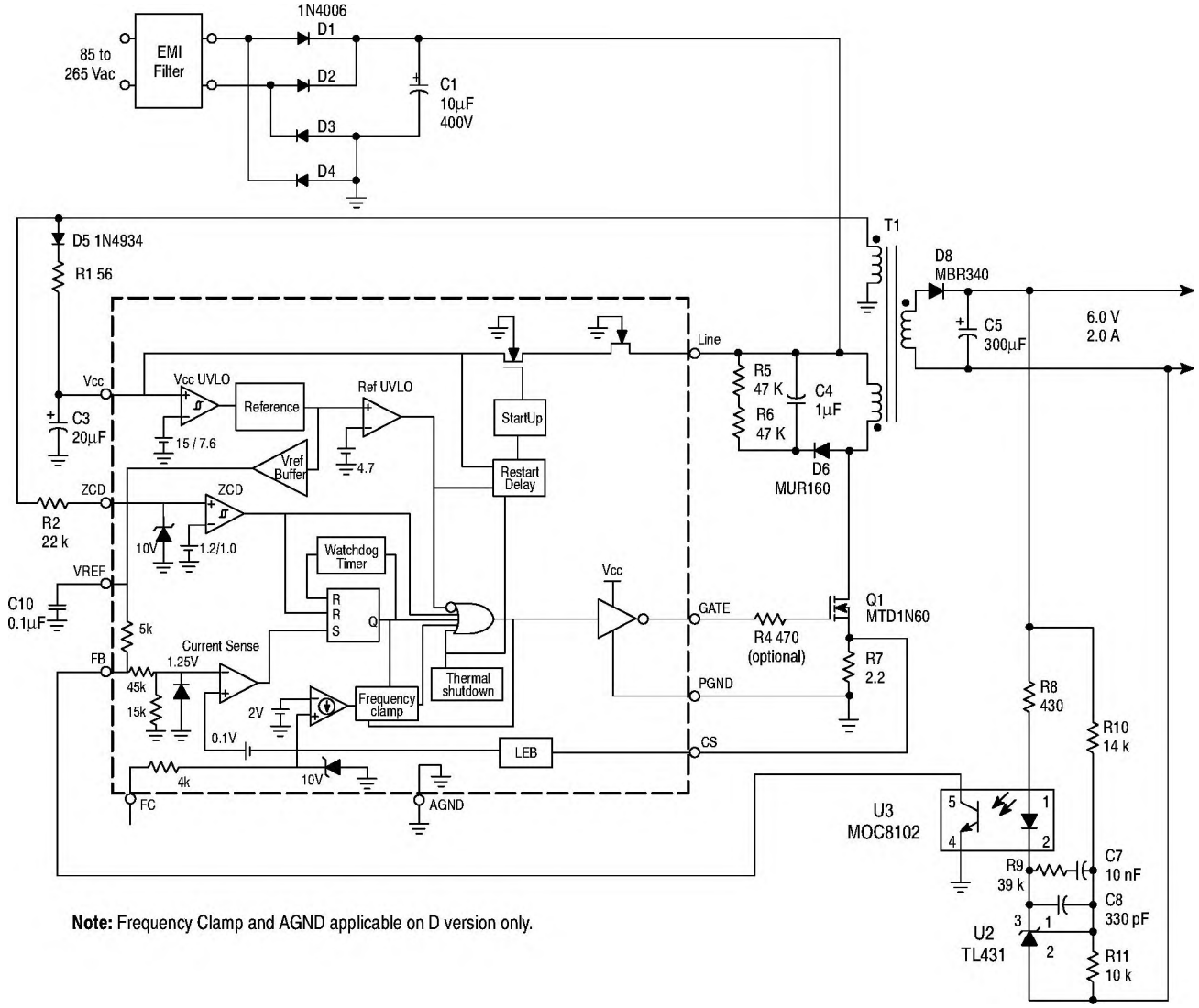


Figure 7. Feedback Voltage versus Current Sense Voltage

FUNCTIONAL DESCRIPTION

INTRODUCTION

With the goal of reducing the size and cost of off–line power supplies, there is an ever increasing demand for an economical method of obtaining a regulated galvanically isolated dc output voltage using a control which operates directly from the ac line. This data sheet describes a monolithic control IC that was specifically designed for power supply control with a minimal number of external components. It offers the designer a simple cost effective solution to obtain the benefits of off–line power regulation.



Note: Frequency Clamp and AGND applicable on D version only.

Figure 8. Functional Block Diagram

Operating Description

The MC33364 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 8, note that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Zero Current Detector

The MC33364 operates as a critical conduction current mode controller, whereby the output switch conduction is initiated by the Zero Current Detector pin and terminated when the peak inductor current reaches the programmed threshold level. The ZCD pin indirectly monitors the inductor current by sensing the auxiliary winding voltage. When the voltage falls below the set threshold, 1.0 volt, the comparator resets the latch to turn on the MOSFET. There is 200 mV of hysteresis built into the comparator for noise immunity and to prevent false tripping

The ZCD pin is internally protected by a 10 volt and –0.7 volt clamp. An external resistor is necessary to limit the input current to 2 mA to protect the clamp.

Since the MC33364 implements the ZCD pin, the SMPS circuit has the following benefits:

1. A less expensive rectifier can be used on the output windings because of the zero current switching which naturally softens the diode turn–off.
2. The second benefit is the peak drain current which is limited to twice the average input current. By combining the ZCD series resistor with the pin capacitance, a drain–source valley switching can be implemented, further reducing the turn–on losses and the EMI disturbances.
3. By preventing the SMPS from entering the Continuous Conduction Mode (CCM), the MC33364 forces the system to stay a first–order device (in the lower frequency range) in any operating condition (output short, start–up, low mains). The feedback compensation network is thus considerably simplified.

Current Sense and Feedback Inputs

The Current Sense pin and the Feedback pin are linked internally in the device via the current sense comparator. The output of the comparator is connected to the Set of the RS Latch, which turns the external MOSFET off.

The current sense operates by using a resistor, connected between the source of the MOSFET and ground, to convert the current through the inductor to a voltage. Leading Edge Blanking is implemented to prevent false triggering due to parasitics. The current sense voltage is level shifted up by 0.1 volt into the non–inverting input of the comparator. This offset accounts for the optocoupler VCEsat and allows the duty–cycle to be zero.

The maximum peak switch current is 1.15V (the maximum voltage at the inverting input, 1.25 volts, minus 0.1 volt, the level shift) divided by the external current sense resistance. The Current Sense Input to Drive Output propagation delay is 232 nsec typically.

The Feedback pin is internally pulled up with a 5 kOhm resistor from the 5.0 volt Vref pin. The Feedback pin uses a resistor divider to proportionally adjust the voltage into the inverting input of the comparator. The inverting input also has a 1.25 volt clamp. Typically the Feedback pin is connected to the collector of the optocoupler.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 410 microseconds after the inductor current reaches zero. This time–out thus ensures the IC will restart when the demagnetization signal is lower than the internal ZCD 1V threshold or has simply been lost.

Undervoltage Lockout

The MC33364 has a hysteretic UVLO associated with the V_{CC} pin. During startup, V_{CC} must rise to 15 volts to turn off the startup circuit associated with the Line pin and to enable the output drivers. The voltage at V_{CC} must remain above 7.6 volts for the part to remain operational.

Internal Reference

The MC33364 has an internal buffered 5.0 volt reference. The reference requires a 0.1 μF bypass capacitor for noise immunity. The reference is capable of sourcing 10 mA typically. The reference contains an independant UVLO which will disable the output drive circuitry.

Startup Circuit and Restart Delay

A high voltage Startup Circuit is contained within the MC33364 eliminating the need for external components. The internal startup circuit operates as a constant current source to charge up the bypass capacitor on the V_{CC} pin. The Startup Circuitry is controlled by the Restart Delay circuitry. The threshold levels of the turn on and turn off are below 4.5 volts and above 15 volts, respectively, as measured on the V_{CC} pin.

A restart delay function is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. During a short circuit, the restart delay prevents excessive power dissipation in the primary side of the SMPS and allows time for the output to reset the fault condition. The restart delay time is approximately 100 msec.

Output Switching Frequency Clamp

In normal operation, the MC33364 operates the flyback transformer in the critical conduction mode. The CCM is defined by the transformer ramping to a peak current value, ramping down to zero, then immediately ramping positive again. The peak current is programmed by the current sense resistor and is compared with a divided down voltage from

the feedback pin. When the output is reduced from full load to standby or no load, the switching frequency can increase dramatically to hundreds of kilohertz. Due to EMI regulations above 150 kHz, the Frequency Clamp on the MC33364D and MC33364D1 will limit the upper frequency by inserting a minimum off time.

The frequency of a switching regulator is determined by $f = 1/(T_{on} + T_{off})$. During light load and no load conditions, T_{off} is the reset time of the transformer plus dead time. At no load conditions, T_{on} is approximately the LEB and T_{off} is the programmed minimum off–time. With the addition of logic delay times, the maximum frequency when the FC pin floats is 126 kHz nominally.

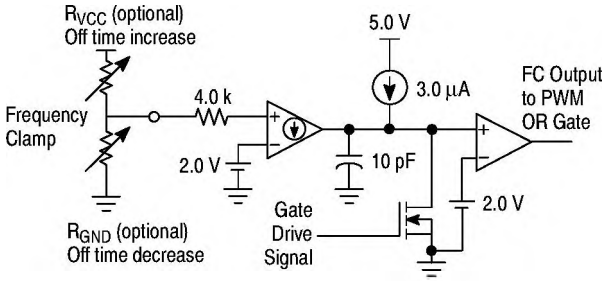
The Frequency Clamp inserts a minimum off–time immediately after the driving signal goes low. If the ZCD signal comes within this minimum off–time, the information is ignored until the minimum off–time expires. By forcing the minimum off–time, the transformer will operate in the Discontinuous Mode. The next coming ZCD signal starts the latch. The MC33364 is available in three versions:

MC33364D1: the internal minimum off–time is fixed at 6.9μsec typically

MC33364D2: there is no internal minimum off–time

MC33364D: the internal minimum off–time can be either lengthened, shortened or eliminated by biasing the appropriate pin

The FC pin contains a 4.0 kOhm series resistor into the non–inverting input of a comparator. The non–inverting input has a 10 volt clamp to limit overvoltage. Refer to Figure 9 for a detailed circuit of the Frequency Clamp.



NOTE: For proper operation, use either R_{Vcc} or R_{gnd} or let the pin float.

Figure 9. Simplified Frequency Clamp Circuit

The MC33364D has a Frequency Clamp pin which can vary the maximum frequency. If the FC pin floats, the minimum off–time is fixed at 6.9 μsec typically. If the FC pin is grounded, the clamp is disabled. Sinking or sourcing a current up to 100 μA into the FC pin will vary the maximum frequency (see Figure 6). However, we do not recommend exceeding 80μA because the high dDT/dIFC would not ensure a stable operation.

Output

The IC contains a CMOS output driver specifically designed for direct drive of power MOSFETs. The Drive Output typical rise and fall time is 50 nS with a 1.0 nF load. Unbalanced Source and Sink capability eliminates the need for an external resistor between the IC Drive output and the Gate of the external MOSFET. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the UVLO is active. This characteristic eliminates the need for an external gate pull–down resistor.

APPLICATION INFORMATION

Design Example

Design an off–line Flyback converter according to the following requirements:

Output Power: 12 W
Output: 6.0 V @ 2 Amperes
Input voltage range: 90 Vac – 270 Vac, 50/60 Hz

The operation for the circuit shown in Figure 8 is as follows: the rectifier bridge D1–D4 and the capacitor C1 convert the ac line voltage to dc. This voltage supplies the primary winding of the transformer T1 and the startup circuit in U1 through the line pin. The primary current loop is closed by the transformer's primary winding, the TMOS switch Q1 and the current sense resistor R7. The resistors R5, R6, diode D6 and capacitor C4 create a snubber clamping network that protects Q1 from spikes on the primary winding. The network consisting of capacitor C3, diode D5 and resistor R1 provides a V_{CC} supply voltage for U1 from the auxiliary winding of the transformer. The resistor R1 makes V_{CC} more stable and resistant to noise. The resistor R2 reduces the current flow through the internal clamping and protection zener diode of the Zero Crossing Detector (ZCD) within U1. C3 is the decoupling capacitor of the supply voltage. The resistor R3 can provide additional bias current for the optoisolator's transistor. The diode D8 and the capacitor C5 rectify and filter the output voltage. The TL431, a programmable voltage reference, drives the primary side of the optoisolator to provide isolated feedback to the MC33364. The resistor divider consisting of R10 and R11 program the voltage of the TL431. The resistor R9 and the capacitors C7 and C8 provide frequency compensation of the feedback loop. Resistor R8 provides a current limit for the opto coupler and the TL431.

Since the critical conduction mode converter is a variable frequency system, the MC33364 has a built–in special block to reduce switching frequency in the no load condition. This block is named the "frequency clamp" block. MC33364 used in the design example has an internal frequency clamp set to 126 kHz. However, optional versions with a disabled or variable frequency clamp are available. The frequency clamp works as follows: the clamp controls the part of the switching cycle when the MOSFET switch is turned off. If this "off–time" (determined by the reset time of the transformer's core) is too short, then the frequency clamp does not allow the switch to turn–on again until the defined frequency clamp time is reached (i.e., the frequency clamp will insert a dead time).

There are several advantages of the MC33364's startup circuit. The startup circuit includes a special high voltage switch that controls the path between the rectified line voltage and the V_{CC} supply capacitor to charge that capacitor by a limited current when the power is applied to the input. After a few switching cycles the IC is supplied from the transformer's auxiliary winding. After V_{CC} reaches the undervoltage lockout threshold value, the startup switch is turned off by the undervoltage and the overvoltage control circuit. Because the power supply can be shorted on the output, causing the auxiliary voltage to be zero, the MC33364 will periodically start its startup block. This mode is named "hiccup mode". During this mode the temperature of the chip rises but remains protected by the thermal shutdown block. During the power supply's normal operation, the high voltage internal MOSFET is turned off, preventing wasted power, and thereby, allowing greater circuit efficiency.

Since a bridge rectifier is used, the resulting minimum and maximum dc input voltages can be calculated:

$$V_{in(min)}dc = \sqrt{2}xV_{in(min)}ac = (\sqrt{2})(90\ Vac) = 127\ V$$

$$V_{in(\mu ax)}dc = \sqrt{2}xV_{in(\mu ax)}ac = (\sqrt{2})(270\ Vac) = 382\ V$$

The maximum average input current is:

$$I_{in} = \frac{P_{out}}{nV_{in(min)}} = \frac{12\ W}{0.8(127\ V)} = 0.118\ A$$

where n = estimated circuit efficiency.

A TMOS switch with 600 V avalanche breakdown voltage is used. The voltage on the switch's drain consists of the input voltage and the flyback voltage of the transformer's primary winding. There is a ringing on the rising edge's top of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by the RCD network. Design this clamped wave for an amplitude of 50 V below the avalanche breakdown of the TMOS device. Add another 50 V to allow a safety margin for the MOSFET. Then a suitable value of the flyback voltage may be calculated:

$$V_{flbk} = V_{TMOS} - V_{in(max)} - 100\ V =$$
$$600\ V - 382\ V - 100\ V = 118\ V$$

Since this value is very close to the $V_{in(min)}$, set:

$$V_{flbk} = V_{in(min)} = 127\ V$$

The V_{flbk} value of the duty cycle is given by:

$$\partial max = \frac{V_{flbk}}{V_{flbk} + V_{in(min)}} = \frac{127\ V}{[127\ V + 127\ V]} = 0.5$$

The maximum input primary peak current:

$$I_{ppk} = \frac{2\ I_{in}}{\partial max} = \frac{2.0(0.118\ A)}{0.5} = 0.472\ A$$

Choose the desired minimum frequency f_{min} of operation to be 70 kHz.

After reviewing the core sizing information provided by a core manufacturer, a EE core of size about 20 mm was chosen. Siemens' N67 magnetic material is used, which corresponds to a Philips 3C85 or TDK PC40 material.

The primary inductance value is given by:

$$L_p = \frac{\partial max\ V_{in(min)}}{(i_{ppk})(f_{min})} = \frac{0.5(127\ V)}{(0.472\ A)(70\ kHz)} = 1.92\ mH$$

The manufacturer recommends for that magnetic core a maximum operating flux density of:

$$B_{max} = 0.2\ T$$

The cross–sectional area A_c of the EF20 core is:

$$A_c = 33.5\ mm^2$$

The operating flux density is given by:

$$B_{max} = \frac{L_p I_{ppk}}{N_p A_c}$$

From this equation the number of turns of the primary winding can be derived:

$$n_p = \frac{L_p I_{ppk}}{B_{max} A_c}$$

The A_L factor is determined by:

$$A_L = \frac{L_p}{n^2_p} = \frac{L_p(B_{max}A_c)^2}{\left[L_p\left(I_{ppk}\right)^2\right]} = \frac{(0.2\ T)(33.5\ E{-}6\ m^2)^2}{(.00192\ H)(0.472\ A)^2} = 105\ nH$$

From the manufacturer's catalogue recommendation the core with an A_L of 100 nH is selected. The desired number of turns of the primary winding is:

$$n_p = \left(\frac{L_p}{A_L}\right)^{1/2} = \left[\frac{(0.00192\ H)}{(100\ nH)}\right]^{1/2} = 139\ turns$$

The number of turns needed by the 6.0 V secondary is (assuming a Schottky rectifier is used):

$$n_s = \frac{(V_s + V_{fwd})(1{-}\partial max)n_p}{\left[\partial max\left(V_{in(min)}\right)\right]} = \frac{(6.0\ V + 0.3\ V)(1 - 0.5)139}{[0.5(127\ V)]} = 7\ turns$$

The auxiliary winding to power the control IC is 16 V and its number of turns is given by:

$$naux = \frac{(V_{aux} + V_{fwd})(1 - \partial max)n_p}{\left[\partial max(V_{in(min)})\right]} = \frac{(16\ V + 0.9\ V)(1 - 0.5)139}{[0.5(127\ V)]} = 19\ turns$$

The approximate value of rectifier capacitance needed is:

$$C1 = \frac{t_{off}(I_{in})}{V_{ripple}} = \frac{(5\ m\ sec)(0.118\ A)}{50\ V} = 11.8\ \mu F$$

where the minimum ripple frequency is 2 times the 50 Hz line frequency and t_{off}, the discharge time of C1 during the haversine cycle, is assumed to be half the cycle period.

Because we have a variable frequency system, all the calculations for the value of the output filter capacitors will be done at the lowest frequency, since the ripple voltage will be greatest at this frequency. When selecting the output capacitor select a capacitor with low ESR to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C5 = \frac{I_{out}}{(f_{min})(V_{rip})} = \frac{2\ A}{(70\ kHz)(0.1\ V)} = 286\ \mu F$$

Determining the value of the current sense resistor (R7), one uses the peak current in the predesign consideration. Since within the IC there is a limitation of the voltage for the current sensing, which is set to 1.2 V, the design of the current sense resistor is simply given by:

$$R7 = \frac{V_{cs}}{I_{ppk}} = \frac{1.2\ V}{0.472\ A} = 2.54\ \Omega \approx 2.2\ \Omega$$

The error amplifier function is provided by a TL431 on the secondary, connected to the primary side via an optoisolator, the MOC8102.

The voltage of the optoisolator collector node sets the peak current flowing through the power switch during each cycle. This pin will be connected to the feedback pin of the MC33364, which will directly set the peak current.

Starting on the secondary side of the power supply, assign the sense current through the voltage–sensing resistor divider to be approximately 0.25 mA. One can immediately calculate the value of the lower and upper resistor:

$$R_{lower} = R11 = \frac{V_{ref}(TL431)}{I_{div}} = \frac{2.5\ V}{0.25\ mA} = 10\ k$$

$$R_{upper} = R10 = \frac{V_{out} - V_{ref}(TL431)}{I_{div}} = \frac{6.0\ V - 2.5V}{0.25\ mA} = 14\ k$$

The value of the resistor that would provide the bias current through the optoisolator and the TL431 is set by the minimum operating current requirements of the TL431. This current is minimum 1.0 mA. Assign the maximum current through the branch to be 5 mA. That makes the bias resistor value equal to:

$$R_{bias} = R_S = \frac{V_{out} - [V_{ref}(TL431) + V_{LED}]}{I_{LED}}$$

$$= \frac{6.0\ V - [2.5V + 1.4V]}{5.0\ mA} = 420\ \Omega \approx 430\ \Omega$$

The MOC8102 has a typical current transfer ratio (CTR) of 100% with 25% tolerance. When the TL431 is full–on, 5 mA will be drawn from the transistor within the MOC8102. The transistor should be in saturated state at that time, so its collector resistor must be

$$R_{collector} = \frac{V_{ref} - V_{sat}}{I_{LED}} = \frac{5.0\ V - 0.3\ V}{5.0\ mA} = 940\ \Omega$$

Since a resistor of 5.0 k is internally connected from the reference voltage to the feedback pin of the MC33364, the external resistor can have a higher value

$$R_{ext} = R3 = \frac{(R_{int})(R_{collector})}{(R_{int}) - (R_{collector})} = \frac{(5.0\ k)(940)}{5.0\ k - 940}$$

$$= 1157\ \Omega \approx 1200\ \Omega$$

This completes the design of the voltage feedback circuit.

In no load condition there is only a current flowing through the optoisolator diode and the voltage sense divider on the secondary side.

The load at that condition is given by:

$$R_{noload} = \frac{V_{out}}{(I_{LED} + I_{div})}$$

$$= \frac{6.0\ V}{(5.0\ mA + 0.25\ mA)} = 1143\ \Omega$$

The output filter pole at no load is:

$$f_{pn} = \frac{1}{(2\pi\ R_{noload}\ C_{out})}$$

$$= \frac{1}{(2\pi)(1143)(300\ \mu F)} = 0.46\ Hz$$

In heavy load condition the I_{LED} and I_{div} is negligible. The heavy load resistance is given by:

$$R_{heavy} = \frac{V_{out}}{I_{out}} = \frac{6.0\ V}{2.0\ A} = 3.0\ \Omega$$

The output filter pole at heavy load of this output is

$$f_{pn} = \frac{1}{(2\pi\ R_{heavy} C_{out})} = \frac{1}{(2\pi)(3)(300\ \mu F)} = 177\ Hz$$

The gain exhibited by the open loop power supply at the high input voltage will be:

$$A = \frac{\left(V_{in\ max} - V_{out}\right)^2 Ns}{\left((V_{in\ max})(V_{error})(Np)\right)} = \frac{(382\ V - 6.0\ V)^2(7)}{(382\ V)(1.2\ V)(139)}$$

$$= 15.53 = 23.82\ dB$$

The maximum recommended bandwidth is approximately:

$$f_c = \frac{fs\ min}{5} = \frac{70\ kHz}{5} = 14\ kHz$$

The gain needed by the error amplifier to achieve this bandwidth is calculated at the rated load because that yields the bandwidth condition, which is:

$$Gc = 20\ log\left(\frac{f_c}{f_{ph}}\right) - A = 20\ log\left(\frac{14\ kHz}{177}\right) - 23.82\ dB$$

$$= 14.14\ dB$$

The gain in absolute terms is:

$$A_c = 10^{(Gc/20)} = 10^{(14.14/20)} = 51$$

Now the compensation circuit elements can be calculated. The output resistance of the voltage sense divider is given by the parallel combination of resistors in the divider:

$$R_{in} = R_{upper} \,||\, R_{lower} = 10\ k \,||\, 14\ k = 5833\ \Omega$$

$$R9 = (Ac)\ (R_{in}) = 29.75\ k \approx 30\ k$$

$$C8 = \frac{1}{\left[2\pi\ (A_c)\ (R_{in})\ (f_c)\right]} = 382\ pF \approx 390\ pF$$

The compensation zero must be placed at or below the light load filter pole:

$$C7 = \frac{1}{\left[2\pi\ (R9)\ (f_{pn})\right]} = 11.63\ \mu F \approx 10\ \mu F$$

The described critical conduction mode flyback converter has the following performance and maximum ratings:

Output power	12W
Output	12V @ 1Amp max
Input voltage range	90VAC – 270VAC

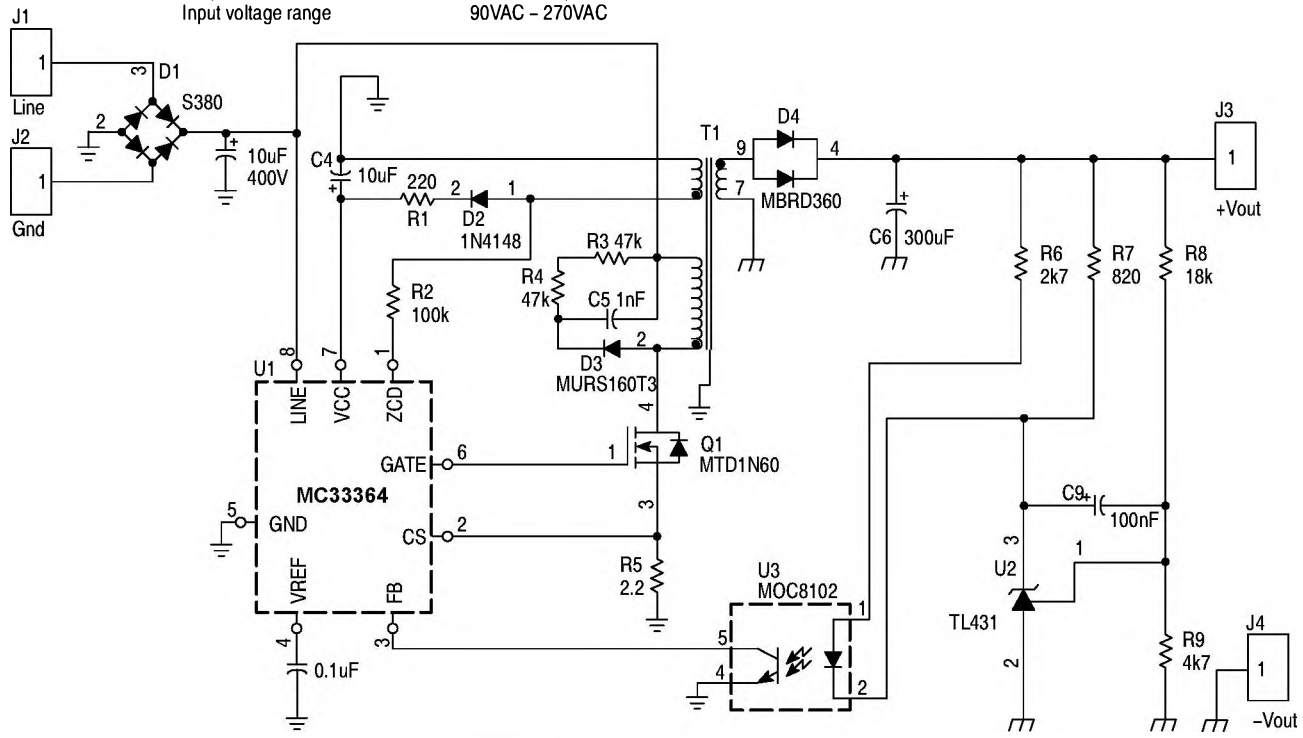


Figure 10. Critical Conduction Mode Flyback Converter

CONVERTER TEST DATA

Test	Conditions	Results
Line Regulation	V_{in} = 120VAC to 240VAC, I_{out} = 0.8A	ΔV = 50mV
Load	V_{in} = 120VAC, I_{out} = 0.2A to 0.8A	ΔV = 40mV
	V_{in} = 240VAC, I_{out} = 0.2A to 0.8A	ΔV = 40mV
Output Ripple	V_{in} = 120VAC, I_{out} = 0.8A	ΔV = 290mV
	V_{in} = 240VAC, I_{out} = 0.8A	ΔV = 24mV
Efficiency	V_{in} = 120VAC, I_{out} = 0.8A	η = 78.0%
	V_{in} = 240VAC, I_{out} = 0.8A	η = 79.4%
Power Factor	V_{in} = 120VAC, I_{out} = 0.8A	Pf = 0.491
	V_{in} = 240VAC, I_{out} = 0.8A	Pf = 0.505

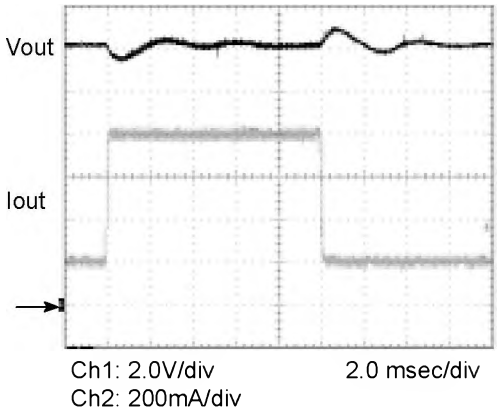


Figure 11. Load Regulation 120V

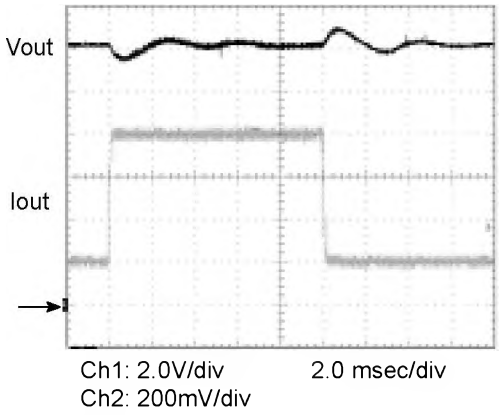


Figure 12. Load Regulation 240V

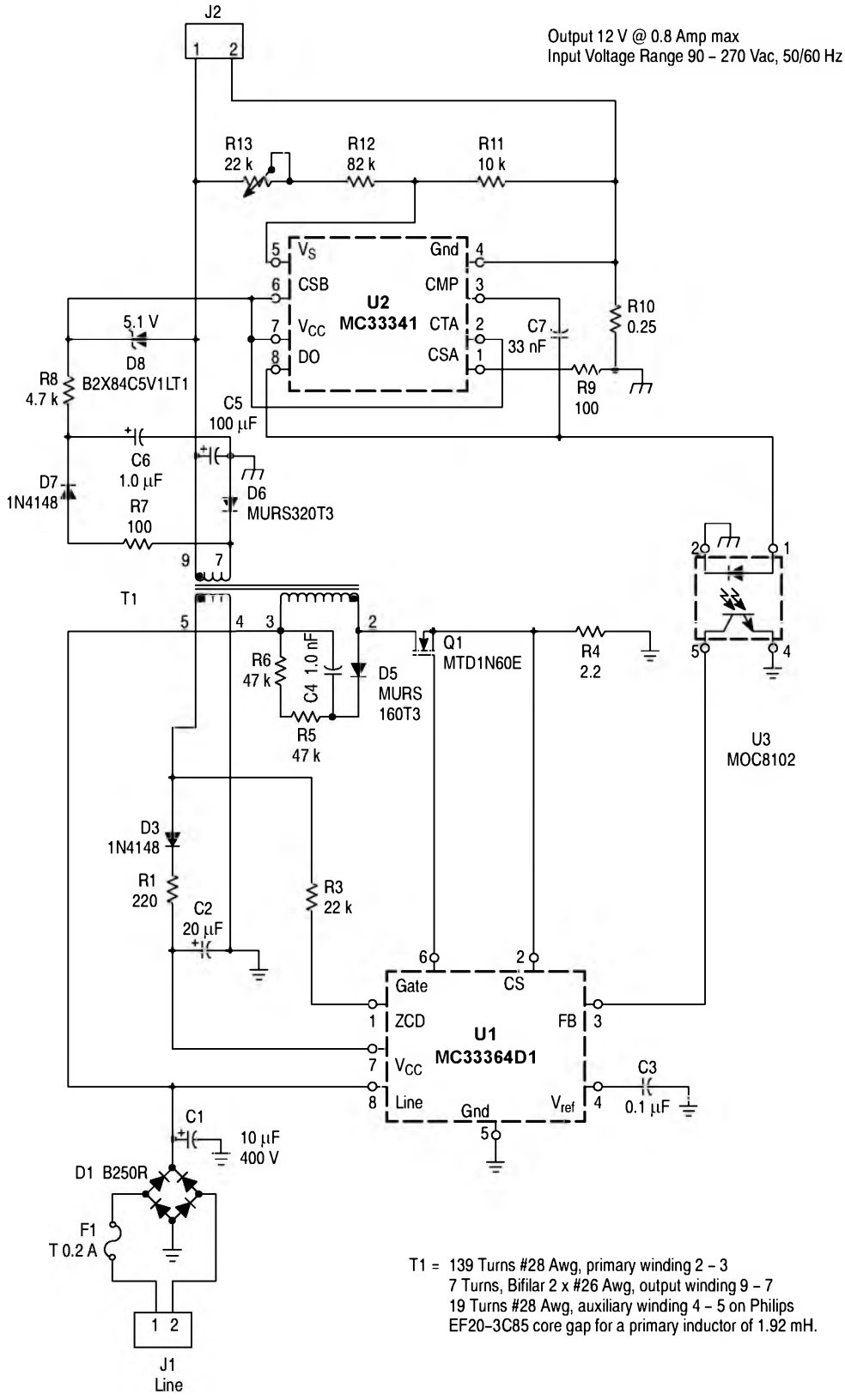


Figure 13. Universal Input Battery Charger

ORDERING INFORMATION

Device	Package	Shipping
MC33364D1	SO–8	98 Units / Rail
MC33364D1R2	SO–8 Tape & Reel	2500 Units / Tape & Reel
MC33364D2	SO–8	98 Units / Rail
MC33364D2R2	SO–8 Tape & Reel	2500 Units / Tape & Reel
MC33364D	SO–16	48 Units / Rail
MC33364DR2	SO–16 Tape & Reel	2500 Units / Tape & Reel