

Advance Information

Dual High-Side Switch

The 33289 is a dual high-side switch (DHSS) dedicated for use in automotive and industrial applications. It is designed to drive typical inductive loads such as solenoid valves.

This device consists of two independent 40 mΩ R_{DS(ON)} MOSFET channels plus corresponding control circuitry in a surface mount package. The 33289 can be interfaced directly to a microcontroller for input control and monitoring of diagnostic output.

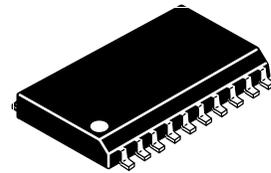
Each switch offers independent protection and diagnosis during short circuit, overvoltage, and undervoltage conditions, as well as an over-temperature shutdown feature. A logic low on the Open Load Detect Enable pin (OLDE) minimizes bias current drain by disabling the open load circuitry current source. The device also has a very low quiescent current in Standby mode.

Features

- Designed to Drive Inductive Loads
- Operating Voltage Range from 6.0 V to 27 V
- Maximum Breakdown Voltage Greater Than 40 V
- Surface Mount Package
- 40 mΩ R_{DS(ON)} at 25°C
- Overtemperature Protection with Hysteresis
- Short Circuit Protection
- Undervoltage Shutdown
- Overvoltage Shutdown
- Open Load Detection in Off-State
- Independent Diagnostic Output
- ESD Protection 2.0 kV with Standby Current > 5.0 μA at V_{BAT} Below 14 V

33289

DUAL HIGH-SIDE SWITCH

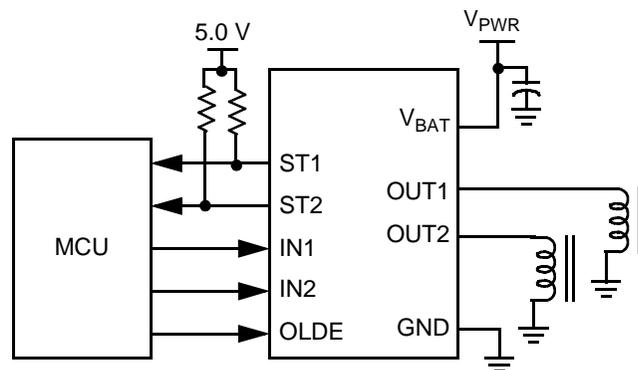


**DW SUFFIX
CASE 751D
20-LEAD SOICW**

ORDERING INFORMATION

Device	Temperature Range (T _A)	Package
MC33289DW/R2	-40 to 125°C	20 SOICW

33289 Simplified Application Diagram



This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

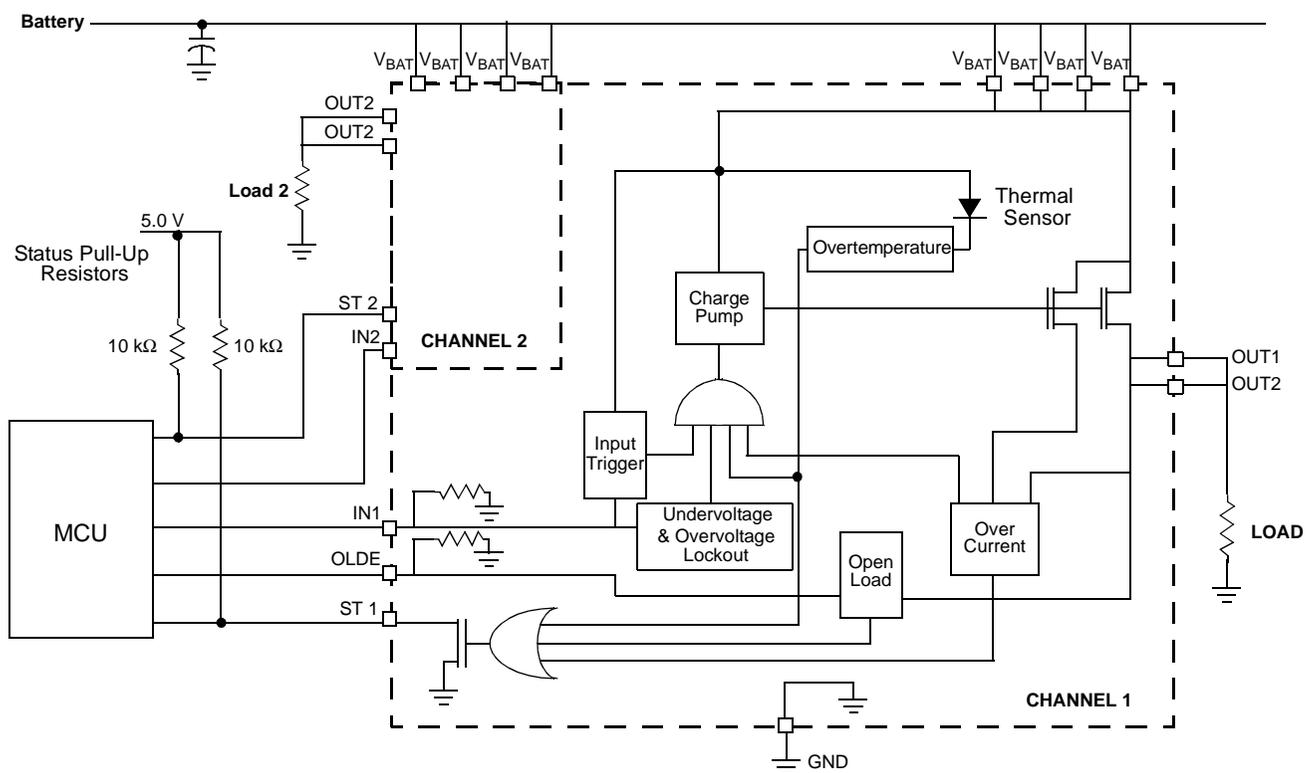
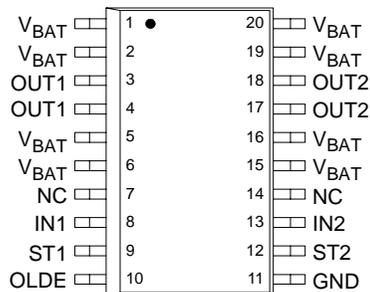


Figure 1. 33289 Simplified Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1, 2 5, 6 15, 16 19, 20	V _{BAT}	Voltage Supply (Battery)	These are the power supply pins of the device. These pins are directly connected with the lead frame of the package and are tied to the drain of the switching MOSFET. These pins can be directly connected to the battery voltage. In addition to their supply function, these pins participate to the thermal behavior of the device in conducting the heat from the switching MOSFET to the printed circuit board.
3, 4	OUT1	Output Channel 1	These pins are the output one terminals. They connect directly to the source of the power MOSFET. These pins are used by the control circuitry to sense the device output voltage. The R _{DS(ON)} is 40 mΩ maximum per output at 25°C and will increase to a maximum of 75 mΩ at 150°C junction temperature.
7, 14	NC	No Connect	These pins do not connect.
8	IN1	Input Channel 1	These are the device input pins. They control their associated outputs. The levels are CMOS compatible. When the input is a logic low, the associated output MOSFET is in the OFF state. When input is high, the MOSFET is turned ON and the load is activated. When both inputs are low, the device is in Standby mode and its supply current is reduced. Each input pin has an internal active pull-down, so it will not float if disconnected.
9	ST1	Status Channel 1	These pins are the channel one fault detection flags. Their internal structure is an open drain architecture with an internal clamp at 6.0 V. An external pull-up resistor connected to VDD (5.0 V) is required. This is an active low output. If the device is in its normal condition the status lines will be high. If open load or other fault occurs, the associated channel status flag will be pulled low. Please see Functional Truth Table.
10	OLDE	Open Load Detection Enable	This pin is a digital input, enabling the open load current diagnostic circuitry. When OLDE is a logic low, the open load circuitry is not powered and the bias current draw of the device is at a minimum. If OLDE is a logic high, the open load circuitry is functional at the price of a higher bias current draw. OLDE pin has a pull down resistor.
11	GND	Ground	Ground of the integrated circuit.
12	ST2	Status Channel 2	These pins are the channel two fault detection flags. Their internal structure is an open drain architecture with an internal clamp at 6V. An external pull up resistor connected to Vdd (5.0 V) is needed. This is an active low output. If the device is in its normal condition the status lines will be high. If open load or other fault occurs, the associated channel status flag will be pulled low. Please, see Functional Truth Table, Table 1.
13	IN2	Input Channel 2	These are the device input pins. They control their associated outputs. The levels are CMOS compatible. When the input is a logic low, the associated output MOSFET is in the OFF state. When input is high, the MOSFET is turned ON and the load is activated. When both inputs are low, the device is in Standby mode and its supply current is reduced. Each input pin has an internal active pull down, so it will not float if disconnected.
17, 18	OUT2	Output Channel 2	These pins are the output two terminals. They are connected to the source of the power MOSFET. These pins are used by the control circuitry to sense the device output voltage. The R _{DS(ON)} is 40 mΩ maximum per output at 25°C and will increase to a maximum of 75 mΩ at 150°C junction temperature.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
V_{BAT} and V_{BATC} Voltage, Continuous/Pulse	V_{BAT}	-0.3 to 41	V
OUT1, OUT2 Voltage with Respect to GND, Continuous/Pulse	V_{OUT}	-4.0 to 41	V
OUT1, OUT2 to V_{BTAP} Voltage, Continuous	V_{OUT}	41	V
ST1, ST2 Voltage, Continuous/Pulse	V_{ST}	-0.3 to 7.0	V
IN1, IN2 Voltage, Continuous	V_{IN}	-0.3 to 7.0	V
IN1, IN2, ST1, ST2, OLDE Current	I_{IN}	± 4.0	mA
ESD Voltage Human Body Model (Note 1) Machine Model (Note 2)	V_{ESD1} V_{ESD2}	± 2000 ± 200	V
Operating Junction Temperature	T_J	-40 to 150	$^{\circ}\text{C}$
Storage Temperature	T_{ST}	-55 to 150	$^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient (Note 3)	$R_{\theta JA}$	70	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-to-Lead, Both Channels ON	$R_{\theta J1}$	15	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-to-Lead, One Channel ON	$R_{\theta J2}$	15	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-to-Lead, Logic Die	$R_{\theta J3}$	30	$^{\circ}\text{C}/\text{W}$
Lead Soldering Temperature (Note 4)	T_{SOLDER}	260	$^{\circ}\text{C}$

Notes

- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}=100$ pF, $R_{ZAP}=1500$ Ω).
- ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}=200$ pF, $R_{ZAP}=0$ Ω).
- With minimum PCB dimensions
- Lead soldering temperature limit is for 10 seconds maximum duration; not designed for immersion soldering; exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_J from $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, $6.0\text{ V} \leq V_{\text{BAT}} \leq 24\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^{\circ}\text{C}$ under nominal V_{BAT} conditions at time to device characterization.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Operating Voltage	V_{BAT}	6.0	—	V_{OV}	V
Supply Current, Both Channels ON $V_{\text{BAT}} = 13.5\text{ V}$; OLDE High	I_{BAT1}	—	6.0	16	mA
Supply Current, One Channel ON $V_{\text{BAT}} = 13.5\text{ V}$; OLDE High	I_{BAT2}	—	5.0	10	mA
Supply Current, Both Channels OFF $V_{\text{BAT}} = 12.6\text{ V}$; OLDE Low, $T_J < 125^{\circ}\text{C}$	I_{BAT3}	—	—	5.0	μA
Supply Current, Any State $V_{\text{BAT}} = 13.5\text{ V}$	$I_{\text{BAT-MAX}}$	—	—	30	mA
Output OFF State Leakage Current per Channel $V_{\text{BAT}} = 13.5\text{ V}$; IN1, IN2, OLDE Low, Both Output Grounded $T_J < 125^{\circ}\text{C}$	I_{DSS}	—	0.1	5.0	μA
Drain-Source ON Resistance $V_{\text{BAT}} > 10\text{ V}$, $T_A = 25^{\circ}\text{C}$	R_{DSON1}	—	—	40	$\text{m}\Omega$
Drain-Source ON Resistance $V_{\text{BAT}} > 10\text{ V}$, $T_A = 150^{\circ}\text{C}$	R_{DSON2}	—	—	75	$\text{m}\Omega$
Negative Inductive Clamp Voltage $I_{\text{OUT}} = 1.0\text{ A}$	V_{CLAMP}	-4.0	—	-1.0	V

INPUT CHARACTERISTICS

High Input Voltage (IN1, IN2)	V_{IH}	3.25	—	—	V
High Input Voltage (OLDE)	V_{OLDEH}	3.5	—	—	V
Low Input Voltage (IN1, IN2, OLDE)	V_{IL}	—	—	1.5	V
Logic Input Hysteresis (IN1, IN2)	V_{HYS}	0.4	0.6	0.8	V
Logic Input Current $V_{\text{IN}} = 1.5\text{ V}$	I_{IN}	3.0	—	—	μA
Logic Input Current $V_{\text{IN}} = 3.25\text{ V}$	I_{IN}	—	—	32.5	μA
Logic Input Clamp Voltage At $I_{\text{IN}} = 1.0\text{ mA}$	V_{CLAMP}	5.5	—	7.0	V
Input Capacitance IN1, IN2 $R_{\text{IN}} = 47\text{ k}\Omega$ at 100 kHz	C_{IN}	—	—	80	pF

STATUS CHARACTERISTICS

Status Voltage $I_{\text{ST}} = 1.0\text{ mA}$, Output in Fault	V_{ST}	—	—	0.5	V
Status Leakage Current $V_{\text{ST}} = 5.0\text{ V}$	I_{STLK}	—	—	10	μA
Status Pin Capacitance $V_{\text{ST}} = 5.0\text{ V}$	C_{ST}	—	—	80	pF

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions T_J from $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, $6.0\text{ V} \leq V_{\text{BAT}} \leq 24\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^{\circ}\text{C}$ under nominal V_{BAT} conditions at time t_0 device characterization.

Characteristic	Symbol	Min	Typ	Max	Unit
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OVERLOAD PROTECTION CHARACTERISTICS

Overcurrent Latchoff Threshold $V_{\text{BAT}} = 13.5\text{ V}$	I_{OCT}	4.0	—	9.0	A
Thermal Shutdown	T_{SHUT}	150	165	175	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	T_{HYS}	—	—	10	$^{\circ}\text{C}$
Overvoltage Shutdown Threshold Both IN1, IN2 Logic High	V_{OV}	27	—	38	V
Overvoltage Shutdown Hysteresis Both IN1, IN2 Logic High	V_{OVHYS}	0.1	—	2.0	V
Undervoltage Shutdown Threshold Both IN1, IN2 Logic High	V_{UV}	4.75	—	6.0	V
Undervoltage Shutdown Hysteresis Both IN1, IN2 Logic High	V_{UVHYS}	0.3	0.6	1.0	V

OPEN CIRCUIT DETECTION CHARACTERISTICS

Open Load Detect Current $V_{\text{OUT}} = 3.5\text{ V}$, $\text{OLDE} = 4.0\text{ V}$	I_{OL}	200	290	400	μA
Open Load Threshold Voltage	V_{OL}	1.5	2.4	3.5	V
Open Load Threshold Voltage	V_{INOL}	1.5	2.5	3.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_J from $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, $6.0\text{ V} \leq V_{\text{BAT}} \leq 24\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^{\circ}\text{C}$ under nominal V_{BAT} conditions at time of device characterization.

Characteristic	Symbol	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS ($8.0\text{ V} < V_{\text{BAT}} < 18\text{ V}$, $R_{\text{LOAD}} = 7.0\ \Omega$)

Turn ON Slew Rate From 10% to $V_{\text{BAT}} - 3.0\text{ V}$	S_{RPOUT1}	1.0	—	2.0	V/ μs
Turn ON Slew Rate From $V_{\text{BAT}} - 3.0\text{ V}$ to 90%	S_{RPOUT2}	0.1	—	3.0	V/ μs
Turn OFF Slew Rate From 90% to 10%	S_{MOUT}	1.0	—	20	V/ μs
Turn ON Delay Time From $V_{\text{IN}2}$ to 10% V_{BAT}	t_{DON}	1.0	2.5	15	μs
Turn OFF Delay Time From $V_{\text{IN}2}$ to 90% V_{BAT}	t_{DOFF}	1.0	5.0	15	μs

OPEN CIRCUIT DETECTION CHARACTERISTICS

Open Load to Status Low Delay Time From $\text{IN} = 1.5$ to Status Flag $< 1.5\text{ V}$	t_{OLSTDT}	—	—	100	μs
Open Load Detect Blanking Time From $\text{IN} = 1.5$ to Open Load Circuitry Enable	t_{OLDBT}	3.0	10	50	μs

OVERLOAD PROTECTION CHARACTERISTICS

Overcurrent Latchoff Delay From Overcurrent Threshold Achieved to Output Voltage = 10% V_{BAT}	T_{OCTDLY}	—	—	30	μs
Overcurrent Latchoff Status Delay From Output Voltage = 10% V_{BAT} to Status Flag $< 1.0\text{ V}$	$T_{\text{OCTST-DLY}}$	—	—	50	μs

Table 1. Functional Truth Table

Conditions	IN1	IN2	OUT1	OUT2	ST1	ST2
Normal Operating Conditions	Low Level	Low Level	Low Level	Low Level	High Level	High Level
	High Level	Low Level	High Level	Low Level	High Level	High Level
	Low Level	High Level	Low Level	High Level	High Level	High Level
	High Level					
Overtemperature Channel 1 Overtemperature Channel 2 Overtemperature Channel 1/Channel 2	High Level	Don't Care	Low Level	Don't Care	Low Level	High Level
	Don't Care	High Level	Don't Care	Low Level	High Level	Low Level
	High Level	High Level	Low Level	Low Level	Low Level	Low Level
Open Load Channel 1 Open Load Channel 2	Low Level	Don't Care	High Level	Don't Care	Low Level	High Level
	Don't Care	Low Level	Don't Care	High Level	High Level	Low Level
Overcurrent Channel 1 Overcurrent Channel 2	High Level	Don't Care	Low Level	Don't Care	Low Level	High Level
	Don't Care	High Level	Don't Care	Low Level	High Level	Low Level
Undervoltage Condition	Don't Care	Don't Care	Low Level	Low Level	High Level	High Level
Overvoltage Condition	Don't Care	Don't Care	Low Level	Low Level	High Level	High Level

DEVICE DESCRIPTION

INTRODUCTION

The 33289 is a dual high-side switch with appropriate control, protection, and diagnostic features dedicated to drive inductive loads such as solenoid drivers for automotive and industrial applications. The device consists of two independent applications with two independent 40 mΩ power switches. It can be linked directly with a microcontroller. It is available in a SOICW 20 surface mount package.

Power Supply

The 33289 can be directly connected to the supply line. In Standby mode (in-1 and in-2 at 0V), the supply current is less than 5.0 μA for V_{BAT} supply voltage below 14 V. This feature allows a very low supply current on the battery, for example, when an auto is idle or parked. During OFF state, the status pins are in high impedance. In case of loss of (digital) ground, the power MOSFETs turn OFF in order to safely tie the load current to zero.

Nominal Voltage and Transient Operation

The nominal operation voltage is from 6.0 to 26 V. The 33289 device is functional over a larger voltage range from 6.0 V to 27V. The technology used for both power and analog circuitry sustains 40 V DC voltage.

Power Output Switches

The device has two independent high-side switches. Each switch is realized with an N-channel power MOSFET and includes current and temperature sensing circuitries. The MOSFET gates are driven by analog circuitry which includes charge pump and fault detection.

Each output has a 40 mΩ $R_{DS(on)}$ maximum 25°C. The $R_{DS(on)}$ value reaches 75 mΩ at 150°C junction temperature. Each output has a parasitic drain to source diode, inherent to any vertical MOSFET. This diode can sustain as much current at the MOSFET. The diode is reversed biased during normal operation of the MOSFET and is forward biased during reverse battery, or negative transient pulses.

Status

The device has an independent status pin per output, reporting an overtemperature, overcurrent, and an open load condition in the device. This pin is an open drain structure, requiring an external pull-up resistor. The device incorporates overtemperature sense on each output MOSFET in order to independently protect each output.

Open Load Function

The open load detection is active during the OFF phase, or cold open load detection. An amplifier measures the differential voltage between V_{BAT} and V_{OUT} .

When the load current is below 400 mA, the open load circuitry will pull down the status output. The open load circuitry can be disabled with the OLDE to ensure very low standby current.

Package

The device is assembled into a surface mount package.

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