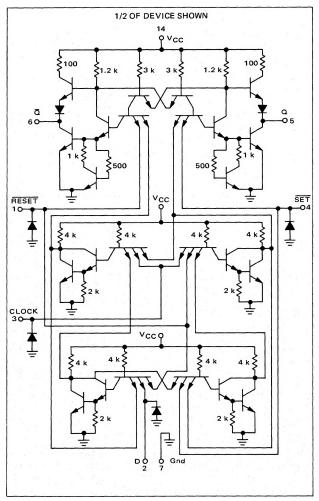
DUAL TYPE D FLIP-FLOP

MC3160F · MC3060F MC3160L · MC3060L,P



LOGIC DIAGRAM

RESET

1/2 OF DE VICE SHOWN

CLOCK

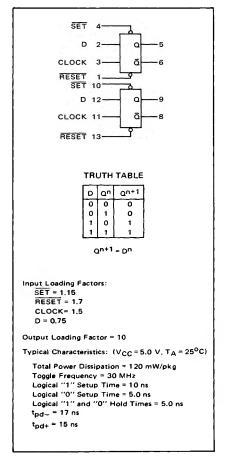
SET

See General Information section for packaging

This dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\overline{\rm Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct SET or RESET inputs.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

					õ	CLOCK	3-	T	Ø	9					L				TES	1	RENT	/V0LT/	TEST CURRENT/VOLTAGE VALUES					
					ľœ	RESET			6					@ Test			mA						Volts					
						SET	10 -	15	الم ا	σ			_E	Temperature	re lor	но,	- H	ا- ا	V _{II}	>	>	> 8	V _{RH}	V _{max}	Vccı	V _{CCH}		
)	4		7)) —55°C	C 20	-2.0	- 0	-	1.1	2.0	0.4	2.4	4.0	1	4.5	5.5		
					ฉ	CLOCK 11-	11-	T	10	8		Σ	MC3160	1+25°C	C 20	-2.0	0 1.0	0 -10	1.1	1.8	0.4	2.4	4.0	7.0	4.5	5.5		
					ΙŒ	RESET 13	13-	1	6					(+125°C	ς 20	-2.0	- 0	1	0.8	1.8	0.4	2.4	4.0	-	4.5	5.5		
														0	0°C 20	-2.0	- 0	-	1.1	2.0	0.4	2.5	4.0	,	4,75	5.75	_	
												Σ.	MC3060	\ +25°C	ر 20	-2.0	0 1.0	01-0	1.1	1.8	0.4	2.5	4.0	7.0	4.75	5,75		
			7. J											(+75°C	°C 20	-2.0	0	'	0.9	1.8	0.4	2.5	4.0	,1	4.75	5,75		
		Pin			2	est Lii	mits			MC30	MC3060 Test Limits	Limit	s		_		TEST CL	IREN	1/V0L	TAGE	APPL	ED 10	FEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:	BELOV	ت			
Characteristic	Cymbol	Under		—55°C	-	+25°C	+125°C	+125°C	O N	1	+25°C		+75°C	1			=	-	>	>	>	>	V	>	>	7	*_	Gnd
Input Forward Current	IFC	g ~	'	-3.0	-	-3.0		-3.0		-3.0	1		-3.0	-	+	+-	1-	_		_	+-	+	-	1		41		2,4,7,11
	LFD	2	'	-1.5		-1.5		-1.5	1	-1.5	7	-1.5	1.5	5 mAdc	0	-	'	1	Ŀ	<u> </u>	2	-	1,4	•		14		3,7,11
	I _F §	4	1	-2.3	,	-2.3	1	-2.3	1	-2.3	1	-2.3	2.3	3 mAdc	- 0	-	,		'	'	4		1	,		14	,	2,3,7,11
	LFE	1	1	-3.4	1	-3.4	1	-3.4		-3.4	1	-3.4	3.4	1 mAdc	2	<u> </u>	1	1		,	-		2,4	1	1	14	1	3,7,11
Leakage Current	^I RC	8	1.	100	1	100	1	100		100	- 1	100	- 100	μAdc	0	-	-	'	'	'	-	8	4	1,	. 1	14	1	1,2,7,11
	L _{RD}	23	,	20	1	20	1	20	1	20	45	- 09	20	μAdc	0	<u>'</u>	1	'	1	'	'	2	3,4			14	1	1,7,11
	IRĒ	4		100	1	100	,	100	1	100	-	100	- 100	μAdc	0	-	'	1	1	'	<u>'</u>	4	1,2			14	က	7,11
	IRE	7		140	1	140		140		140	-	140 -	140	μAdc	0	'	-	!	'	1	'	-	4	'	,	14	e5	2,7,11
Breakdown Voltage	BV _{in}	8844	1111	114	5.5	1111		1111	1 1 1 1	1 1 1 1		1 1 1 1		Vdc			884-	1111		1111	1111	1111	3,4 1,2 4	1111	,,,,	41	1 100	1,2,7,11 1,7,11 7,11 2,7,11
Clamp Voltage	$^{\Lambda}_{\mathrm{D}}$	8241	inte	1111	1111	-1.5	1,111	9111	471.1	1111	7	-1.5	1 1 1 1	Vdc			1111	8244	1111	1111	1111			1111	14		1111	7,11
Output Output Voltage	ТОЛ	9 10	. 1 1	0.4	1 1	0.4	1.1	0.4	1.1	0.4	00	0.4	0.4	Vdc	9.0	1.1	1.1	1.1	41	1.4	' '	1 1		1.1	14 14	1 1	1 1	2,3,7,11 2,3,7,11
,	МОЛ	9 2	2.4	ir	2.4	1.1	2.4	13	2.5	111	2.5	25	2 2	Vde	0.0	915	1 1	1 1	T 4	4	1 1	1 1		1 (14	, ,	1 1	2,3,7,11
Short-Circuit Current	Js	9 5	-20	-65	-20	-65	-20	-65	-20-	-65	-20	-65 -20 -65 -20	0 -65	mAdc mAdc	lc ic	1 1	1 1	1 1		4	1 4	1 1		- 1	1 1	14	1 1	6,7,11 5,7,11
Power Requirements (Total Device) Maximum Power Supply Current	Imax	14		1	. !	42				,1	4	42	1	mAdc	- le			'	,	-	'	1	1,13	14	,	,		3,4,7,10,11
Power Supply Drain	TPD	14	1	31		31	1	31	,	31	- 3	31 -	31	mAde	- le	_	-	Ŀ	,	1	-		4,10		1	-14	1	1,3,7,11,13

* Pulse is used to set flip-flop in desired state. $P_1 = \prod_{n=0}^{4} V(VRH)$. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

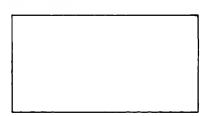
OPERATING CHARACTERISTICS

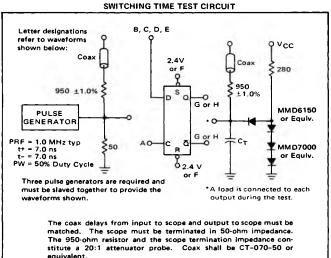
Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct SET and RESET inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.





CT = 25 pF = total parasitic capacitance, which includes probe,

VOLTAGE WAVEFORMS AND DEFINITIONS

wiring, and load capacitances.

