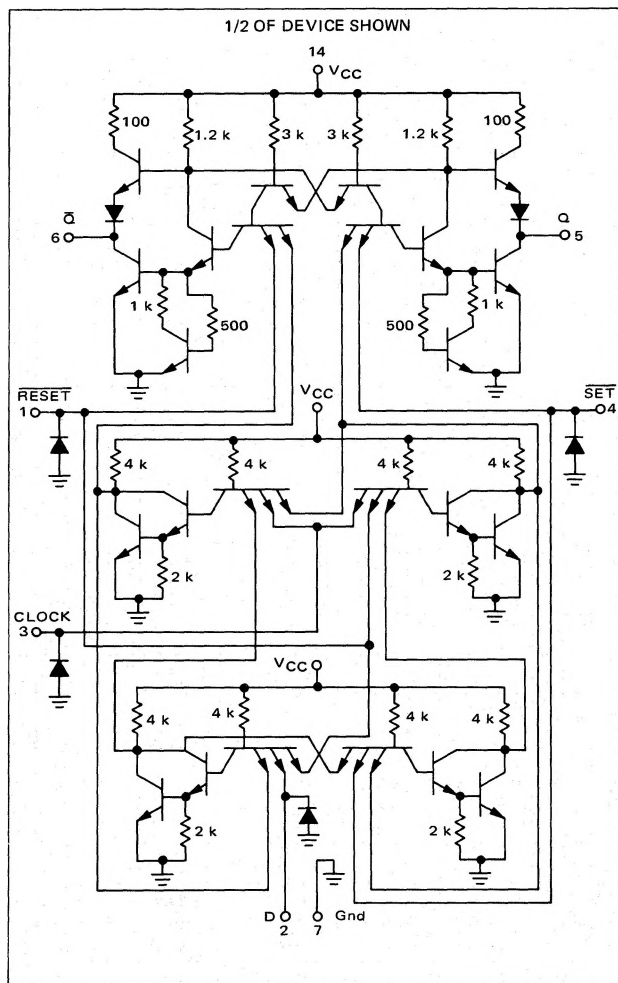


DUAL TYPE D FLIP-FLOP

MC3100/MC3000 series

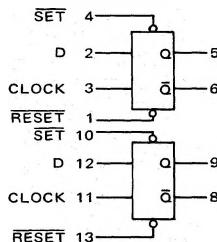
MC3160F • MC3060F MC3160L • MC3060L,P



This dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and \bar{Q} respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct SET or RESET inputs.



TRUTH TABLE

D	Q ⁿ	Q ⁿ⁺¹
0	0	0
0	1	0
1	0	1
1	1	1

$$Q^{n+1} = D^n$$

Input Loading Factors:

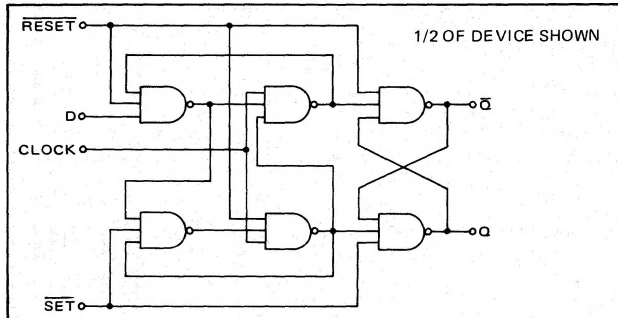
SET = 1.15
RESET = 1.7
CLOCK = 1.5
D = 0.75

Output Loading Factor = 10

Typical Characteristics: ($V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$)

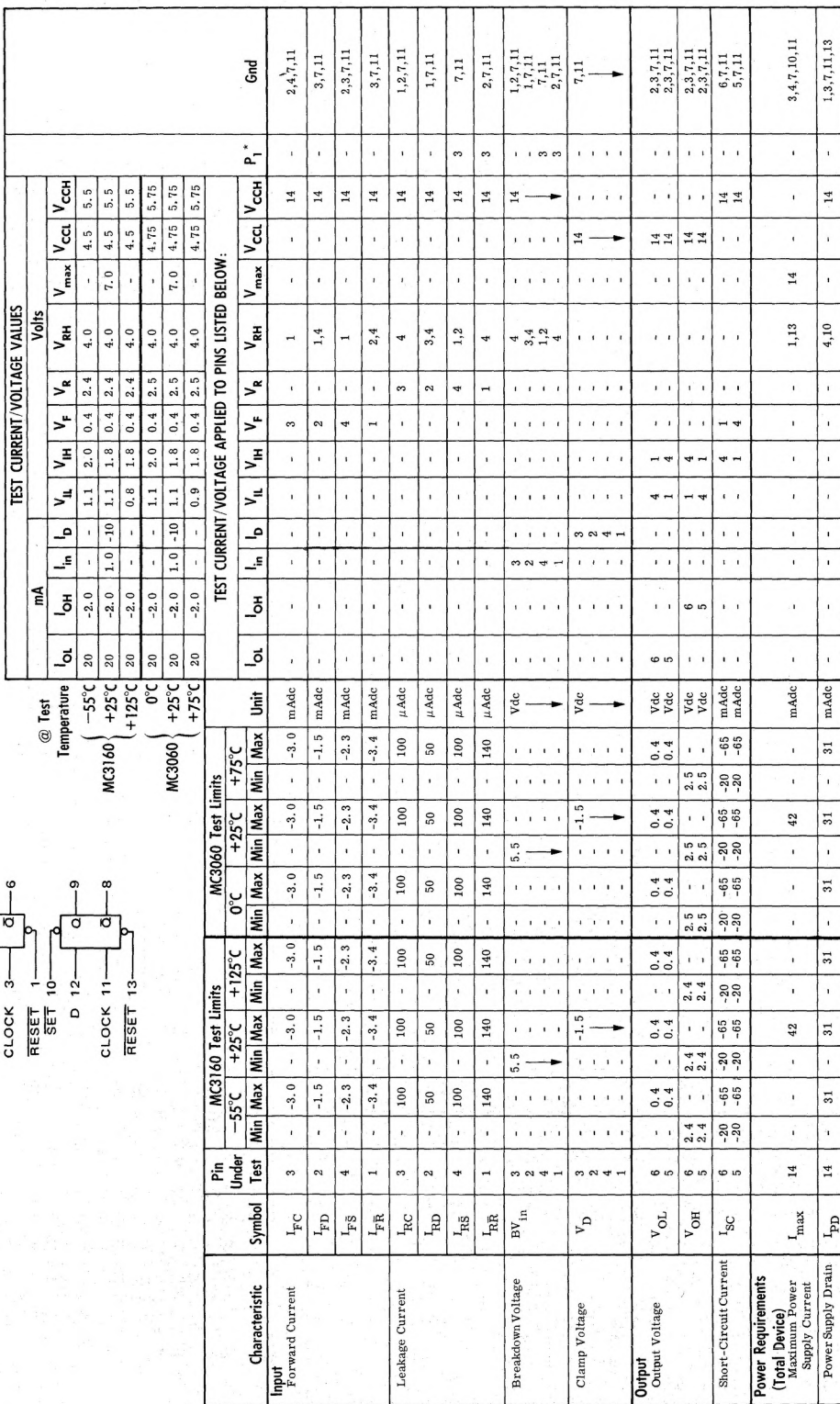
Total Power Dissipation = 120 mW/pkg
Toggle Frequency = 30 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Setup Time = 5.0 ns
Logical "1" and "0" Hold Times = 5.0 ns
 $t_{pd-} = 17$ ns
 $t_{pd+} = 15$ ns

LOGIC DIAGRAM



See General Information section for packaging

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



* Pulse is used to set flip-flop in desired state. $P_1 = \begin{cases} 4.0 \text{ V (VRH)} \\ 0 \text{ V} \end{cases}$. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

OPERATING CHARACTERISTICS

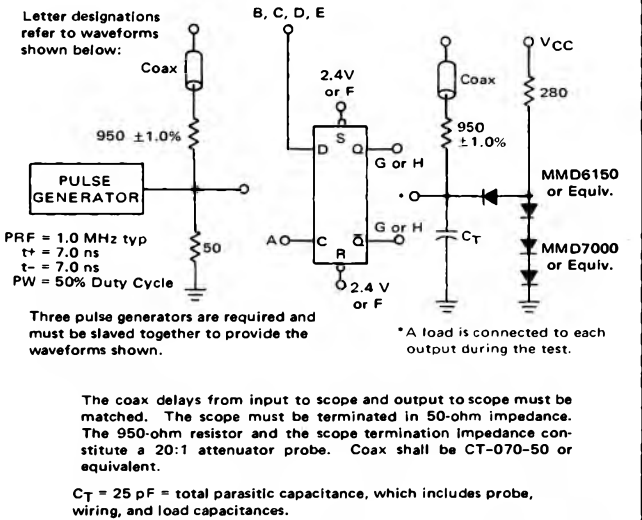
Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct SET and RESET inputs may be used at any time as they completely override the clock.

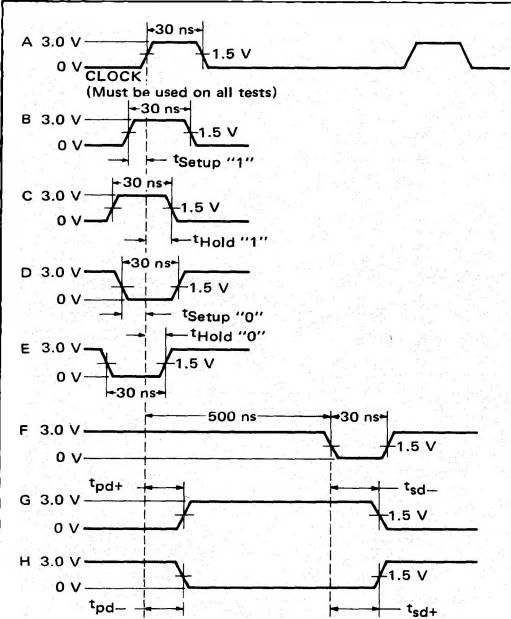
Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT			Q*	Q*	LIMITS (ns)	
	D*	SET*	RESET*			Min	Max
$t_{Setup}^{"1"}$	D	B	2.4 V	F	G	H	15
$t_{Hold}^{"1"}$	D	C	2.4 V	F	G	H	5.0
$t_{Setup}^{"0"}$	D	D	F	2.4 V	H	G	15
$t_{Hold}^{"0"}$	D	E	F	2.4 V	H	G	5.0
t_{pd+}	Delay from clock to Q during $t_{Setup}^{"1"}$ D test. Delay from clock to \bar{Q} during $t_{Setup}^{"0"}$ D test.					10	25
t_{pd-}	Delay from clock to Q during $t_{Setup}^{"0"}$ D test. Delay from clock to \bar{Q} during $t_{Setup}^{"1"}$ D test.					10	25
t_{sd+}	Delay from SET to Q during $t_{Setup}^{"0"}$ D test. Delay from RESET to \bar{Q} during $t_{Setup}^{"1"}$ D test.					5.0	20
t_{sd-}	Delay from SET to \bar{Q} during $t_{Setup}^{"0"}$ D test. Delay from RESET to Q during $t_{Setup}^{"1"}$ D test.					5.0	20

* Letters shown in these columns refer to waveforms at left.