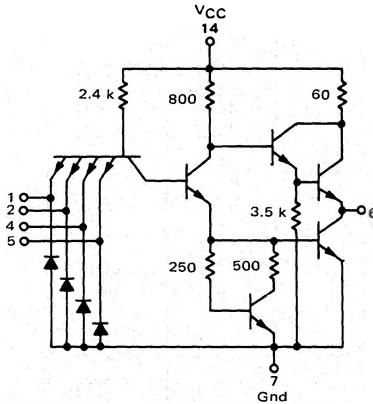


DUAL 4-INPUT "NAND" GATE

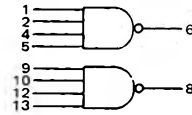
MC3100/MC3000 series

MC3110F • MC3010F MC3110L • MC3010L,P (54H20J) (74H20J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.



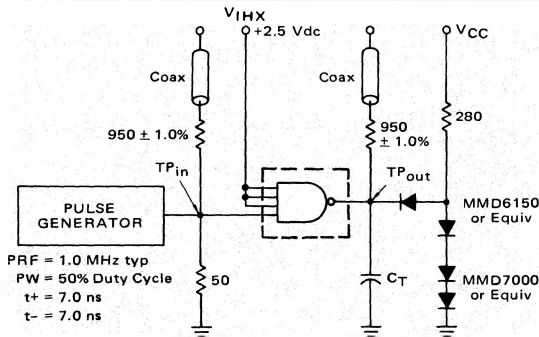
Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H20F/74H20F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3110F,L/3010F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H20F/74H20F	1	12	3	13	14	2	11	10	6	7	14	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



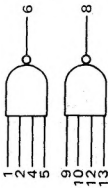
$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic		Pin Under Test	MC3110 Test Limits						MC3010 Test Limits						TEST CURRENT / VOLTAGE VALUES															
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	I _{OL}	I _{OH}	I _{IN}	I _{ID}	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}		
Input																														
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mA	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*	
Leakage Current	I _R	1	-	50	-	50	-	50	-	50	-	50	-	50	-	50	μA	-	-	-	1	-	-	-	-	-	14	-	2, 4, 5, 7*	
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	-	-	V	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*	
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	-	-	V	-	-	-	-	-	-	-	-	14	-	7		
Output																														
Output Voltage	V _{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V	-	-	-	1	-	2, 4, 5	-	-	14	-	7*		
	V _{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	2.5	-	V	-	6	-	-	-	2, 4, 5	-	-	14	-	7*		
Short-Circuit Current	I _{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mA	-	-	-	-	-	-	-	-	-	14	-	7*	
Power Requirements (Test Device)																														
Maximum Power Supply Current	I _{max}	14	-	-	-	12.5	-	-	-	-	-	-	-	12.5	-	-	mA	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	
Power Supply Drain	I _{PDH}	14	-	20	-	20	-	20	-	20	-	20	-	20	-	20	mA	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	14	-	7	
	I _{PDL}	14	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	mA	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13	
Switching Parameters																														
Turn-On Delay	t _{pd-}	1, 6	-	-	-	10	-	-	-	-	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	14	-	-	2, 4, 5	7*	
Turn-Off Delay	t _{pd+}	1, 6	-	-	-	10	-	-	-	-	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	14	-	-	2, 4, 5	7*	

*Since this is an inverting gate, power drain is minimised by grounding the inputs to gates not under test.