

DUAL J-K FLIP-FLOP

MC3100/MC3000 series

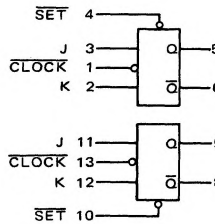
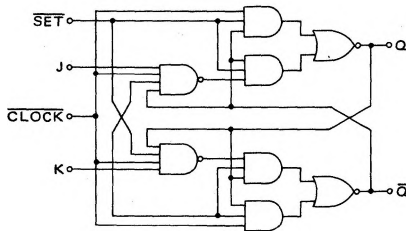
MC3162F • MC3062F MC3162L • MC3062L,P

This dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN



Input Loading Factors:
CLOCK, SET = 1.75
J, K, = 0.75

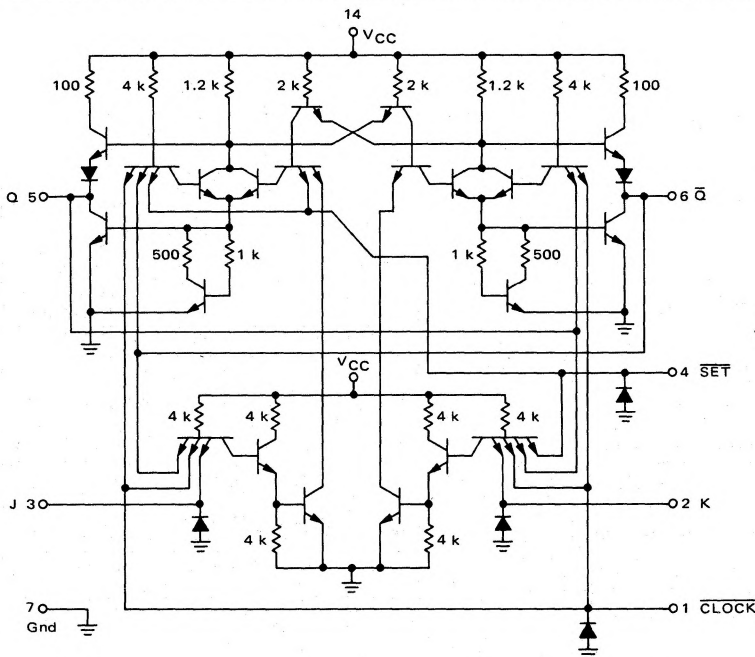
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q ⁿ	Q ⁿ⁺¹
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd+} = 12 ns
t_{pd-} = 12 ns



CIRCUIT SCHEMATIC
1/2 OF DEVICE SHOWN

ELECTRICAL CHARACTERISTICS

[illegible]

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

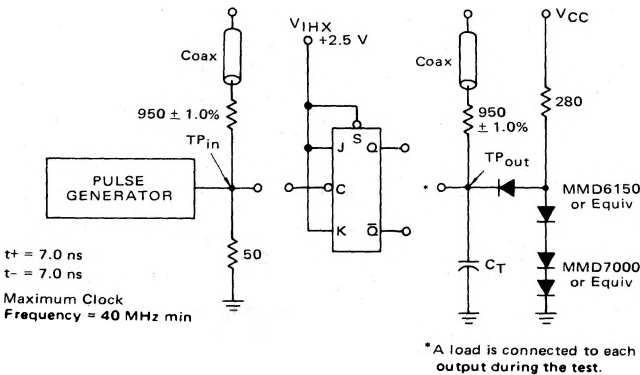
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the $Q = 1$ state by applying a low level to the **SET** input. The direct **SET** inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

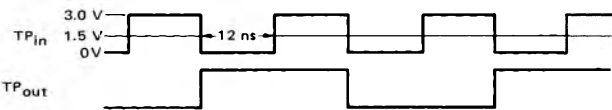
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

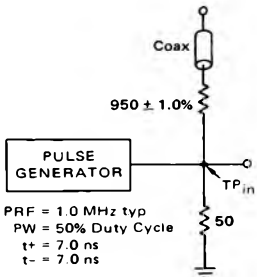
VOLTAGE WAVEFORMS AND DEFINITIONS



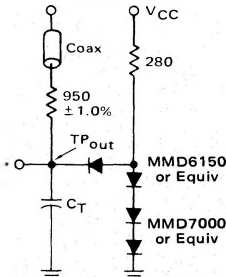
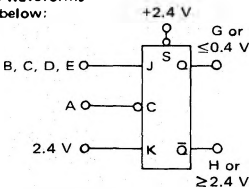
MC3162, MC3062 (continued)

OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT
(For J Inputs; to test other inputs, refer to Test Procedures Chart)



Letter designations refer to waveforms shown below:



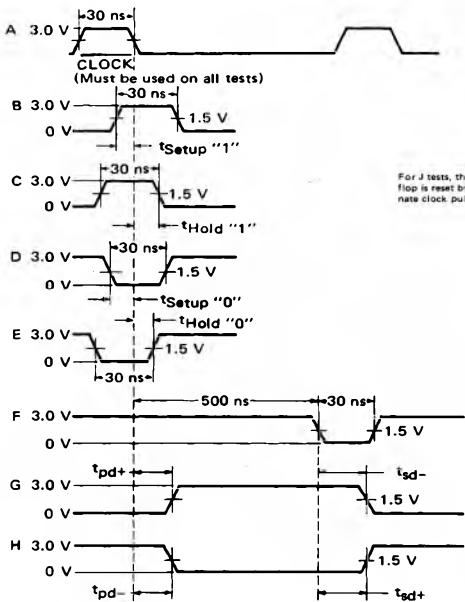
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

$C_T = 25\text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



For J tests, the flip-flop is reset by alternate clock pulses.

TEST PROCEDURES CHART

TEST	INPUT					LIMITS (ns)
	J*	SET*	K*	Q*	Q-bar*	
t _{Setup} "1" J	B	2.4 V	2.4 V	G	H	15
t _{Hold} "1" J	C	2.4 V	2.4 V	G	H	0**
t _{Setup} "0" J	D	2.4 V	2.4 V	≤0.4 V	≥2.4 V	15
t _{Hold} "0" J	E	2.4 V	2.4 V	≤0.4 V	≥2.4 V	0**
t _{Setup} "1" K	Gnd	F	B	H	G	15
t _{Hold} "1" K	Gnd	F	C	H	G	0**
t _{Setup} "0" K	Gnd	F	D	≥2.4 V	≤0.4 V	15
t _{Hold} "0" K	Gnd	F	E	≥2.4 V	≤0.4 V	0**
t _{pd} +	Delay from CLOCK to Q during t _{Setup} "1" J test. Delay from CLOCK to Q during t _{Setup} "1" K test.					18
t _{pd} -	Delay from CLOCK to Q during t _{Setup} "1" J test. Delay from CLOCK to Q during t _{Setup} "1" K test.					18
t _{sd} +	Delay from SET to Q during t _{Setup} "1" K test.					18
t _{sd} -	Delay from SET to Q during t _{Setup} "1" K test.					18

* Letters shown in test columns refer to waveforms shown at the left.

** t_{Hold} is typically a negative number.