

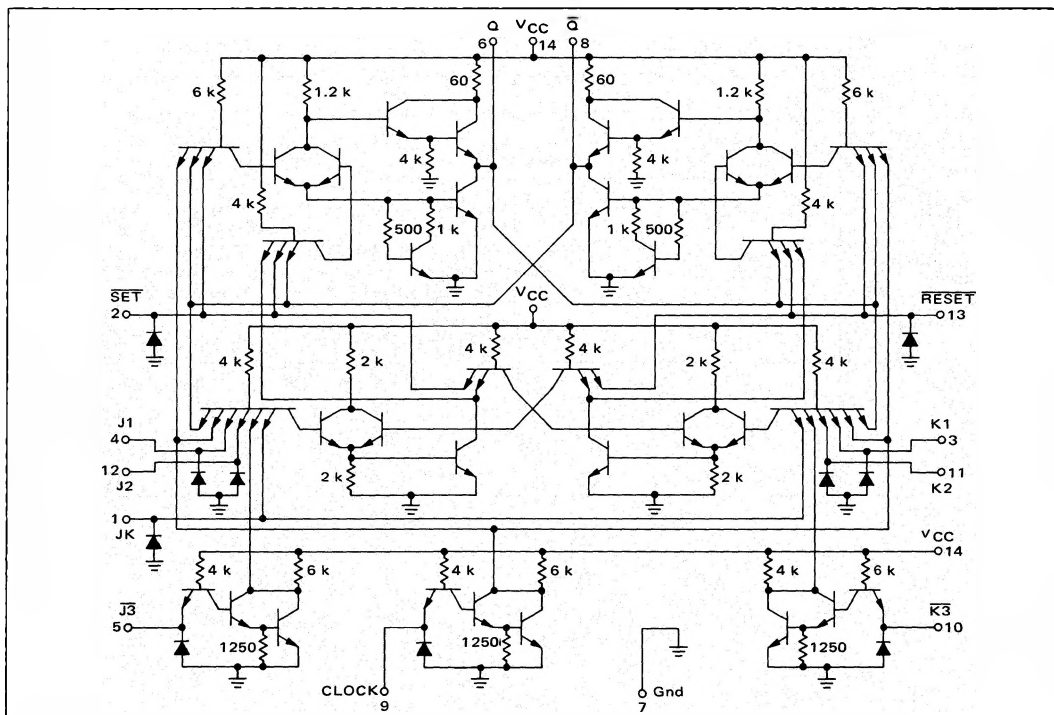
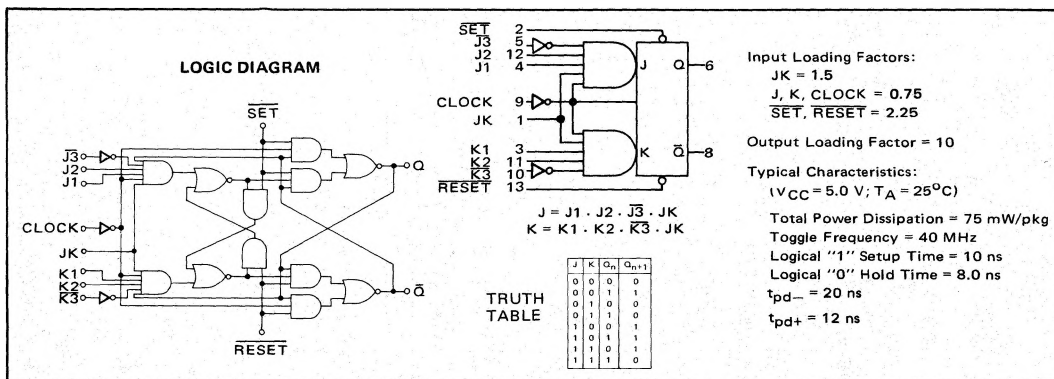
"AND" INPUT $\overline{J}\overline{K}$
FLIP-FLOP

MC3100/MC3000 series

MC3152F • MC3052F
MC3152L • MC3052L,P

This is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a $\overline{J}$ -input ANDed together and two K-inputs and a $\overline{K}$ -input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, $\overline{J}$, K and $\overline{K}$) or an additional logic input (JK) for use in counters or certain other applications. A direct SET and RESET are provided to enable presetting data into the flip-flop such as initial conditions. The direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

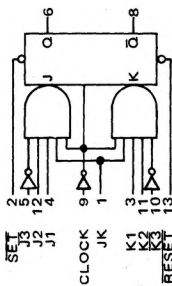
Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct SET or RESET provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct SET or RESET inputs.



See General Information section for packaging.

MC3152, MC3052 (continued)

ELECTRICAL CHARACTERISTICS

[illegible]

OPERATING CHARACTERISTICS

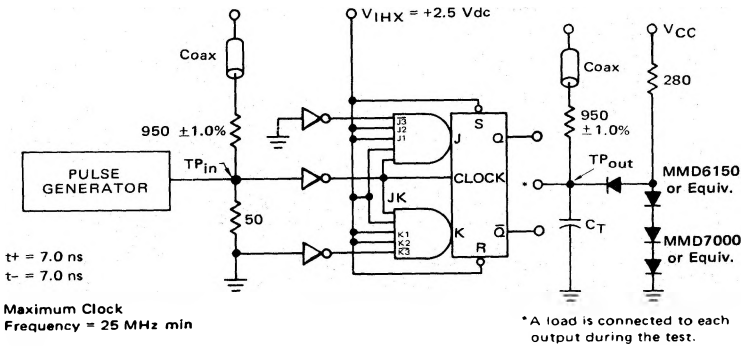
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the SET input sets Q high and low level on the RESET input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering – When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused J and K inputs must be tied to ground. The unused SET and RESET inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

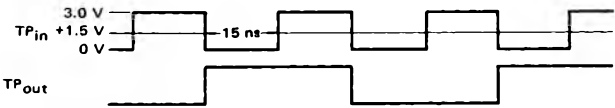
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

WAVEFORMS AND DEFINITIONS

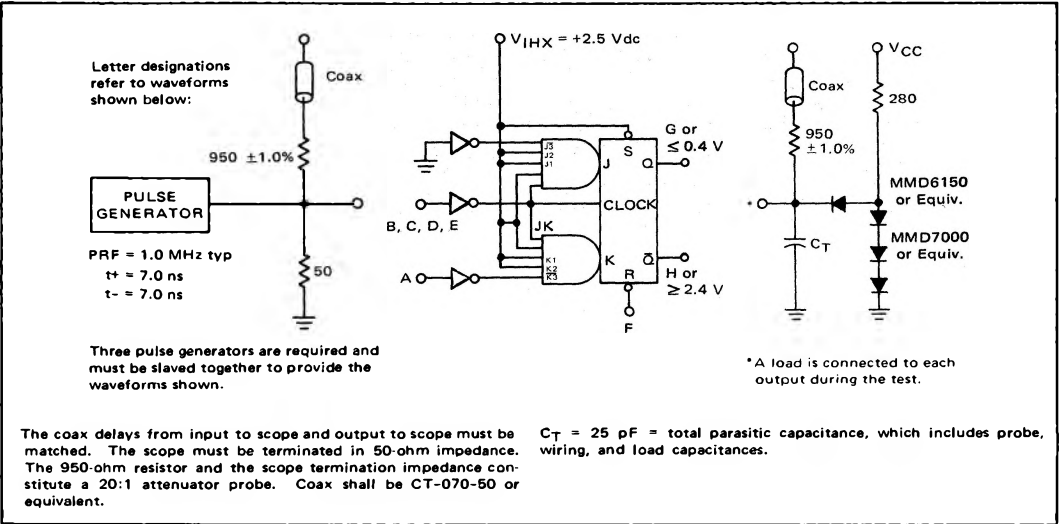


MC3152, MC3052 (continued)

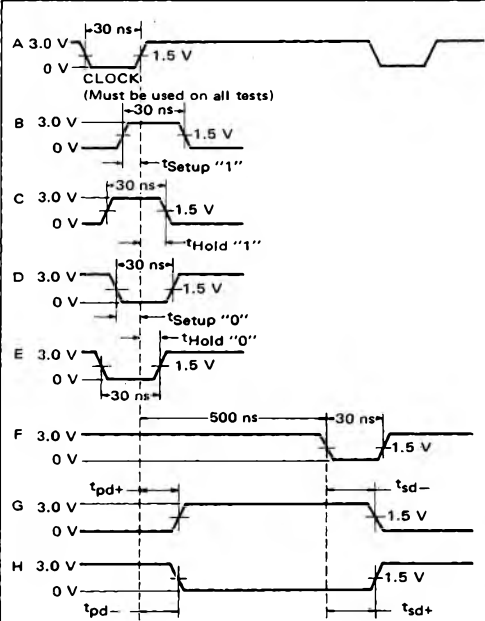
OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT						Q*	Q*	LIMITS (ns)	
	J*	J*	SET*	RESET*	K*	R*			Min	Max
t_{Setup} "1" J	C	Gnd	2.4 V	F	Gnd	Gnd	G	H	-	15
t_{Hold} "0" J	B	Gnd	2.4 V	F	Gnd	Gnd	≤ 0.4 V	≥ 2.4 V	-	-3.0
t_{Setup} "1" K	Gnd	Gnd	F	2.4 V	C	Gnd	H	G	-	15
t_{Hold} "0" K	Gnd	Gnd	F	2.4 V	B	Gnd	≥ 2.4 V	≤ 0.4 V	-	-3.0
t_{Setup} "1" J	2.4 V	E	2.4 V	F	2.4 V	Gnd	G	H	-	15
t_{Hold} "0" J	2.4 V	D	2.4 V	F	2.4 V	Gnd	≤ 0.4 V	≥ 2.4 V	-	-3.0
t_{Setup} "1" R	2.4 V	Gnd	F	2.4 V	E	H	G	-	-	15
t_{Hold} "0" R	2.4 V	Gnd	F	2.4 V	2.4 V	D	≥ 2.4 V	≤ 0.4 V	-	-3.0
t_{pd+}	Delay from clock to Q during t_{Setup} "1" J test. Delay from clock to Q during t_{Setup} "1" K test.								8	20
t_{pd-}	Delay from clock to Q during t_{Setup} "1" J test. Delay from clock to Q during t_{Setup} "1" K test.								14	28
t_{sd+}	Delay from SET to Q during t_{Setup} "1" K test. Delay from RESET to Q during t_{Setup} "1" J test.								-	18
t_{sd-}	Delay from SET to Q during t_{Setup} "1" K test. Delay from RESET to Q during t_{Setup} "1" J test.								-	25

*Letters shown in these columns refer to waveforms.