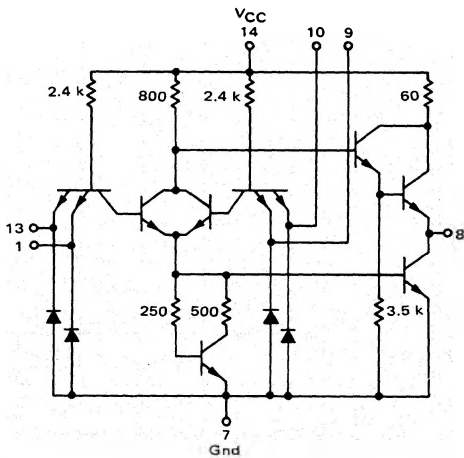


**DUAL 2-WIDE 2-INPUT
"AND-OR-INVERT" GATE**

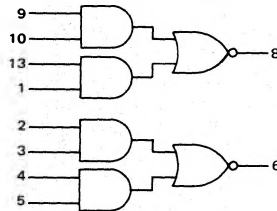
MC3100/MC3000 series

MC3123F • MC3023F
MC3123L • MC3023L,P
(54H51J) (74H51J, N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This dual device consists of two 2-input AND gates ORed together and driving an output inverter.



Positive Logic:

$$8 = (9 + 10) + (13 + 1)$$

Negative Logic:

$$8 = (9 + 10) + (13 + 1)$$

Input Loading Factor = 1

Output Loading Factor = 10

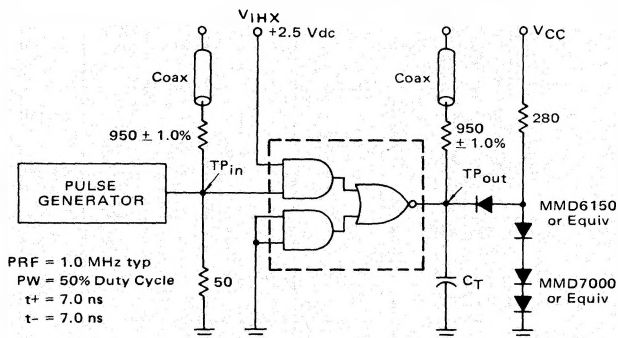
Total Power Dissipation = 62.5 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H51F/74H51F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3123F,L/3023F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H51F/74H51F	5	6	7	8	9	10	11	12	13	14	1	2	3	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

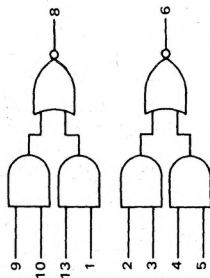


$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



		TEST CURRENT / VOLTAGE VALUES																												
		Volts																												
		mA																												
		I _{OL}	I _{OH}	I _{IN}	I _{DD}	V _{IL}	V _{IH}	V _F	V _R	V _{BH}	V _{max}	V _{CC}	V _{CCL}	V _{CH}	V _{HH}															
Input	Characteristic	Symbol	Pin Under Test	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														Pin Under Test	6nd											
				MC3023 Test Limits																										
				-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit														
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max													
				I _F	1	-	-2.0	-	-2.0	-	2.0	-	-2.0	-	-2.0	-	-2.0			-	mAdc	-	-	-	1	-	13	-	-	14
I _R	1	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	μAdc	-	-	-	1	-	-	-	14	-	7, 9, 10, 13*			
Breakdown Voltage	BV _{IN}	1	-	-	5.5	-	-	-	5.5	-	-	-	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	7, 9, 10, 13*
Clamp Voltage	V _D	1	-	-	-1.5	-	-	-	-1.5	-	-	-	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	7, 9, 10*	
Output	Output Voltage	V _{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	8	-	-	-	-	-	-	-	-	-	-	-	-	7, 9, 10*	
Short-Circuit Current	I _{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 7, 9, 10, 13*
Power Requirements (Total Device)	Maximum Power Supply Current	I _{max}	14	-	-	20	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Power Supply Drain	I _{PDH}	14	-	24	-	24	-	24	-	24	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	7
Power Supply Drain	I _{PDL}	14	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Switching Parameters	Turn-On Delay	t _{pd-}	1, 8	-	-	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13
Turn-Off Delay	t _{pd+}	1, 8	-	-	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.