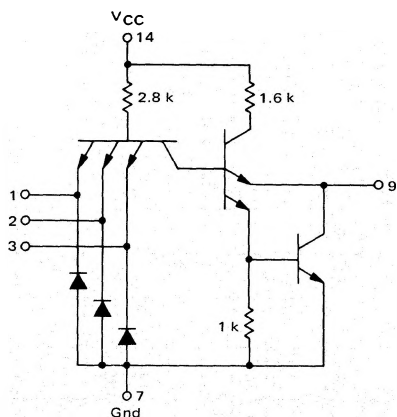


TRIPLE 3-INPUT EXPANDER
FOR "AND-OR" GATES

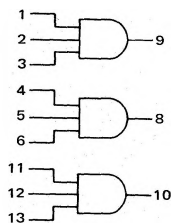
MC3100/MC3000 series

MC3119F • MC3019F
MC3119L • MC3019L,P
(54H61J) (74H61J, N)

1/3 OF CIRCUIT SHOWN



This device consists of three independent 3-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3019 expander, with the MC3031 expandable gate, up to six AND gates can be Ored together.



Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.

Total Power Dissipation = 25 mW typ/pkg

Propagation Delay Time:

$\Delta t_{pd1} = +0.4$ ns typ

$\Delta t_{pd0} = +0.05$ ns typ

When added to the expandable "AND-OR" gate.

$\Delta t_{pd1}/pF = +0.3$ ns/pF typ

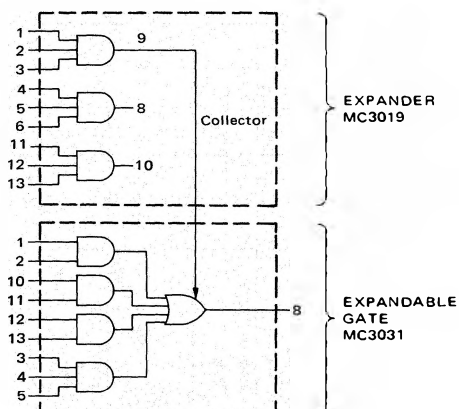
$\Delta t_{pd0}/pF = +0.04$ ns/pF typ

Caused by additional capacitance at expansion points.

Pin numbers for the 54H61F/74H61F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3119F,L/3019F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H61F/74H61F	1	2	3	5	6	7	11	13	14	12	8	9	10	4

APPLICATION: EXPANDABLE 4-WIDE 2-2-2-3-INPUT AND-OR GATE
WITH A TRIPLE 3-INPUT EXPANDER CONNECTED



Positive Logic:

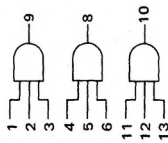
$$8 = (1 \cdot 2) + (3 \cdot 4 \cdot 5) + (10 \cdot 11) + (12 \cdot 13) + (1 \cdot 2 \cdot 3)$$

Expandable Gate

Expander

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



Characteristics		Pin Under Test	TEST CURRENT/VOLTAGE VALUES																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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*Ground inputs to gates not under test.