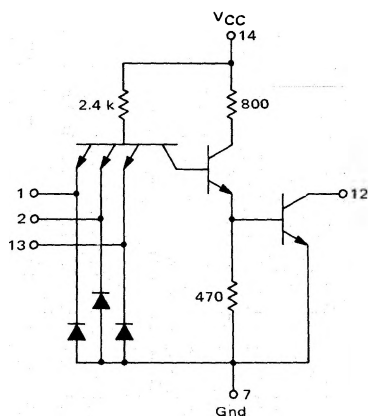


TRIPLE 3-INPUT "NAND" GATE
(Open Collector)

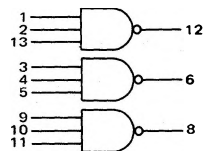
MC3100/MC3000 series

MC3107F • MC3007F
MC3107L • MC3007L,P

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



This device consists of three 3-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.

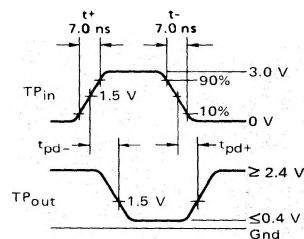
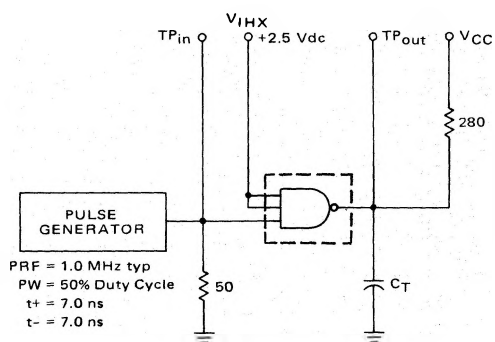


Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$

Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

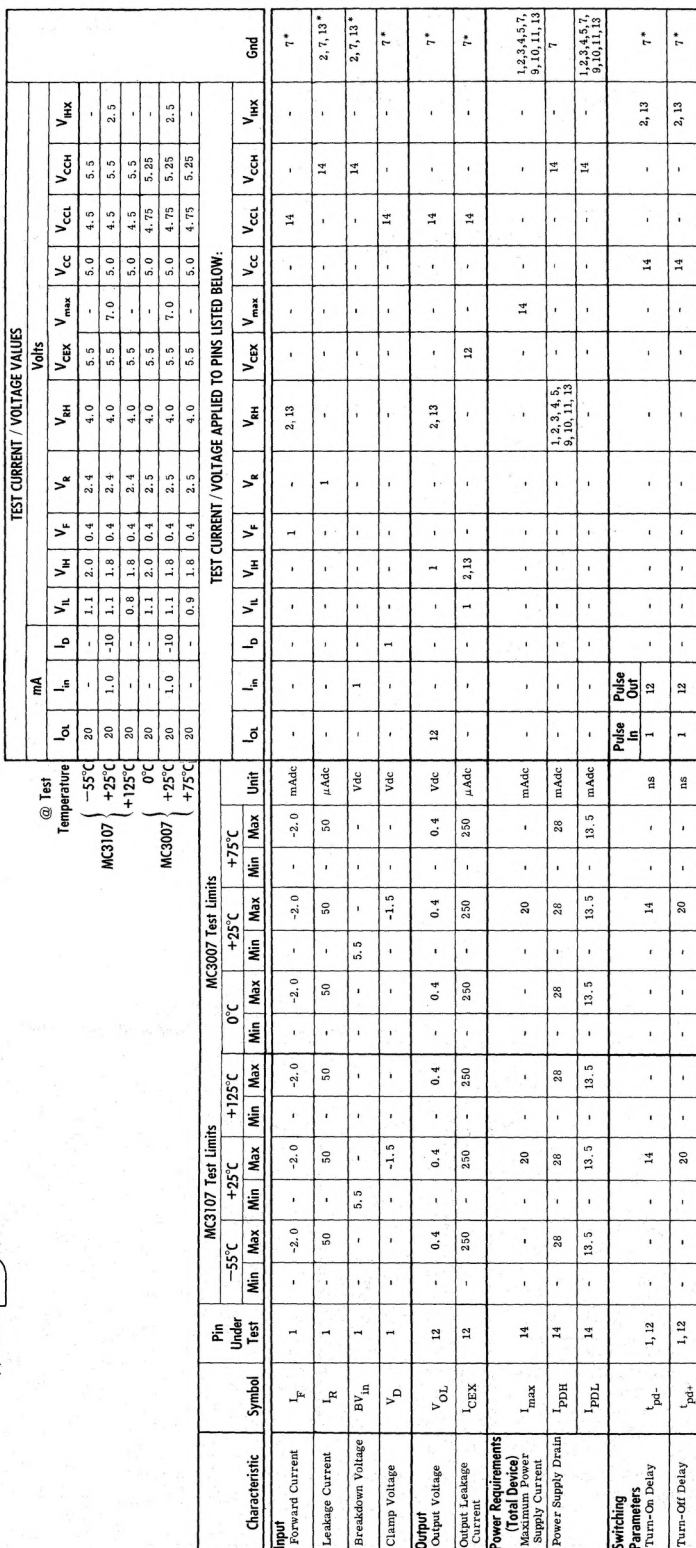
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.