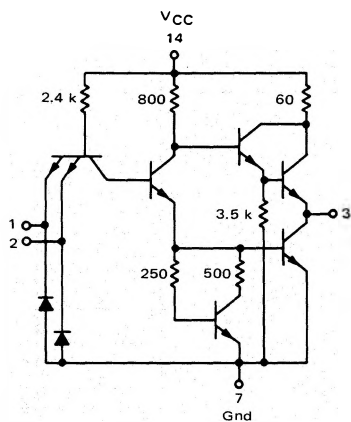


QUAD 2-INPUT "NAND" GATE

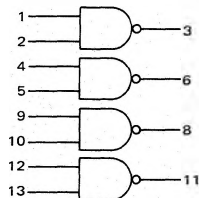
MC3100/MC3000 series

MC3100F • MC3000F
MC3100L • MC3000L,P
 (54H00J) (74H00J,N)

CIRCUIT SCHEMATIC
 1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



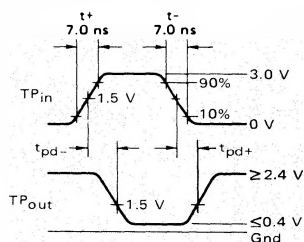
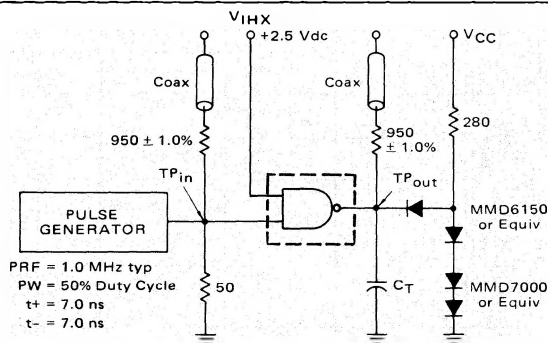
Positive Logic: $3 = \overline{1 \cdot 2}$
 Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
 Output Loading Factor = 10
 Total Power Dissipation = 88 mW typ/pkg
 Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H00F/74H00F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS															
MC3100F,L/3000F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
54H00F/74H00F	1	2	3	6	7	5	11	8	9	10	14	12	13	4		

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

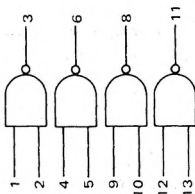


$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.