MC1581L

MONOLITHIC DUAL MECL LINE RECEIVER

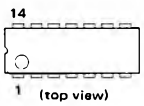
. . . designed with output emitter follower voltage levels that switch in response to a differential input voltage. The device output voltage levels are compatible with that of the MECL digital logic family. With its excellent common-mode input voltage range, the MC1581L is ideally suited for receiving digital data in noisy environments. Typical applications include line sharing, voltage comparator, and level translation.

- High Input Impedance – 8.0 k ohms @ 10 MHz
- Low Propagation Delay Time – 20 ns max
- Wide Common-Mode Input Voltage Range – ±3.5 Vdc
- Device Compatability with Other Members of the Line Driver/Receiver Series

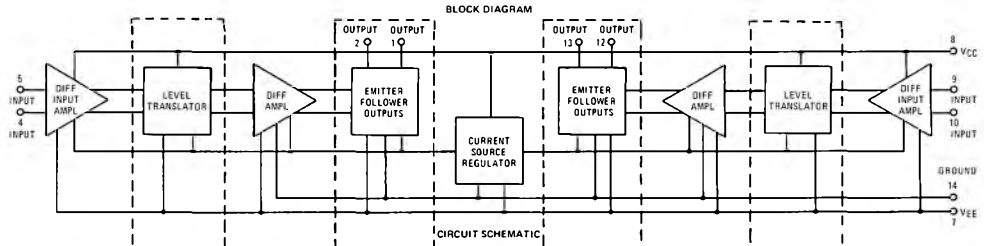
DUAL MECL LINE RECEIVER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

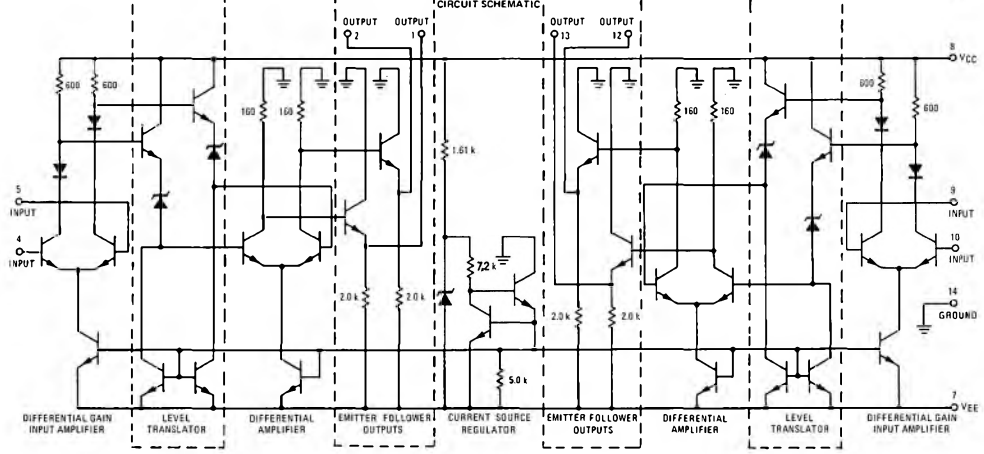
CASE 632
CERAMIC PACKAGE
TO-116



BLOCK DIAGRAM



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage	V_{in}	±7.0	Volts
Common-Mode Input Signal Voltage	CMV_{in}	±10	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 575 3.85	 mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Each Receiver, V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Operating Supply Currents	1	I_{CC} I_{EE}	– –	5.3 22.2	8.0 28.1	mA
Input Leakage Current	1	I_R	–	–	0.1	μA
Input Current T_A = -55°C T_A = +25°C T_A = +125°C	1	I_{in}	 – – –	 0.020 0.014 0.012	 0.1 0.1 0.1	mA
Output Voltage High T_A = -55°C T_A = +25°C T_A = +125°C	1	V_{OH}	 -0.825 -0.690 -0.535	 -0.900 -0.780 -0.62	 -0.990 -0.850 -0.700	Volt
Output Voltage Low T_A = -55°C T_A = +25°C T_A = +125°C	1	V_{OL}	 -1.580 -1.500 -1.380	 -1.83 -1.70 -1.73	 – – –	Volts
Input Voltage Transition Width* T_A = -55°C T_A = +25°C T_A = +125°C		V_{TR}	 – – –	 20 20 30	 50 50 50	mV
Switching Times Propagation Delay Time Rise Time Fall Time	2	 t_{pd+} t_{pd-} t_r t_f	 – – – –	 15 25 12 23	 20 30 – –	ns
Parallel Input Impedance (f = 5.0 MHz) Capacitance Resistance		 $C_{p\ (in)}$ $R_{p\ (in)}$	 – –	 4.5 14	 – –	 pF k ohms
Common-Mode Input Voltage Range (T_A = -55 to +125°C)	3	$CMVR_{in}$	+3.5 -3.5	+4.4 -4.2	– –	Volts
Power Supply Operating Range		V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.2	+6.00 -6.00	Vdc
Total Power Dissipation		P_D	–	145	185	mW

*Measurement taken from points of Unity Gain.
Ground unused inputs to assure correct device biasing.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS AND VOLTAGES

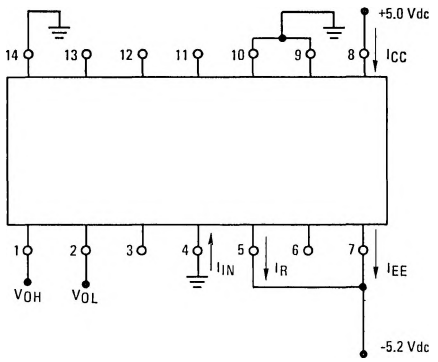


FIGURE 2 – TRANSIENT RESPONSE

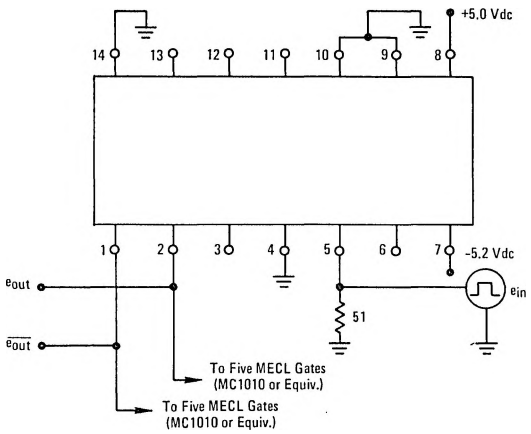
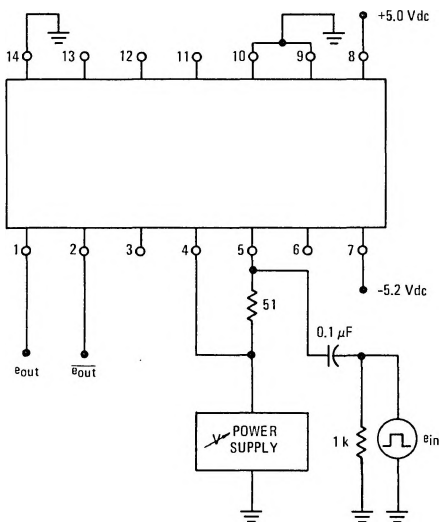
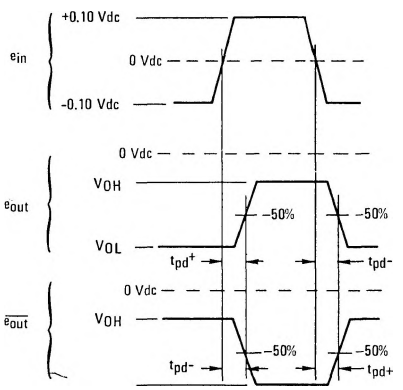
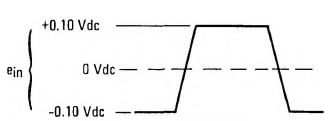


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE







Common-Mode Input Voltage Range is that value of the variable supply ~~(-V)~~ which causes a 10% shift in e_{out} or $\overline{e_{out}}$ whichever occurs first.

TYPICAL CHARACTERISTICS

FIGURE 4 – OUTPUT VOLTAGE versus INPUT VOLTAGE AND TEMPERATURE

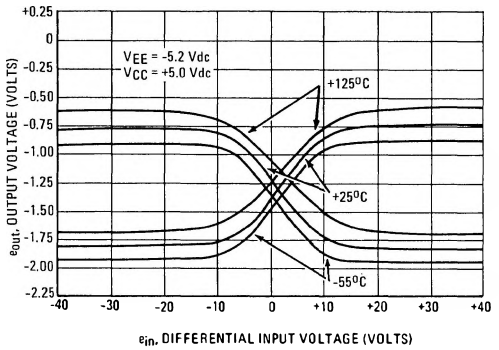


FIGURE 5 – OUTPUT VOLTAGE versus INPUT VOLTAGE AND SUPPLY VARIATION

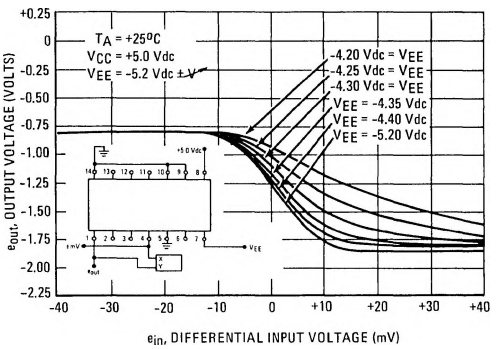


FIGURE 6 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

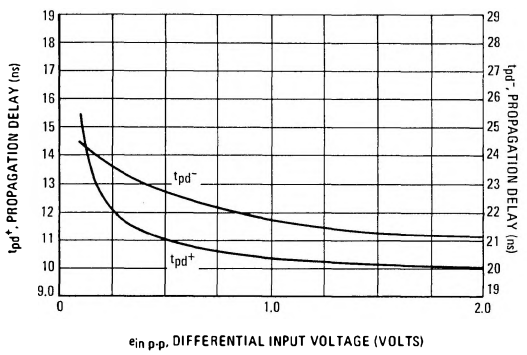


FIGURE 7 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

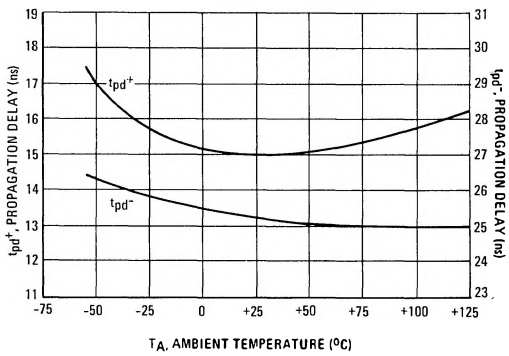
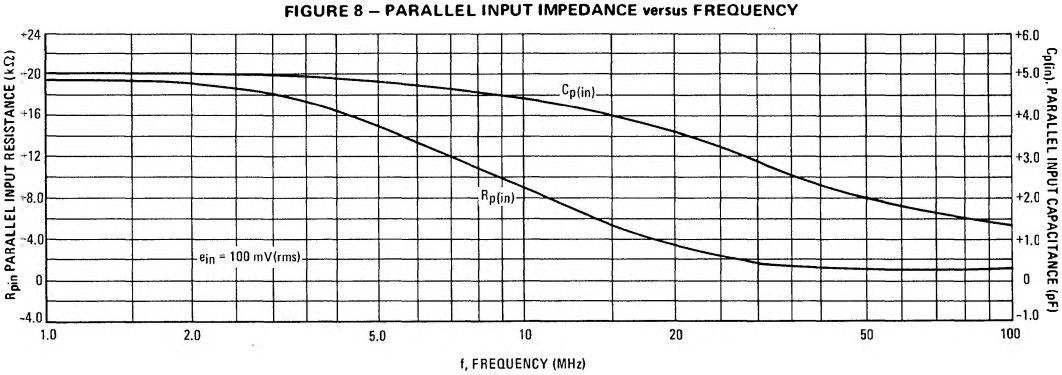


FIGURE 8 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines, e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability of operating in a party-line mode whereby a number of drivers can be connected to a single line. The series provides both drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

MC1580L	Dual Line Driver/Receiver
MC1581L	Dual MECL Receiver
MC1582L	Dual MDTL/MTTL Driver
MC1583L	Dual Receiver (Open Collector)
MC1584L	Dual Receiver (Active Pullup)

Figure 9 indicates the line drivers and receivers recommended for interfacing with each of the various digital logic families.

FIGURE 9

Digital Logic Family	Driver	Receiver
MECL	MC1580L	MC1581L
MDTL	MC1582L	MC1583L MC1584L
MTTL	MC1582L	MC1583L MC1584L
MRTL	MC1580L MC1582L	MC1583L

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in such applications as voltage comparators, waveform generators and high-input impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1581L in Figure 10 serves as the line receiver in a balanced differential transmission line. The outputs of the MC1581L receiver and the inputs to the MC1580L driver are compatible with MECL.

While common-mode noise is the major concern in a twisted pair transmission line, a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_O, calculate the minimum differential input voltage from the equation:

$$\pm V_{in} = \frac{I_{O(min)} \times Z_O}{4}$$

For a 170-ohm line, $V_{in} \frac{(6.9)\ (170)}{4} = 0.29$ Volts

Since the MC1581L requires a 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V, (see Figure 11).

FIGURE 11

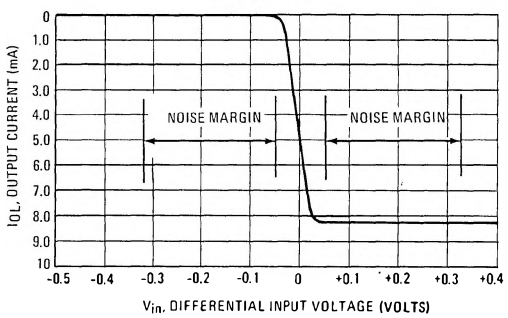
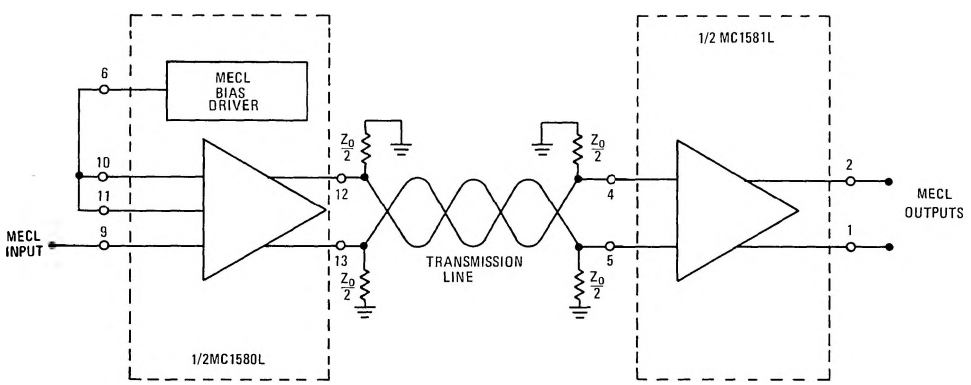


FIGURE 10 – MECL COMPATIBLE TRANSMISSION SYSTEM



The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5/–3.5 volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupled lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input impedance of the MC1581L and high output impedance of the MC1580L minimize impedance discontinuities on the

APPLICATIONS INFORMATION (continued)

transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1581L and the MC1580L in a bi-directional MECL compatible transmission system is shown in Figure 12. The MC1580L has an internal MECL bias network that allows the circuit to be used as a MECL line driver. The drivers of Figure 12 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S, supplies the current required by one driver. The current for the other driver is drawn from the termination impedances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts.

If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL}, and hence the maximum number of drivers that can be connected to a given transmission line.

Voltage Translator

Translation of voltage levels from MHTL (tailored for the noisy input/output system portions) to MECL (best suited for the high-speed logic circuits) is often required. The MC1581L performs this function as shown in Figure 13.

FIGURE 12 – BI-DIRECTIONAL TRANSMISSION

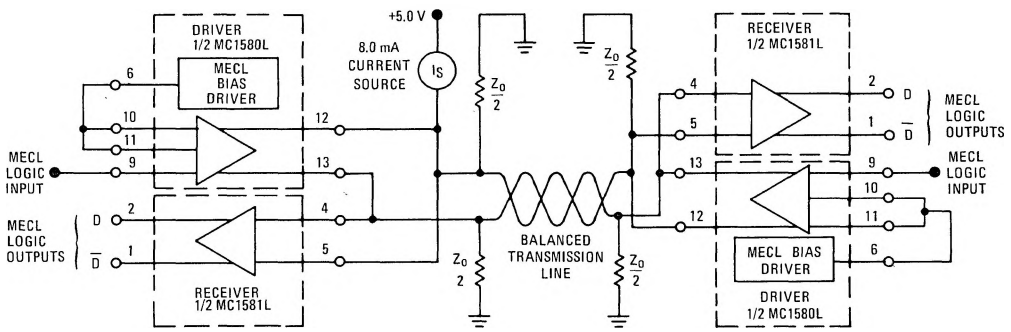


FIGURE 13 – MHTL-TO-MECL VOLTAGE LEVEL TRANSLATOR