MC1455, MC1455B

Timers

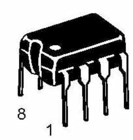
The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode, time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free–running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

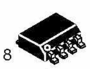
- Direct Replacement for NE555 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally ON or Normally OFF Output

TIMING CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

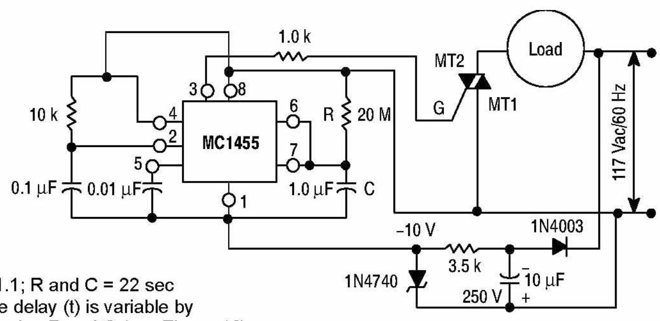




D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1455P1	T_A = 0° to +70°C	Plastic DIP
MC1455D		SO–8
MC1455BD	T_A = – 40° to +85°C	SO–8
MC1455BP1		Plastic DIP



t = 1.1; R and C = 22 sec
Time delay (t) is variable by changing R and C (see Figure 16).

Figure 1. 22 Second Solid State Time Delay Relay Circuit

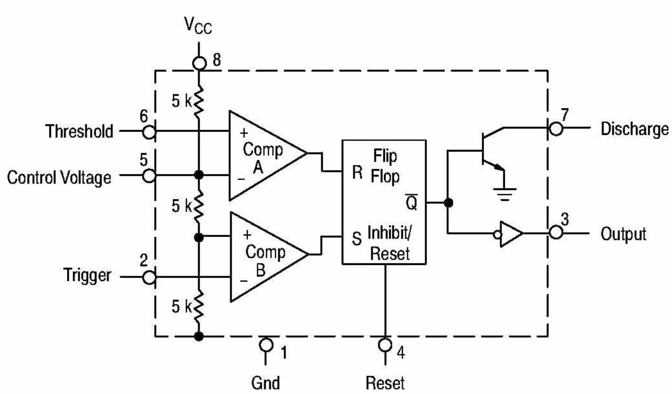
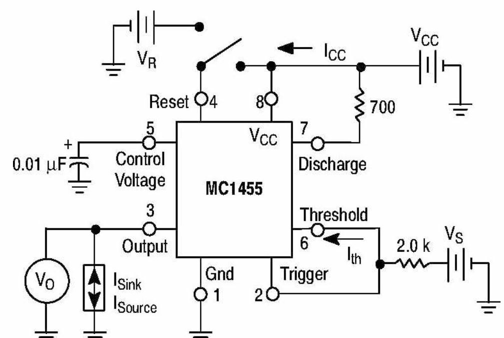


Figure 2. Representative Block Diagram



Test circuit for measuring DC parameters (to set output and measure parameters):
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, Pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V_{CC}.

Figure 3. General Test Circuit

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation) P1 Suffix, Plastic Package Derate above T_A = +25°C D Suffix, Plastic Package Derate above T_A = +25°C	 P_D P_D	 625 5.0 625 160	 mW mW/°C mW °C/W
Operating Temperature Range (Ambient) MC1455B MC1455	T_A	 –40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	4.5	–	16	V
Supply Current V_{CC} = 5.0 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞, Low State (Note 1)	I_{CC}	 – –	 3.0 10	 6.0 15	mA
Timing Error (R = 1.0 kΩ to 100 kΩ) (Note 2) Initial Accuracy C = 0.1 µF Drift with Temperature Drift with Supply Voltage		 – – –	 1.0 50 0.1	 – – –	 % PPM/°C %/V
Threshold Voltage/Supply Voltage	V_{th}/V_{CC}	–	2/3	–	
Trigger Voltage V_{CC} = 15 V V_{CC} = 5.0 V	V_T	 – –	 5.0 1.67	 – –	V
Trigger Current	I_T	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	µA
Discharge Leakage Current (Pin 7)	I_{dischg}	–	–	100	nA
Control Voltage Level V_{CC} = 15 V V_{CC} = 5.0 V	V_{CL}	 9.0 2.6	 10 3.33	 11 4.0	V
Output Voltage Low I_{Sink} = 10 mA (V_{CC} = 15 V) I_{Sink} = 50 mA (V_{CC} = 15 V) I_{Sink} = 100 mA (V_{CC} = 15 V) I_{Sink} = 200 mA (V_{CC} = 15 V) I_{Sink} = 8.0 mA (V_{CC} = 5.0 V) I_{Sink} = 5.0 mA (V_{CC} = 5.0 V)	V_{OL}	 – – – – – –	 0.1 0.4 2.0 2.5 – 0.25	 0.25 0.75 2.5 – – 0.35	V
Output Voltage High V_{CC} = 15 V (I_{Source} = 200 mA) V_{CC} = 15 V (I_{Source} = 100 mA) V_{CC} = 5.0 V (I_{Source} = 100 mA)	V_{OH}	 – 12.75 2.75	 12.5 13.3 3.3	 – – –	V
Rise Time Differential Output	t_r	–	100	–	ns
Fall Time Differential Output	t_f	–	100	–	ns

NOTES: 1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V Monostable mode.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 MΩ.

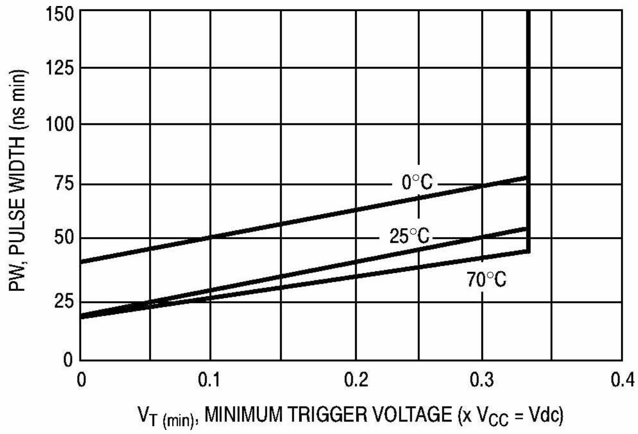


Figure 4. Trigger Pulse Width

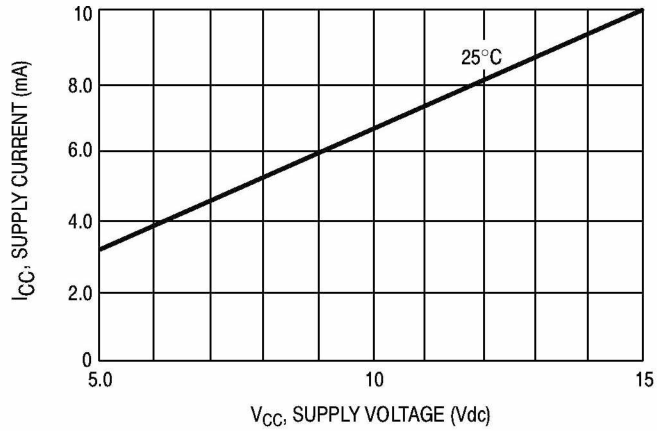


Figure 5. Supply Current

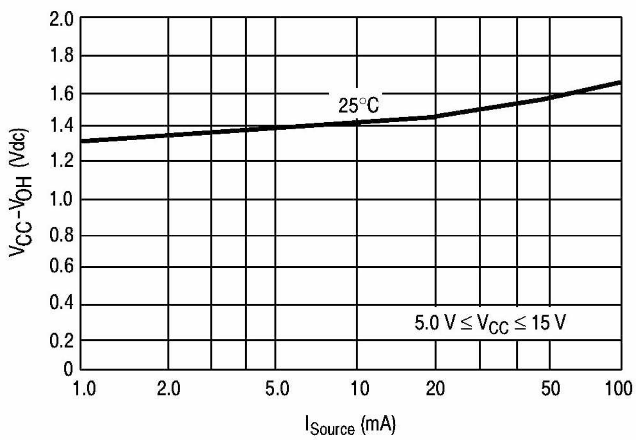


Figure 6. High Output Voltage

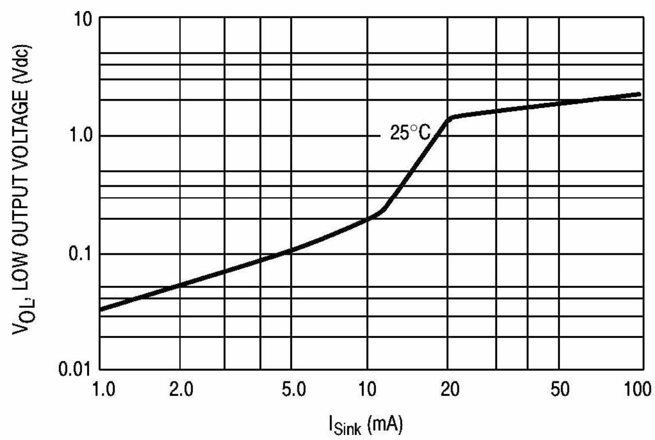


Figure 7. Low Output Voltage @ V_{CC} = 5.0 Vdc

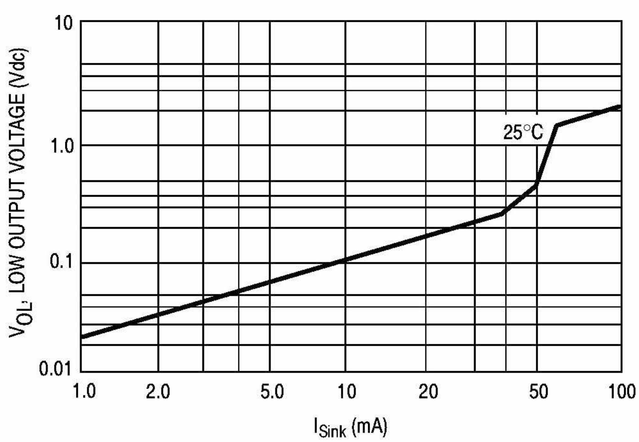


Figure 8. Low Output Voltage @ V_{CC} = 10 Vdc

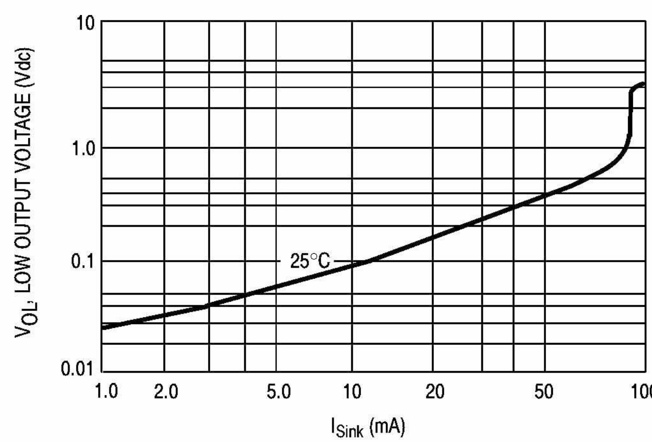


Figure 9. Low Output Voltage @ V_{CC} = 15 Vdc

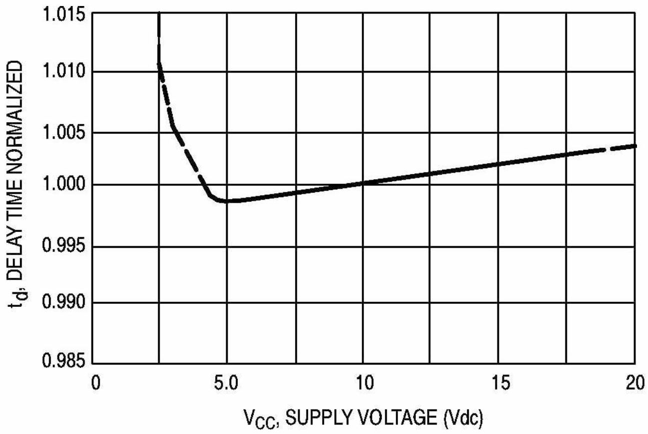


Figure 10. Delay Time versus Supply Voltage

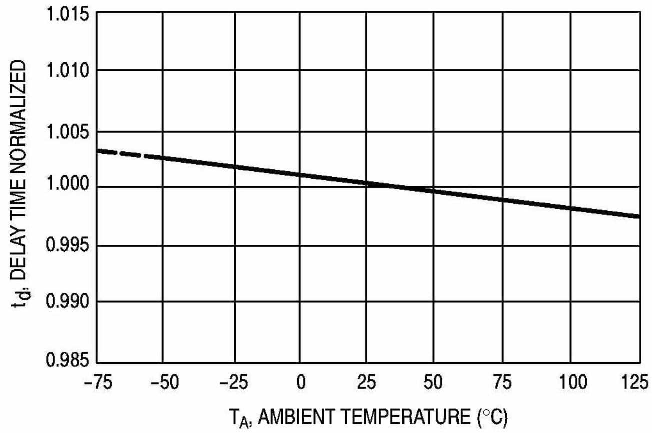


Figure 11. Delay Time versus Temperature

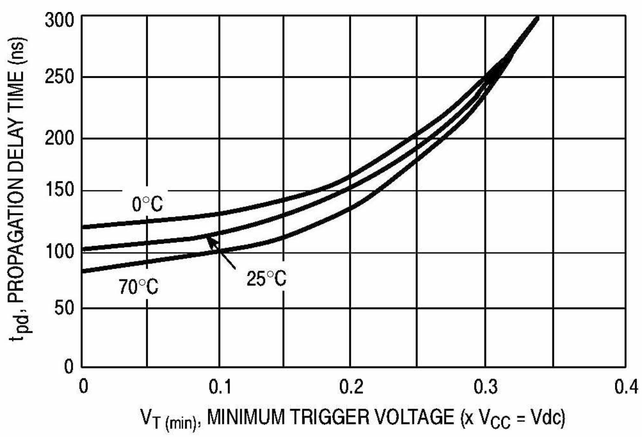


Figure 12. Propagation Delay versus Trigger Voltage

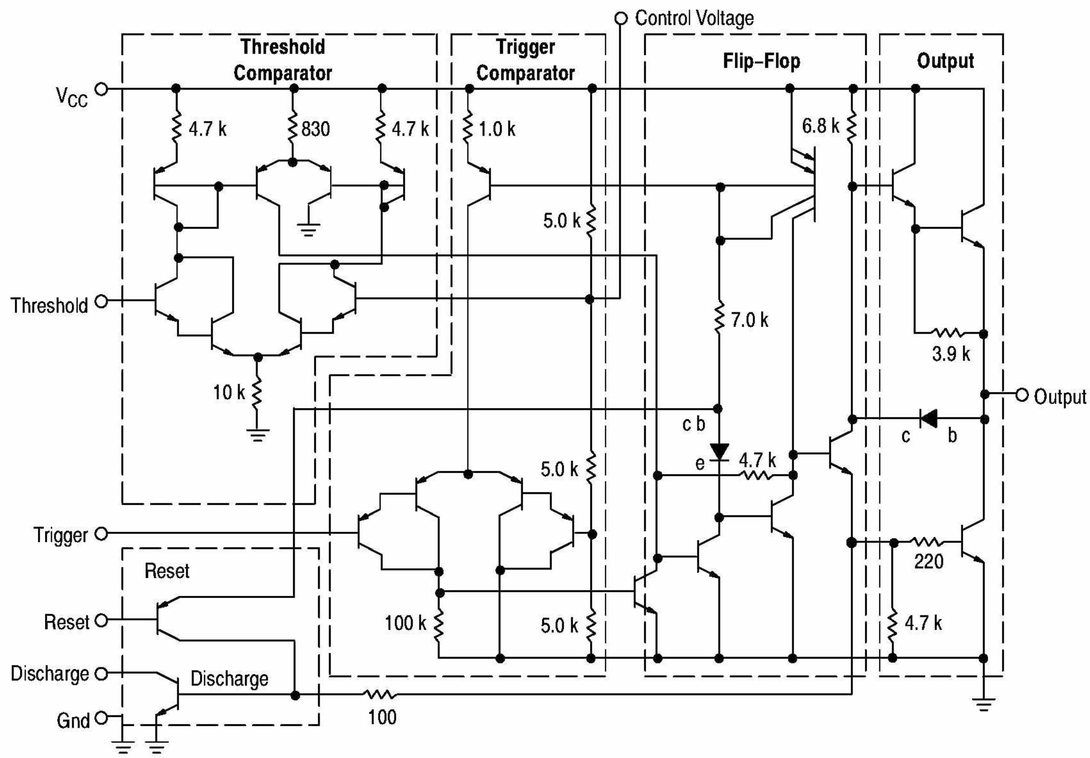


Figure 13. Representative Circuit Schematic

GENERAL OPERATION

The MC1455 is a monolithic timing circuit which uses an external resistor – capacitor network as its timing element. It can be used in both the monostable (one–shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip–flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode (refer to circuit in Figure 14). When the input voltage to the trigger comparator falls below 1/3 V_{CC}, the comparator output triggers the flip–flop so that its output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC}, the threshold comparator resets the flip–flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip–flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor, thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

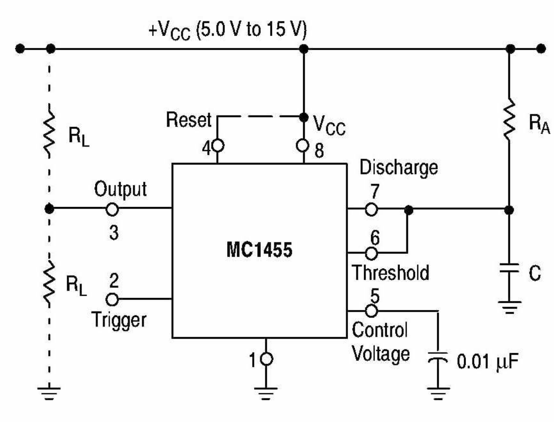
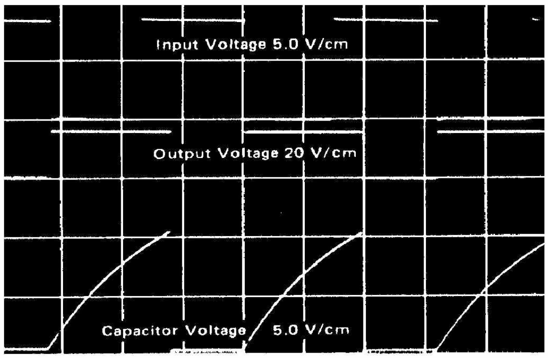


Figure 14. Monostable Circuit



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

Figure 15. Monostable Waveforms

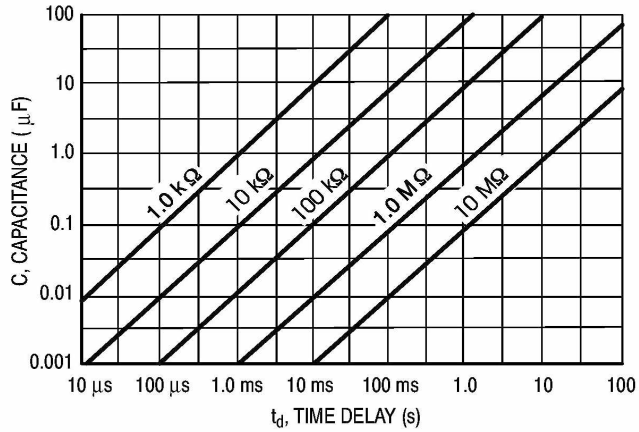


Figure 16. Time Delay

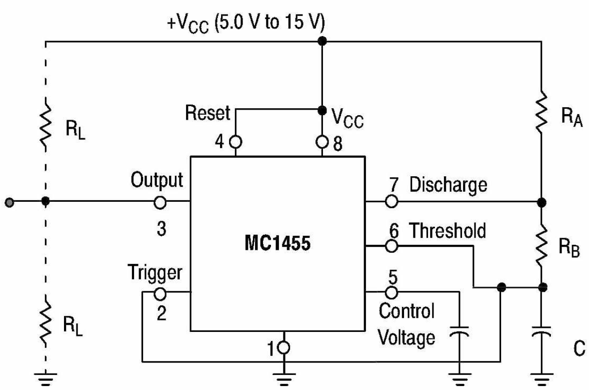
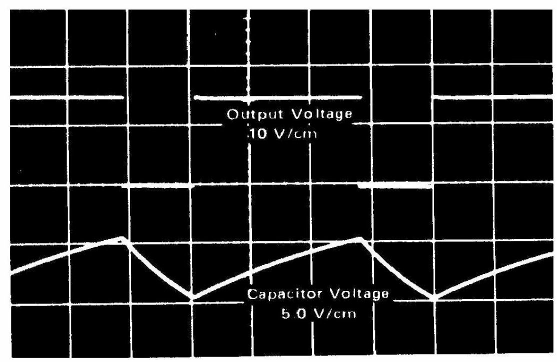


Figure 17. Astable Circuit



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ; R_B = 3.9 kΩ, V_{CC} = 15 V)

Figure 18. Astable Waveforms

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor changes to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.695\ (R_A + R_B)\ C$$

The discharge time (output low) is given by:

$$t_2 = 0.695\ (R_B)\ C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (Vdc)}{I7\ (A)} \geq \frac{V_{CC}\ (Vdc)}{0.2}$$

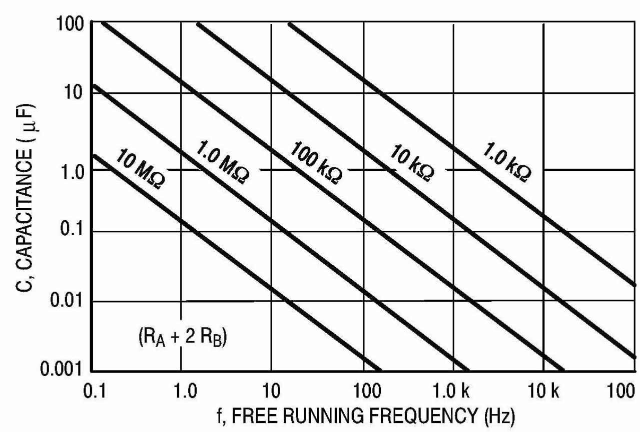


Figure 19. Free Running Frequency

APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 V_{CC} to 2/3 V_{CC}. The linear ramp time is given by:

$$t = \frac{2}{3}\frac{V_{CC}}{1}, \quad \text{where } I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$$

If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

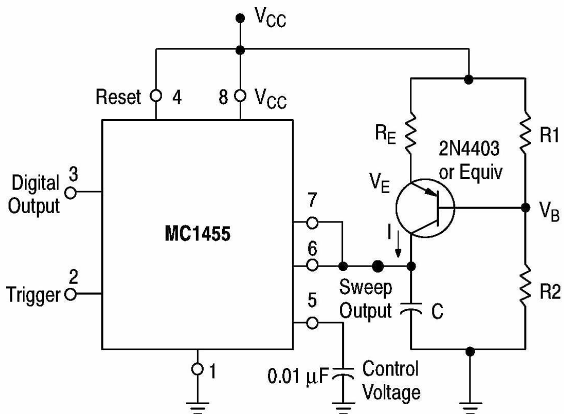


Figure 20. Linear Voltage Sweep Circuit

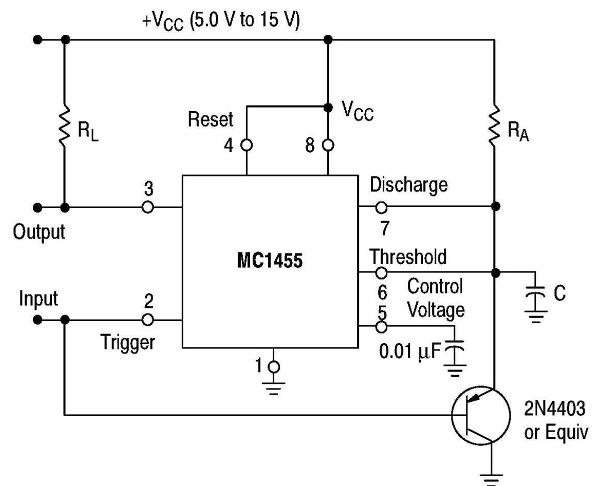
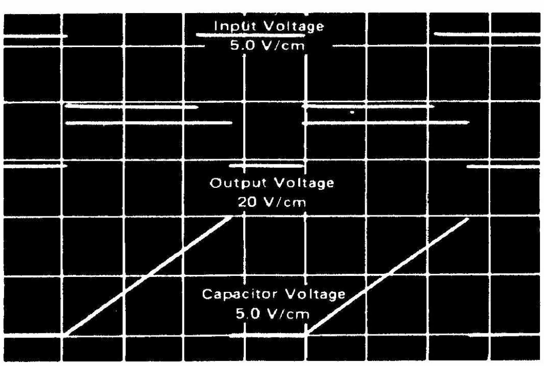


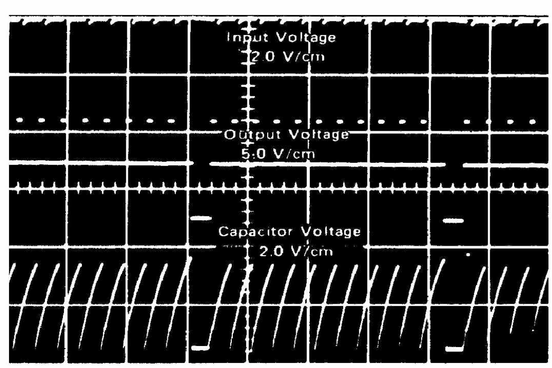
Figure 21. Missing Pulse Detector



t = 100 µs/cm

(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Figure 22. Linear Voltage Ramp Waveforms



t = 500 µs/cm

(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Figure 23. Missing Pulse Detector Waveforms

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monstable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

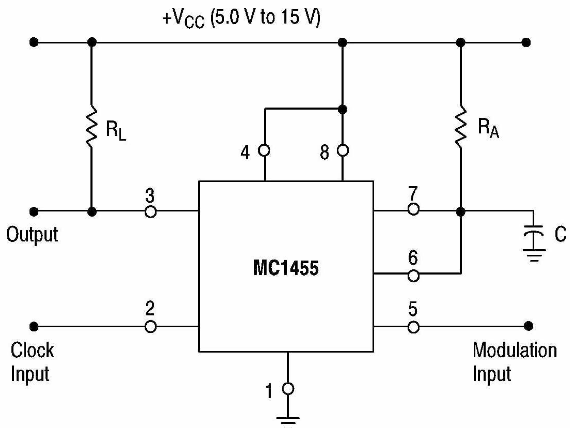
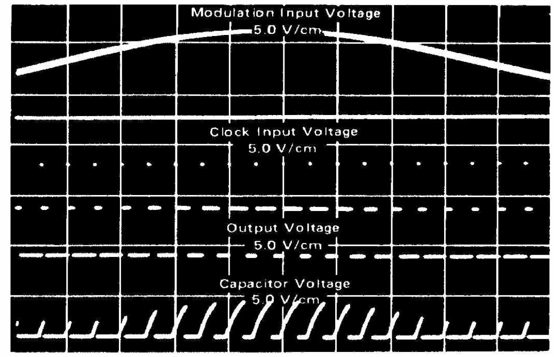


Figure 24. Pulse Width Modulator



t = 0.5 ms/cm
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)

Figure 25. Pulse Width Modulation Waveforms

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

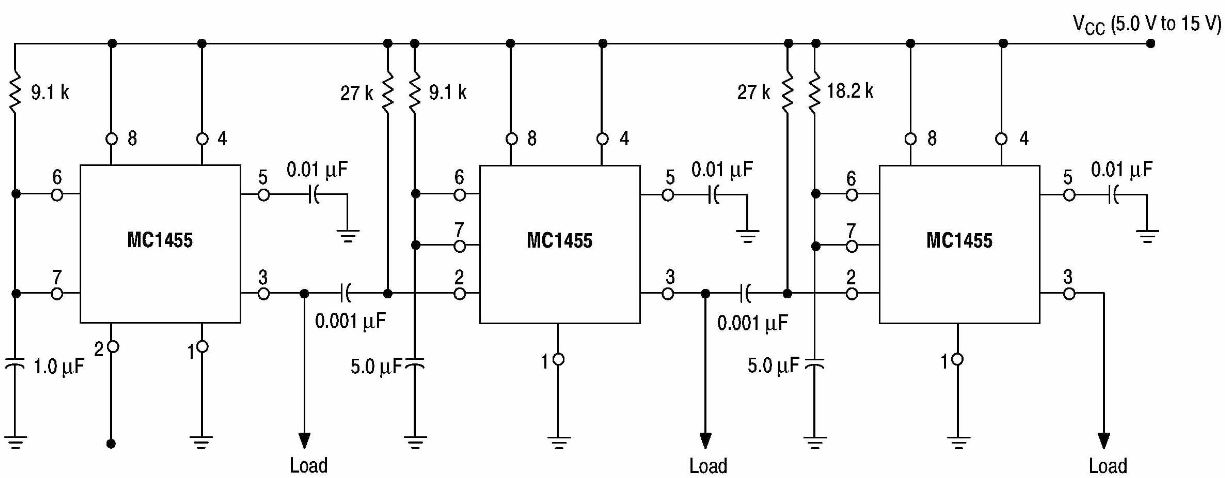


Figure 26. Sequential Timer