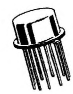
MC1439G

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



Lead 4 connected to case

CASE 96
(TO-99)
"G" SUFFIX

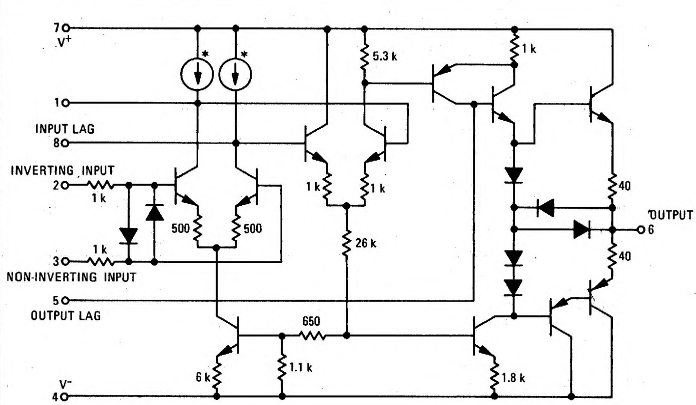
Typical Amplifier Features:

- Low Input Offset Voltage — 2.0 mV typ
- Low Input Offset Current — 100 nA max
- Large Power-Bandwidth — 20 $V_{p\text{-}p}$ Output Swing at 10 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate — 34 V/μs typ

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

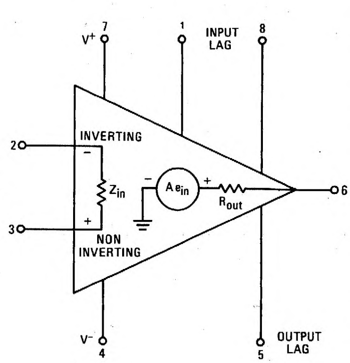
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm V^+$	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Derate above 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



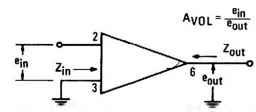
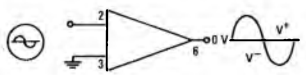
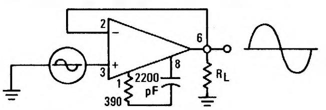
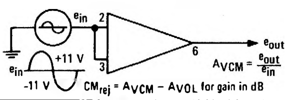
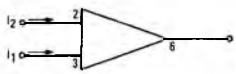
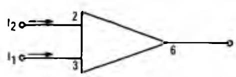
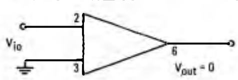
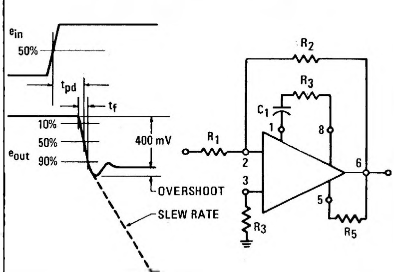
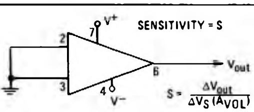
*PATENT PENDING

EQUIVALENT CIRCUIT



MC1439G (continued)

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L = 2.0 kΩ, V_{out} = ±10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	100,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	4.0	-	kΩ
	Input Impedance (f = 20 Hz)	Z_{in}	100	300	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2.0 kΩ)	V_{out}	 ±12 ±10	 ±14 ±13	 - -	V_{peak}
	Power Bandwidth (A_v = 1, R_L = 2.0 kΩ, THD ≦ 5%, V_o = 20 V_{p-p})	P_{BW}	10	50	-	kHz
	Input Common Mode Voltage Swing	CMV_{in}	±11	±12	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	80	100	-	dB
	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	 - -	 0.20 0.23	 1.0 1.5	µA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	 - - -	 20 - -	 100 150 150	nA
	Input Offset Voltage (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	 - -	 2.0 -	 7.5 10	mV
	Step Response Gain = 100, no overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ, R_4 = 10 kΩ, R_5 = 10 kΩ,* C_1 = 2200 pF Gain = 100, no overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ, R_4 = 10 kΩ, R_5 = ∞,* C_1 = 2200 pF Gain = 10, 15% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ, R_4 = 1.0 kΩ, R_5 = 10 kΩ,* C_1 = 2200 pF Gain = 10, 15% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ, R_4 = 1.0 kΩ, R_5 = ∞,* C_1 = 2200 pF Gain = 1, 15% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ, R_4 = 390 Ω, R_5 = 10 kΩ,* C_1 = 2200 pF Gain = 1, 15% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ, R_4 = 390 Ω, R_5 = ∞,* C_1 = 2200 pF	t_f / t_{pd} / dV_{out}/dt‡ t_f / t_{pd} / dV_{out}/dt‡ t_f / t_{pd} / dV_{out}/dt‡ t_f / t_{pd} / dV_{out}/dt‡ t_f / t_{pd} / dV_{out}/dt‡ t_f / t_{pd} / dV_{out}/dt‡	- / - / - - / - / - - / - / - - / - / - - / - / - - / - / -	700 / 100 / 34 700 / 100 / 1.7 600 / 80 / 6.25 600 / 80 / 1.7 400 / 80 / 4.2 400 / 80 / 1.4	- / - / - - / - / - - / - / - - / - / - - / - / - - / - / -	ns / ns / V/µs ns / ns / V/µs ns / ns / V/µs ns / ns / V/µs ns / ns / V/µs ns / ns / V/µs
	Equivalent Input Noise Voltage (Open Loop) (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	-	30	-	$nV/(Hz)^{1/2}$
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50Ω, T_A = 0°C to +75°C) (R_S ≦ 10 kΩ, T_A = 0°C to +75°C)	TC_{Vio}	 - -	 3.0 5.0	 - -	µV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	90	200	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	200	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	50	200	µV/V

*To improve performance, development is in process to include resistor R_5 ≈ 10 kΩ on the device chip. Available after September 1968.
‡dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

(V^{+} = +15 Vdc, V^{-} = -15 Vdc, T_A = 25°C)

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 1)					
			$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	$R_4(\Omega)$	R_5*(Ω)	C_1(pF)
2	1	1.0	10 k	10 k	5.0 k	390	10 k	2200
	2	1.0	10 k	10 k	5.0 k	390	∞	2200
3	1	A_{VOL}	0	∞	0	∞	∞	0
	2	1000	1000	1.0 M	1000	0	∞	10
	3	100	1000	100 k	1000	10 k	∞	2200
	4	10	1000	10 k	1000	1.0 k	∞	2200
	5	1.0	10 k	10 k	5.0 k	390	∞	2200
4	1	A_{VOL}	0	∞	0	∞	∞	0
	2	A_{VOL}	0	∞	0	10 k	∞	2200
	3	A_{VOL}	0	∞	0	390	∞	2200

*To improve performance, development is in process to include resistor $R_5 \approx 10\ k\Omega$ on the device chip. Available after September 1968.

FIGURE 1 – TEST CIRCUIT

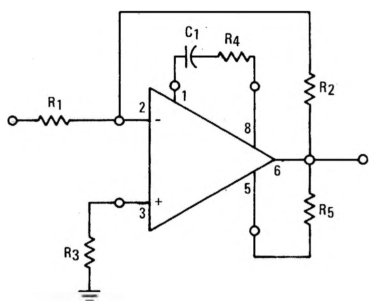


FIGURE 2 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

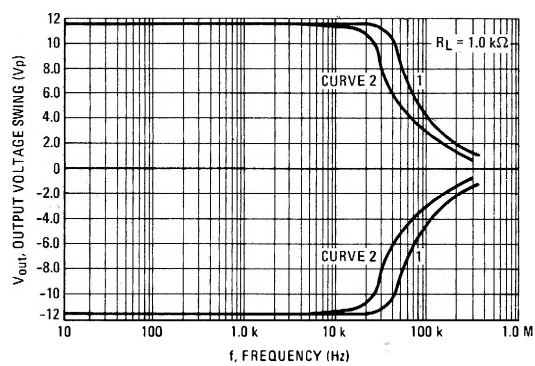


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

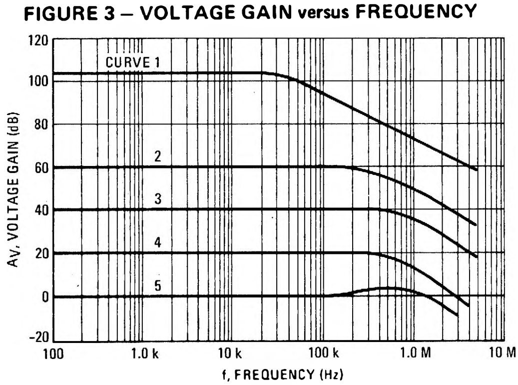


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

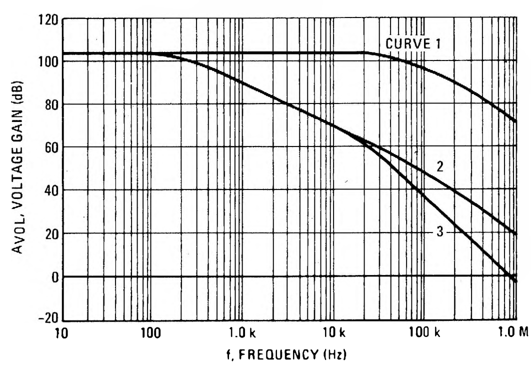


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

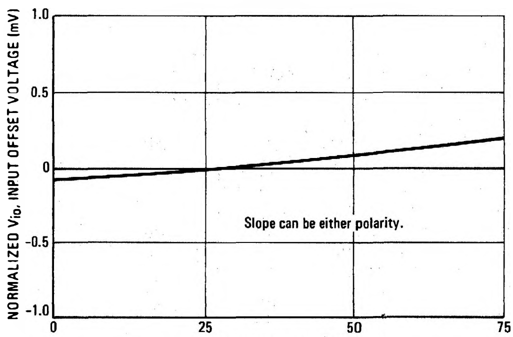


FIGURE 6 – INPUT OFFSET CURRENT versus TEMPERATURE

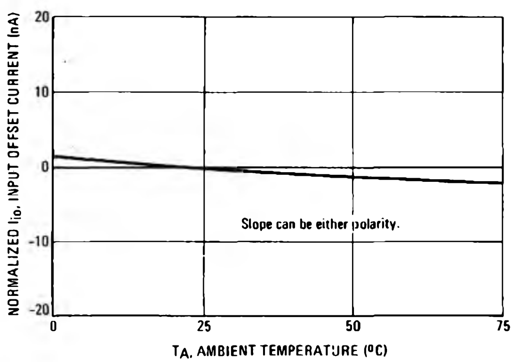


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

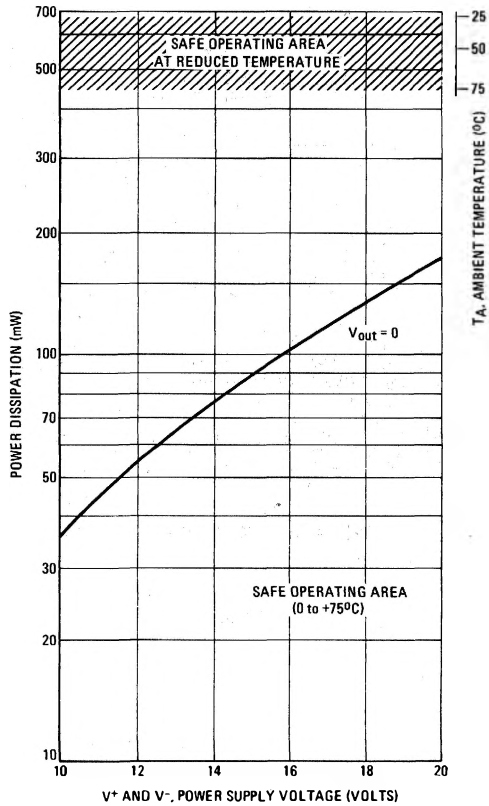


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

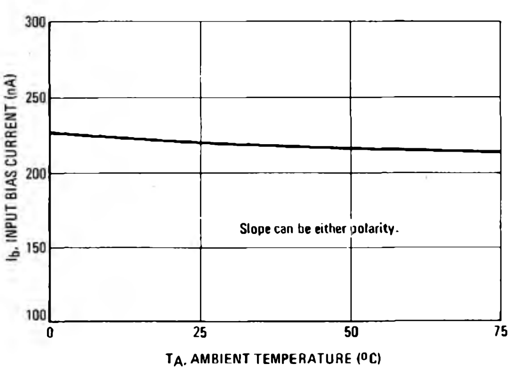


FIGURE 9 – SPECTRAL NOISE DENSITY