19-0382; Rev 1; 8/95

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

General Description

The MAX624 is a dual DC-DC converter intended for size-constrained applications, such as power supplies that must fit inside PCMCIA memory cards. At the heart of the MAX624 are two boost-topology converters, plus auxiliary functions including a start-up inrush surge-current limiter and a power-on reset output with timer (power-good signal). The MAX624 accepts input voltages from 3V to 5.5V and generates two outputs: a fixed 5V ±4% output at 200mA (guaranteed), and an adjustable auxiliary output that is configurable for various loads with an external power transistor. The auxiliary output is typically set to 12V ±2% for flash memory applications, but can be adjusted via a resistor divider from V_{IN} to 30V or more.

The MAX624's high switching frequency (1MHz) reduces external component sizes. High-frequency switching losses have minimal impact on efficiency, which is 85% for the main 5V supply. Small ceramic filter capacitors, together with the soft-start function, reduce start-up inrush current surges.

Applications

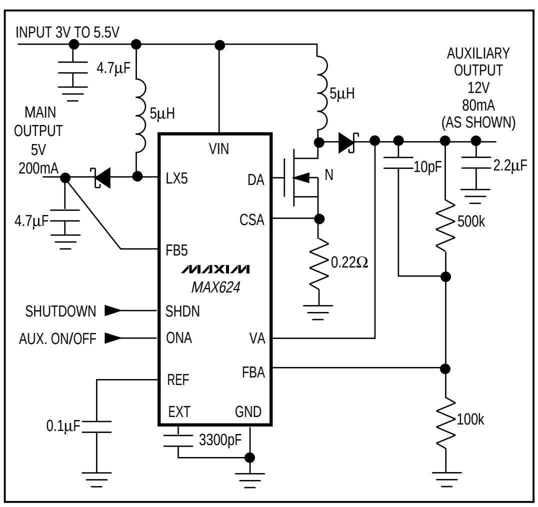
PCMCIA Memory Cards

Solid-State Disk Drives

Host-Side PCMCIA Adapters

LCD Bias Power Supplies

Typical Operating Circuit



Features

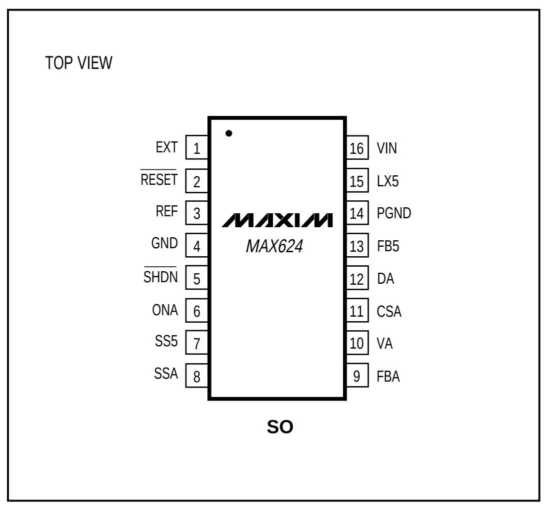
- **1MHz Switching Frequency for Small Components**
- **5V ±4% Boost Converter with Internal Power Switch**
- **Adjustable ±2% Output Boost Converter with External Power Switch**
- **Optional Inrush Surge-Current Limiting**
- **40µA Shutdown Current**
- **0.5mA Quiescent Current**
- **3.0V to 5.5V Input Range**
- **85% Main 5V SMPS Efficiency**
- **Independent Soft-Start for Each Supply**
- **Reset Output with 2.8V ±3% Threshold and 4ms Timeout**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX624C/D	0°C to +70°C	Dice*
MAX624ISE	-25°C to +85°C	16 Narrow SO

** Dice are tested at T_A = +25°C. Contact factory for dice specifications.*

Pin Configuration



Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

ABSOLUTE MAXIMUM RATINGS

VIN, FB5, LX5, $\overline{SHDN}$, ONA to GND ....-0.3V to 7V
EXT to GND ....-0.3V to 12V
RESET, REF to GND ....-0.3V to (VIN + 0.3V)
PGND to GND ....±0.3V
SS5, SSA, DA, CSA, FBA to GND ....-0.3V to (FB5 + 0.3V)
VA to GND ....-0.3V to 17V

Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range
MAX624ISE ....-25°C to +85°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, GND = PGND = 0V, $\overline{SHDN}$ = V_{IN}, EXT open, FBA feedback resistors set for 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range		3.0		5.5	V
OUTPUT VOLTAGES					
5V Output Voltage		4.80		5.20	V
FBA Regulation Point		1.96		2.04	V
SUPPLY CURRENTS					
V_{IN} Shutdown Current	V_{IN} = 5.5V, $\overline{SHDN}$ = ONA = 0V		40	60	µA
V_{IN} Quiescent Current	Circuit of Figure 1, V_{IN} = 3.3V, ONA = 0V		500		µA
FB5 Quiescent Current	FB5 = 5.5V, $\overline{SHDN}$ = 3V, ONA = 0V		200	400	µA
VA Quiescent Current	FB5 = 5.5V, VA = 12.5V		30	60	µA
FB5 Shutdown Discharge Current	FB5 = 5V, V_{IN} = 3V, $\overline{SHDN}$ = 0V, internal V_{IN} to FB5 discharge switch	100	5000		µA
VA Shutdown Discharge Current	VA = 12V, V_{IN} = 3V, ONA = 0V, internal V_{IN} to VA discharge switch	5	15		µA
FBA Leakage Current	VA = 12V, FBA = 2.1V			100	nA
5V MAIN SMPS					
Line Regulation	3V < V_{IN} < 5.5V (Note 1)		0.03	0.2	%
Switch On-Resistance			0.33	0.6	Ω
Switch Leakage Current	LX5 = 7V			10	µA
Switch Current Limit		0.7	0.9	1.1	A
Switch On-Time Constant (K5)	3V < V_{IN} < 5V, t_{ON5} = K5 / V_{IN}	0.8	1.3	1.7	µs-V
Switch Off-Time Ratio (SR5)	3V < V_{IN} < 5V, FB5 = 5V (Note 2)	0.2		0.8	
Efficiency	Circuit of Figure 1, I_{LOAD} = 100mA		85		%
AUXILIARY SMPS CONTROLLER					
Line Regulation	3V < V_{IN} < 5.5V (Note 1)		0.03	0.2	%
Enable Trip Voltage Level	ONA input will be inhibited until FB5 rises above this level	3.5	4.0	4.5	V
CSA Bias Current				10	µA
CSA Current-Limit Threshold		180		220	mV
DA On-Resistance	FB5 = 5.5V		4	15	Ω
DA Drive Current	DA = 2.5V		0.5		A
Switch On-Time Constant (KA)	3V < V_{IN} < 5V, t_{ONA} = KA / V_{IN}	1.5	2.2	3.0	µs-V
Switch Off-Time Ratio (SRA)	3V < V_{IN} < 5V, 7V < FBA < 11V (Note 3)	0.2		0.9	
Efficiency	Circuit of Figure 1, I_{LOAD} = 60mA		75		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, GND = PGND = 0V, $\overline{SHDN}$ = V_{IN}, EXT open, FBA feedback resistors set for 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START CONTROL					
Source Resistance	SS5, SSA; $\overline{SHDN}$ = ONA = 3V	14	20	28	kΩ
Discharge Resistance	SS5, SSA; $\overline{SHDN}$ = ONA = 0V		50	300	Ω
LOGIC INPUTS AND OUTPUTS					
Input Low Voltage	$\overline{SHDN}$, ONA			0.8	V
Input High Voltage	$\overline{SHDN}$, ONA	2			V
Input Leakage	$\overline{SHDN}$, ONA			±1	µA
Output Low Voltage	$\overline{RESET}$, I_{SINK} = 2mA, V_{IN} = 2.6V			0.4	V
Output High Voltage	$\overline{RESET}$, I_{SINK} = 1mA, V_{IN} = 3V	V_{IN} - 0.8			V
$\overline{RESET}$ Trip Level	Rising V_{IN} edge, typical hysteresis = 1%	2.7		2.9	V
$\overline{RESET}$ Timeout		2		10	ms
EXT Output Voltage	V_{IN} = 2.9V, I_{SOURCE} = 2µA	6.5			V
	V_{IN} = 5.5V, I_{SOURCE} = 0µA			11.8	
EXT Output Voltage in Reset	V_{IN} = 2V, I_{SINK} = 0.1mA			1	V

Note 1: Line Regulation is tested by measuring the reference line regulation, since both converters are supplied from the regulated 5V output.

Note 2: Switch off-time ratio guarantees that the inductor will go into continuous conduction. The ratio is tested for two cases for the main SMPS:
1) V_{IN} = 5V, FB5 = 5V   SR5 = 0.120 x t_{OFF} / t_{ON}
2) V_{IN} = 3V, FB5 = 5V   SR5 = 0.867 x t_{OFF} / t_{ON}
Note that the constants are calculated from: (FB5 + 0.6V - V_{IN}) / V_{IN}

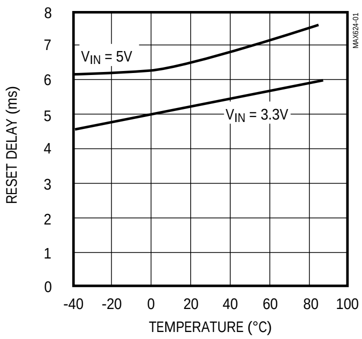
Note 3: Switch off-time ratio guarantees that the inductor will go into continuous conduction. The ratio is tested for two cases for the auxiliary SMPS:
1) V_{IN} = 5V, VA = 7V   SRA = 0.520 x t_{OFF} / t_{ON}
2) V_{IN} = 3V, VA = 11V   SRA = 2.867 x t_{OFF} / t_{ON}
Note that the constants are calculated from: (VA + 0.6V - V_{IN}) / V_{IN}

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

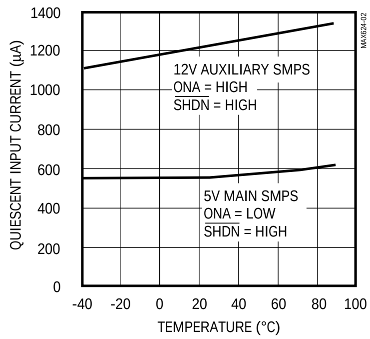
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

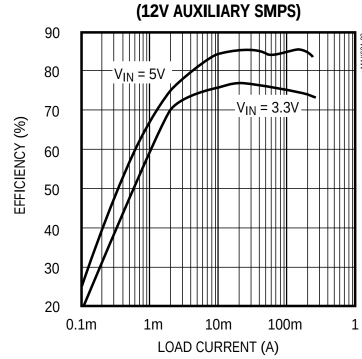
RESET DELAY vs. TEMPERATURE



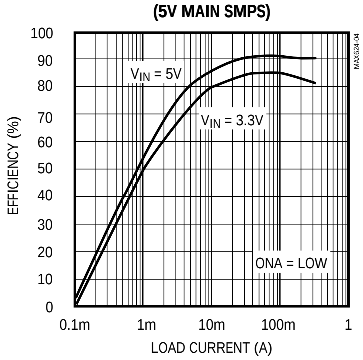
QUIESCENT INPUT CURRENT vs. TEMPERATURE



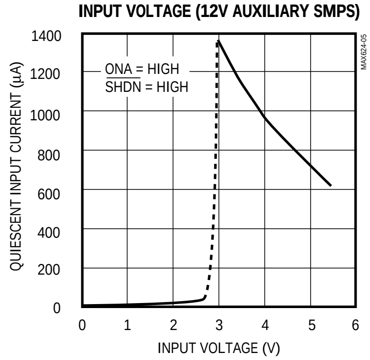
EFFICIENCY vs. LOAD CURRENT (12V AUXILIARY SMPS)



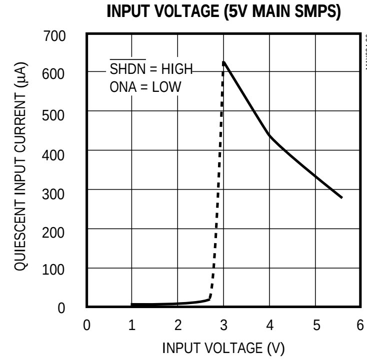
EFFICIENCY vs. LOAD CURRENT (5V MAIN SMPS)



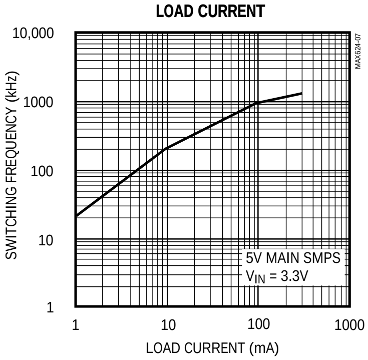
QUIESCENT INPUT CURRENT vs. INPUT VOLTAGE (12V AUXILIARY SMPS)



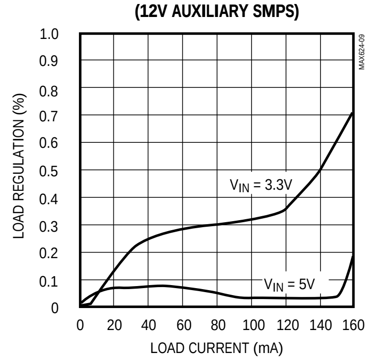
QUIESCENT INPUT CURRENT vs. INPUT VOLTAGE (5V MAIN SMPS)



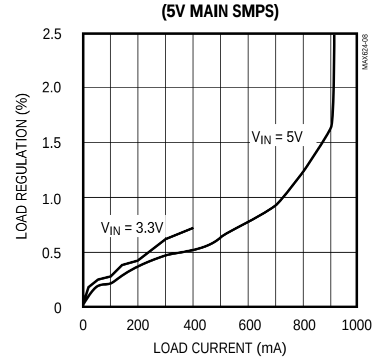
SWITCHING FREQUENCY vs. LOAD CURRENT



LOAD REGULATION vs. LOAD CURRENT (12V AUXILIARY SMPS)



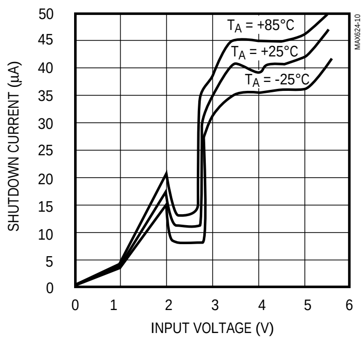
LOAD REGULATION vs. LOAD CURRENT (5V MAIN SMPS)



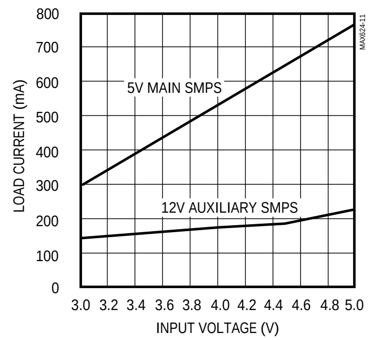
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

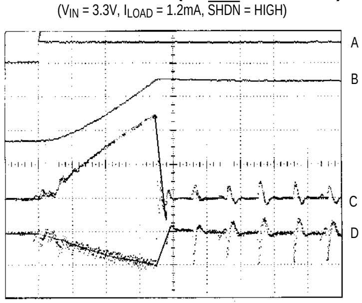
SHUTDOWN CURRENT vs. INPUT VOLTAGE



LOAD CURRENT CAPABILITY vs. INPUT VOLTAGE



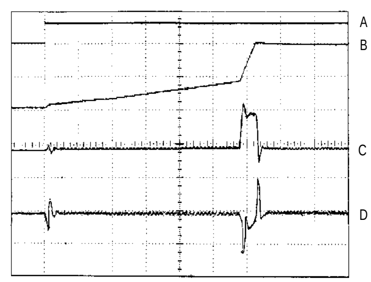
START-UP WAVEFORMS (12V AUXILIARY SMPS)
(V_{IN} = 3.3V, I_{LOAD} = 1.2mA, $\overline{SHDN}$ = HIGH)



100µs/div

A: ONA (5V/div)
B: 12V AUXILIARY SMPS (5V/div)
C: I_{IN} (200mA/div)
D: $V_{SWITCHED}$ (100mV/div, AC-COUPLED)

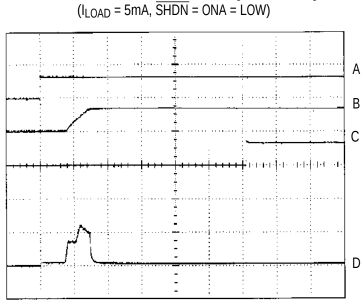
START-UP WAVEFORMS (5V MAIN SMPS)
(V_{IN} = 3.3V, I_{LOAD} = 0A, ONA = LOW)



100µs/div

A: $\overline{SHDN}$ (5V/div)
B: 5V MAIN SMPS (1V/div)
C: I_{IN} (200mA/div)
D: $V_{SWITCHED}$ (100mV/div, AC-COUPLED)

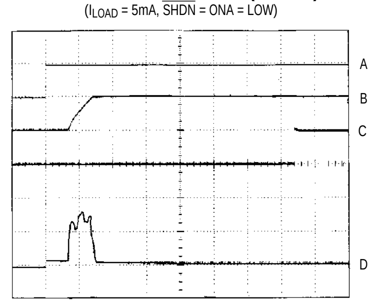
START-UP INRUSH CURRENT (V_{IN} = 3.3V)
(I_{LOAD} = 5mA, $\overline{SHDN}$ = ONA = LOW)



1ms/div

A: V_{IN} (5V/div)
B: $V_{SWITCHED}$ (5V/div)
C: $\overline{RESET}$ (5V/div)
D: I_{IN} (50mA/div)

START-UP INRUSH CURRENT (V_{IN} = 5V)
(I_{LOAD} = 5mA, $\overline{SHDN}$ = ONA = LOW)



1ms/div

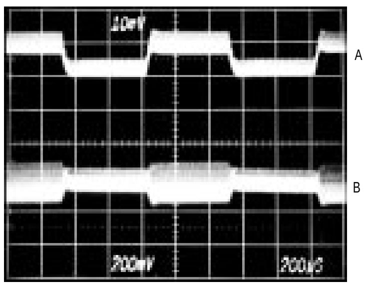
A: V_{IN} (5V/div)
B: $V_{SWITCHED}$ (5V/div)
C: $\overline{RESET}$ (5V/div)
D: I_{IN} (50mA/div)

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Typical Operating Characteristics (continued)

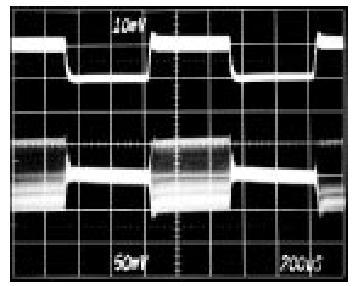
(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (12V AUXILIARY SMPS)



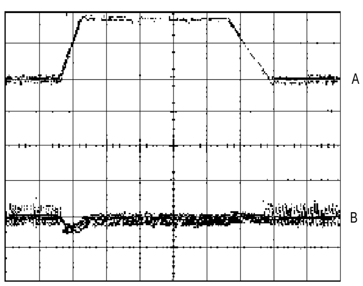
200µs/div
A: I_{LOAD} = 0mA to 80mA
B: 12V AUXILIARY SMPS (200mV/div, AC-COUPLED)

LOAD-TRANSIENT RESPONSE (5V MAIN SMPS)



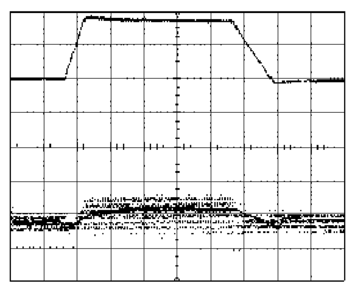
200µs/div
A: I_{LOAD} = 0mA to 200mA
B: 5V MAIN SMPS (50mV/div, AC-COUPLED)

LINE-TRANSIENT RESPONSE (12V AUXILIARY SMPS)



100µs/div
I_{LOAD} = 20mA
A: V_{IN} = 3.3V to 5V
B: 12V AUXILIARY OUTPUT (200mV/div, AC-COUPLED)

LINE-TRANSIENT RESPONSE (5V MAIN SMPS)



100µs/div
I_{LOAD} = 40mA
A: V_{IN} = 3.3V to 5V
B: 5V MAIN OUTPUT (50mV/div, AC-COUPLED)

Pin Description

PIN	NAME	FUNCTION
1	EXT	Gate-Drive Output. Drives inrush surge-current limiting MOSFET. EXT is fed by an internal charge-pump tripler that swings from GND to V_{IN} x 3.
2	$\overline{RESET}$	Power-On Reset Output. Low when V_{IN} < 2.8V and for 4ms after V_{IN} > 2.8V. EXT is low when $\overline{RESET}$ is low. Swings from GND to V_{IN}.
3	REF	2V Reference Output. Bypass to GND with 0.1µF. No external load current is allowed.
4	GND	Quiet Analog Ground and Low-Side Current-Sense Input for Auxiliary SMPS
5	$\overline{SHDN}$	Shutdown. Disables both SMPSs when low. In shutdown, the surge-protection input MOSFET is kept on.
6	ONA	On/Off Control Input for Auxiliary SMPS, low = off
7	SS5	Soft-Start Input for 5V Main SMPS. An external soft-start capacitor varies the 5V start-up time. Ramp time to full current limit is approximately 50µs per nF of soft-start capacitance.
8	SSA	Soft-Start Input for Auxiliary SMPS. An external soft-start capacitor varies the auxiliary SMPS start-up time. Ramp time to full current limit is approximately 50µs per nF of soft-start capacitance.
9	FBA	Feedback Input for Auxiliary SMPS. Regulates around REF (2V nominal). FBA is a high-impedance CMOS input.
10	VA	Output Voltage Sense Input for Auxiliary SMPS. The only purpose of this pin is to set the SMPS timing algorithm. Internally, VA connects to the top of a 250kΩ ±30% resistor that connects to V_{IN}.
11	CSA	Current-Sense Input for Auxiliary SMPS. Current-limit threshold is 200mV nominal with respect to GND.
12	DA	Gate-Drive Output for Auxiliary SMPS. Swings 0V to FB5.
13	FB5	Feedback Input for 5V Main SMPS. FB5 also serves as the supply voltage rail for much of the internal circuitry for both SMPSs (bootstrap supply input).
14	PGND	Power Ground, source connection for the main 5V SMPS power MOSFET
15	LX5	Drain Connection for 5V Main SMPS Power MOSFET
16	VIN	Input Supply Voltage from the External Supply. Normal operating range is 3V to 5.5V.

Standard Application Circuit

In the standard application circuit (Figure 1), the MAX624 generates 5V at 200mA (guaranteed) and 12V at 80mA from a 3.3V or 5V input, and includes soft-start and inrush surge-current limiting features. Successful use of the circuit does not require calculations; use the values given in Figure 1. For more detailed applications information, see the *Design Procedure for Main and Auxiliary SMPS.*

Detailed Description

The MAX624 is a dual-output DC-DC boost converter. The device accepts input voltages from 3V to 5.5V and generates two outputs: a 5V output at 200mA, and an adjustable output (i.e. 12V or 30V). The main 5V output has an internal MOSFET switch and current-sense resistor (0.15Ω), which senses the output current and triggers the current-limit comparator. The auxiliary SMPS's current-limit resistor and MOSFET switch are external to the device. The current-limit voltage of the auxiliary SMPS is 200mV. Both the main and auxiliary SMPS have a soft-start feature that varies the start-up time of the outputs. The SS output source impedance of the two outputs is 20kΩ to charge the external SS capacitor to 150mV (5V output) or 200mV (auxiliary output). The impedance of the SS pin when the device is in reset (5V) and when ONA = low (auxiliary) is 50Ω to GND. Full current limit is reached at a 50µs/nF rate.

To prevent surge currents when the card is plugged into a live socket, this device is capable of driving an external high-side N-channel MOSFET in series with the main V_{CC} supply to the card. The EXT pin drives the gate of the external MOSFET and is fed by an internal charge-pump tripler that delivers three-times V_{IN}, even in shutdown mode. The output source impedance of EXT is approximately 100kΩ, and has an active pull-down.

The SS capacitor and the external inrush-limiting MOSFET are optional components, not necessary unless inrush current is a concern. However, do not remove C9.

When the MAX624 is in reset, the FB5 and VA outputs are discharged to V_{IN} via two internal switches (Figure 2). Discharging the output capacitors to a low voltage level protects against false programming of flash memory chips.

5V Main SMPS

The main output is powered from the FB5 pin (i.e., bootstrapped) for higher speed and lower on-resistance of the power MOSFET. This SMPS consists of an error comparator, an output undervoltage-lockout comparator (set at 4V output), a timing generator for t_{ON} and t_{OFF}, a current-limit comparator, a MOSFET driver, and the power switch (Figure 2).

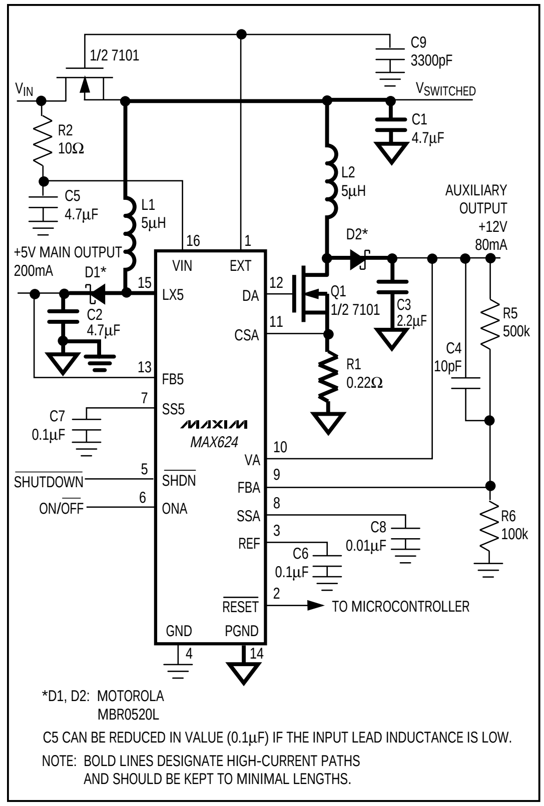


Figure 1. Standard Application Circuit

The error comparator's noninverting input voltage is internally set to V_{REF}. FB5's voltage is scaled internally, so that when it exceeds 5V the comparator output trips and shuts down the PFM.

Leaving only the error comparator on when the switch is off keeps the quiescent current low. The current comparator is powered up after the switch is turned on. This provides leading-edge blanking on the current comparator, in order to filter noise spikes caused by switch gate capacitance so they don't trip the overcurrent comparator and turn off the switch.

The main PFM has an undervoltage-lockout circuit that trips at 4V (preset internal threshold). Until the 4V threshold is reached, the timing generator is disabled and a 100kHz start-up oscillator is used to generate the output.

Table 1. Recommended Components for 12V/80mA Auxiliary SMPS and 5V Main SMPS

DESIGNATION	QTY	DESCRIPTION	SOURCE/TYPE
Q1	1	Dual, N-channel MOSFET	IRF7101 or Si9956DY
L1, L2	2	5µH inductors	Sumida CLS-62B, drawing #94T-217
C1, C2	2	4.7µF ceramic capacitors	Marcon THCR40E1E475ZT or THCS40E1E475ZT
C3	1	2.2µF ceramic capacitor	Marcon THCR30E1E225ZT or THCS30E1E225ZT
C4	1	10pF capacitor	
C5, C6, C7	3	0.1µF capacitors	Murata-Erie GRM42-6X7R104K025V
C8	1	10nF capacitor	
C9	1	3300pF capacitor	
D1, D2	2	I_F = 1A, V_R = 20V Schottky rectifier	Motorola MBR0520L
R1	1	0.22Ω ±10% resistor	Ohmtek 1205LR220LBT or IMS RC-I-1206
R2	1	10Ω resistor	

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX
IMS	(401) 683-9700	(401) 683-5571
International Rectifier	(310) 241-7876	(310) 640-6515
Motorola	(602) 244-3576	(602) 244-4015
Murata-Erie	(800) 831-9172	(814) 238-0490
Ohmtek	(716) 283-4025	(716) 283-5932
Siliconix	(408) 988-8000	(408) 970-3950
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	(03) 607-5111	(03) 607-5144
Toshiba Marcon	(708) 913-9980	(708) 913-1150

Table 3. Operating States

STATE	V_{IN}	$\overline{SHDN}$	ONA	V_{MAIN}	V_{AUX}*	EXT	I (V_{IN})
Reset	<2.8V	X	X	OFF	OFF	OFF	10µA
Shutdown	>2.8V	LO	X	OFF	OFF	ON	40µA
Main On	>2.8V	HI	LO	5.0V	OFF	ON	0.52mA
Both On	>2.8V	HI	HI	5.0V	12V**	ON	1.2mA

* When off, V_{AUX} = V_{IN}.
** V_{AUX} is set to 12V in this example.

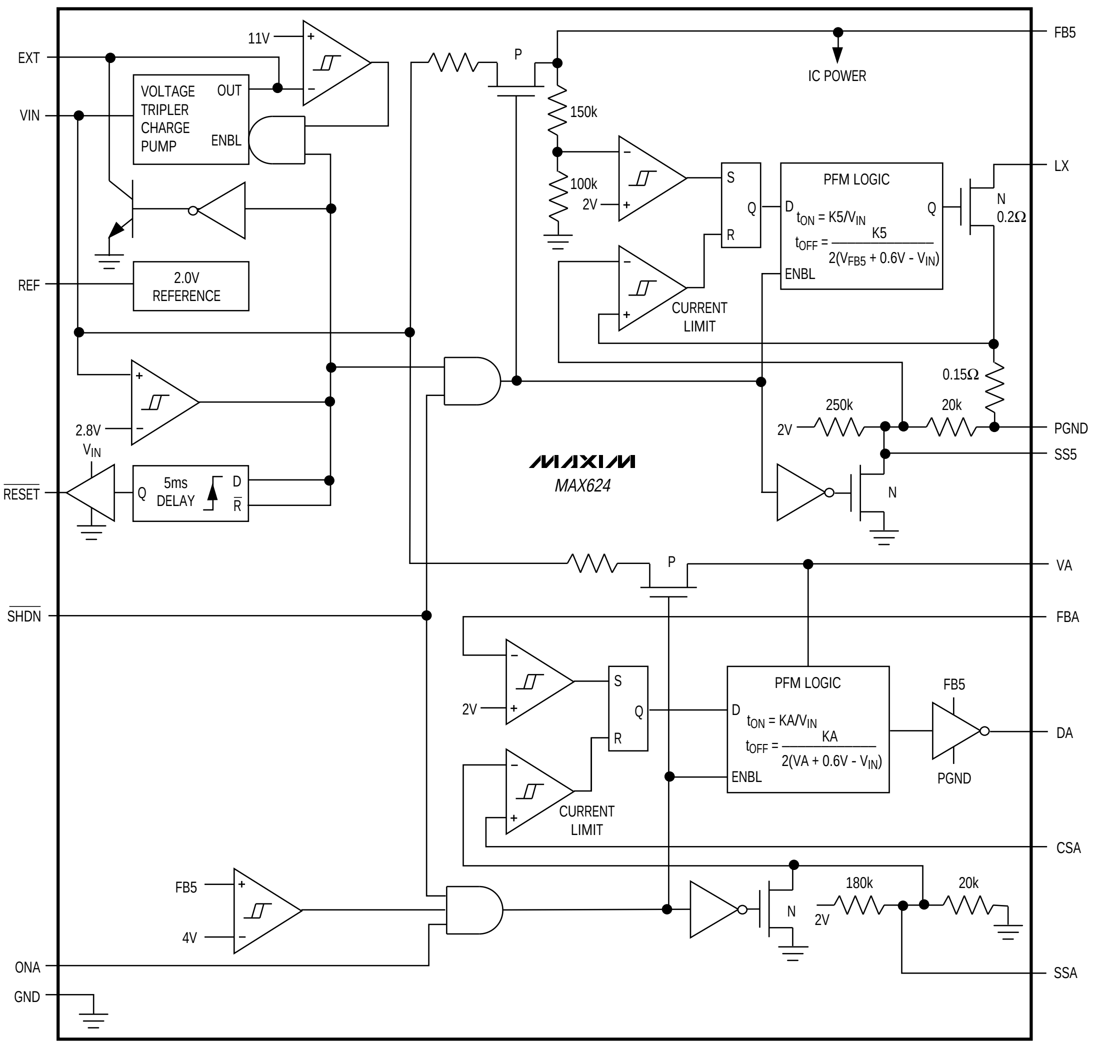


Figure 2. Functional Block Diagram

Adjustable Auxiliary SMPS

The auxiliary output is adjustable from 5V to 15V; two external resistors set the output voltage. The auxiliary SMPS is similar to the main SMPS, but it does not have an undervoltage-lockout comparator, and requires an external power MOSFET (see *Typical Operating Circuit* and *Design Procedure for Main and Auxiliary SMPS*).

The 5V SMPS undervoltage-lockout circuit overrides the ONA input until the 5V main SMPS (V_{MAIN}) output reaches about 4V. This feature ensures that the external auxiliary SMPS MOSFET has sufficient gate-drive voltage.

The adjustable output voltage can be increased to 30V or higher (Figure 9). However, such high output voltages cause the inductor current to become discontinuous, consequently reducing the load-current capability.

Voltage Reference

The MAX624's internal 2.00V reference is powered from the VIN input. The reference is kept alive in all modes (needed for reset function) and must be bypassed with a 0.1µF capacitor to GND for low-noise operation. No external load current is allowed.

Pulse-Frequency-Modulation Control Scheme

A unique pulse-frequency-modulation (PFM) control scheme, with adjustable on-time/off-time circuitry and current limit, is a key feature of both the main SMPS regulator and the auxiliary SMPS converter. The PFM scheme combines the advantages of pulse-width modulation (high output power and efficiency) with those of a traditional pulse-skipper (ultra-low quiescent currents). The on-time is calculated from the input voltage, and the off-time is calculated from V_{OUT} - V_{IN}. The off-time is divided by two so that the inductor current can ramp into continuous conduction. Switch on-times are adjusted down at high input voltages in order to minimize output ripple.

Use the following formulas to calculate t_{ON} and t_{OFF}:

$$t_{ON} = K / V_{IN}$$
$$t_{OFF} = 0.5 \times K / (V_{OUT} + 0.6V - V_{IN})$$

Nominally, K = 1.3µs-V for the main SMPS, and K = 2.2µs-V for the auxiliary SMPS. The K (design constant) scale factor that sets the switching frequency also sets the peak inductor current to control no-load output ripple at low input-to-output differentials (e.g., V_{IN} = 5V, V_{OUT} = 5V).

The PFM's high switching frequency (1MHz) helps reduce external component size. When the peak current limit is reached, the MOSFET switch turns off for at least the off-time set by the one-shot. When the comparator monitoring the output voltage is less than the desired value, it starts another cycle by turning the switch on.

Surge Prevention

Surge prevention is accomplished by slowly high-side driving an N-channel switch. The gate is driven by an on-chip charge pump that triples the input voltage. This charge pump is powered from the input voltage and runs continuously. The reset trip voltage is set to 2.8V to guarantee that the surge-prevention MOSFET can be turned on under worst-case low input voltage conditions. Otherwise, the card would go out of reset even though the supply voltage is unavailable.

Design Procedure for Main and Auxiliary SMPS

Output Filter Capacitor Selection

The output filter capacitor should have the minimum possible ESR for low ripple, and the minimum possible value for smallest physical size (i.e., ceramic). Larger sizes can be used for lower cost (i.e., tantalum). The output ripple is the sum of two components, due to C_F and ESR.

To select the filter capacitor value, follow the steps below:

1) Select the maximum ripple you can tolerate (e.g., 80mV).
2) Calculate the value of C_F, using the formula below:

$$C_F \text{ (in F)} > \frac{2 \times K \times I_{LOAD}}{V_{RIPPLEC} (V_{OUT} + 0.5V - V_{IN})}$$

where K is a design constant. Use the worst-case value from the *Electrical Characteristics*.

3) Calculate the output capacitor's required ESR, using the formula below.

$$ESR \text{ (in } \Omega) < \frac{V_{RIPPLEESR} \times V_{IN}}{4 \times I_{LOAD} (V_{OUT} + 0.5V - V_{IN})}$$

For example: For the 5V main SMPS with K = 1.7µs-V, I_{LOAD} = 200mA, V_{OUT} = 5V, V_{IN} = 3.3V, and maximum tolerable ripple = 80mVp-p, assume $V_{RIPPLEC}$ = 60mV and $V_{RIPPLEESR}$ = 20mV. Calculate C_F > 5µF with ESR < 37mΩ.

Inductor Selection

Select the inductor value to optimize one of the following:

- High Load Currents: Higher inductor values give higher load currents, since the inductor operates in deep continuous conduction.
- Small Physical Size: Lower inductor values result in lower energy storage requirements, hence smaller physical size. The filter capacitor can also be smaller, since the inductor current can ramp up faster when the load is suddenly increased.

To select the inductor value for the main SMPS, take the following steps:

1) Select the input voltage.
2) Select I_{LIMIT} and I_{LOAD}.
3) Use the specified data sheet values and the following formula:

$$L \text{ (in H)} = \frac{SR5 \times K5 (V_{IN} - A)}{2 \times I_{LIMIT} (V_{IN} + A) - 2 \times I_{LOAD} \times B}$$

$A = I_{LIMIT} \times R_{ON}$
$B = V_{OUT} + V_{DIODE}$

where: inductor current = I_{LIMIT}(min) = 0.7A, I_{LOAD}(min) = 200mA, SR5 (the switch off-time ratio) = 0.8, K5(max) = 1.7µs-V, R_{ON}(max) = 0.6Ω, V_{OUT} = 5V, V_{DIODE} = 0.5V, V_{IN}(min) = 3.0V, and L = 5µH (for best performance, use a Sumida 5µH (CLS-62B)).

Input Filter Capacitor Selection

The input filter capacitor is required to reduce reflected current ripple to the input source, and to improve efficiency by providing a low-impedance path for the ripple current. For memory card applications, the input filter capacitor is absolutely necessary due to possible contact resistance in the edge connector. To limit surge currents, use smaller values. Ceramic capacitors are the best choice.

Output Voltage and Component Selection for the Auxiliary SMPS

To select the output voltage and component values for the auxiliary SMPS, take the following steps:

1) Select the desired output voltage between 5V and 15V (e.g., 12V).
2) Select the minimum input voltage (V_{IN}).
3) Select R6 and R5. Choose R6 in the 10kΩ to 200kΩ range (e.g., 100kΩ). Choose R5 = R6 (V_{OUT} / V_{REF} - 1). For example, if V_{OUT} = 12V, then R6 = 100kΩ and R5 = 500kΩ.
4) Select the desired output current (I_{OUT}). Calculate the minimum inductor current (I_{LIMIT}) using the following formula:

   $$I_{LIMIT} \text{ (in Amps)} = [(V_{OUT} + 0.5V) / (V_{IN}(min) - 0.3V)] \times I_{LOAD} \times 2$$

   For example: V_{OUT} = 12V, V_{IN}(min) = 3V, I_{LOAD} = 80mA, and I_{LIMIT} = 0.7A.
5) To calculate the minimum required inductor value, use the following formula:

   $$L \text{ (in H)} = \frac{SRA \times KA (V_{IN} - A)}{2 \times I_{LIMIT} (V_{IN} - A) - 2 \times I_{LOAD} \times B}$$

   $A = I_{LIMIT} \times R_{ON}$

   $B = V_{OUT} + V_{DIODE}$

   For example: I_{LOAD} = 80mA, I_{LIMIT} = 0.7A (calculated using the above formula), SRA (switch off-time ratio) = 0.9, KA (switch on-time) = 3.0µs-V, R_{ON}(max) = 0.2Ω, V_{OUT} = 12V, V_{DIODE} = 0.5V, and L(min) = 3.8µH.
6) R (in Ω) = 180mV / I_{LIMIT} = 0.25Ω for I_{LIMIT} = 0.7A.
7) To select the output capacitor value, take the following steps:

   A) Select the maximum ripple you can tolerate.

   B) Calculate C_F using the formula below.

   $$C_F \text{ (in F)} = \frac{2 \times KA \times I_{LOAD}}{V_{RIPPLE}C \times (V_{OUT} + 0.5 - V_{IN})}$$

   C) Calculate the output capacitor's required ESR using the formula below.

   $$ESR \text{ (in } \Omega) = \frac{V_{RIPPLE}ESR \times V_{IN}}{4 \times I_{LOAD} \times (V_{OUT} + 0.5V - V_{IN})}$$

PC Board Layout and Grounding

Because of the MAX624's high-frequency operation, careful PC board layout is necessary to minimize ground bounce and noise. PC board layout instructions should be explicit, and the layout artist should work from a pencil sketch that shows the placement of power switching components and high-current routing. Use Figures 3–8 (the component placement guide and PC board layouts for the MAX624 evaluation board) as a rough guide for component placement and ground connections. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the following step-by-step guide.

1) Place the high-power components (C1, C2, C3, D1, D2, L1, L2, Q1, and R1) first.

   Priority 1: Minimize current-sense resistor trace lengths.

   Priority 2: Minimize ground trace lengths in the high-current paths (the bold lines in the application circuits).

   Priority 3: Minimize other trace lengths in the high-current paths. Use traces more than 5mm wide.

   Ideally, surface-mount power components are butted up against one another with their ground terminals almost touching. These high-current grounds

(C1, C2, C3, R1, and PGND) are then connected with a wide filled zone of top-layer copper, so they don't go through vias. The resulting top-layer "sub-ground plane" is connected to the normal inner-layer ground plane at the ground output terminals (at the ground of C2). Other high-current paths should also be minimized, but focusing on short ground and current-sense connections eliminates about 90% of all PC board layout problems. See Figures 3–8 for examples.

2) Place the IC and signal components. Keep the main switching node traces (LX node) short and away from sensitive analog components (current-sense traces and REF and SS capacitors). Important: the IC must be no farther than 5mm from the current-sense resistor. Keep the gate-drive trace shorter than 10mm and route it away from REF and SS.

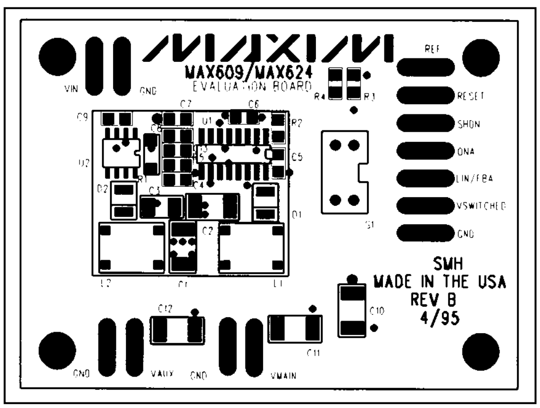


Figure 3. MAX624 PC Board Component Placement Guide

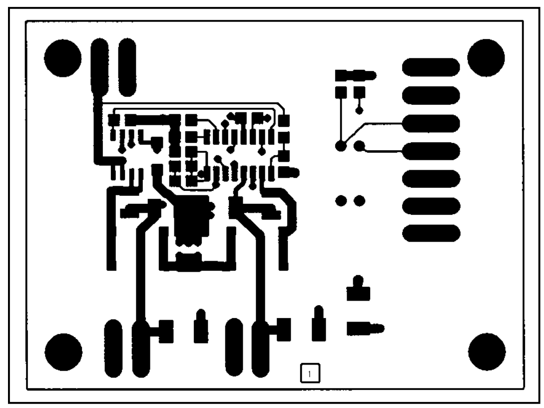


Figure 5. MAX624 PC Board Layout—Component Side

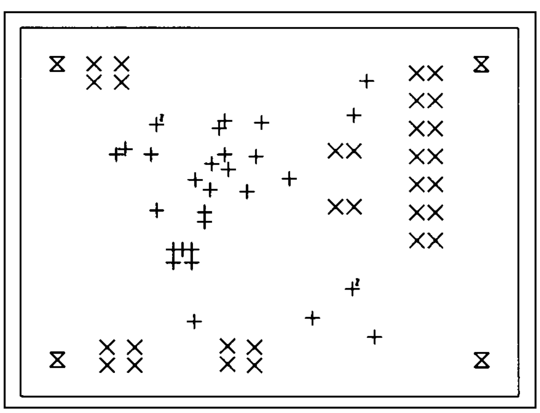


Figure 4. MAX624 PC Board Drill and Mechanical Guide

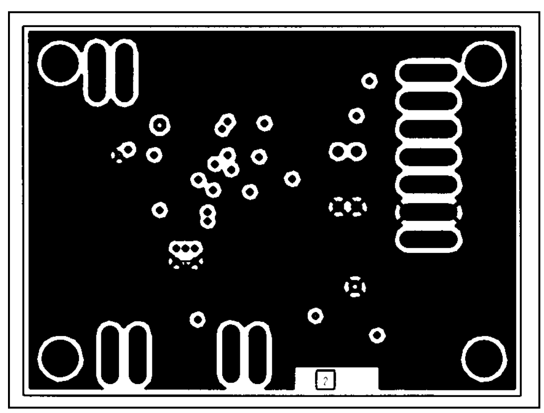


Figure 6. MAX624 PC Board Layout—$V_{SWITCHED}$ Plane

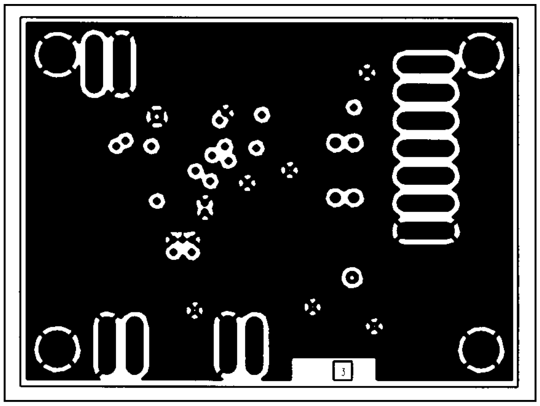


Figure 7. MAX624 PC Board Layout—Ground Plane

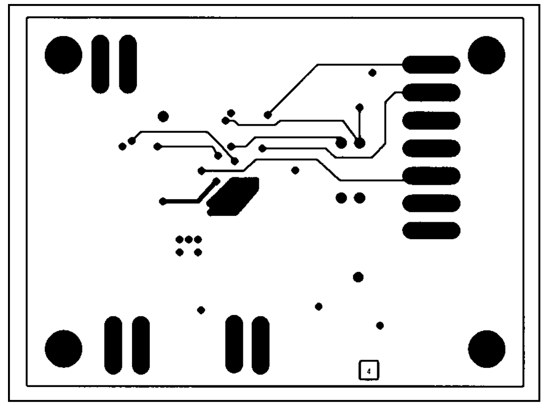


Figure 8. MAX624 PC Board Layout—Solder Side

Application Circuits

Positive 30V Auxiliary Output Circuits

The MAX624 can be used to generate a 30V output at 25mA (Figures 9 and 10). Note that the 12V zener clamp shown in Figure 10 must be used for 5V input applications. A 30V output at 25mA can be generated by tying the VA pin to the main SMPS output, but this circuit does not make optimal use of the inductor (the off-time is about 0.5µs). An alternative approach is to clamp the VA output to 12V using a zener. The off-time is optimized (reduced), which in turn makes better use of the inductor and produces a higher output current of about 35mA (Figure 10). Note that the 12V zener clamp shown in Figure 10 must be used for 5V input applications.

Negative Output Application Circuit

The MAX624 can be used to generate a negative 30V output to power-up LCD supplies (Figure 11). This circuit is part switching regulator and part charge pump. The switching regulator boosts the input to a high positive voltage (30V), while the actual negative voltage is generated using a charge-pump tap on the switching node. The negative 30V output has a 5% load-regulation error from 1mA to 20mA. The ratio of R5 and R6 resistors can be used to adjust the LCD contrast.

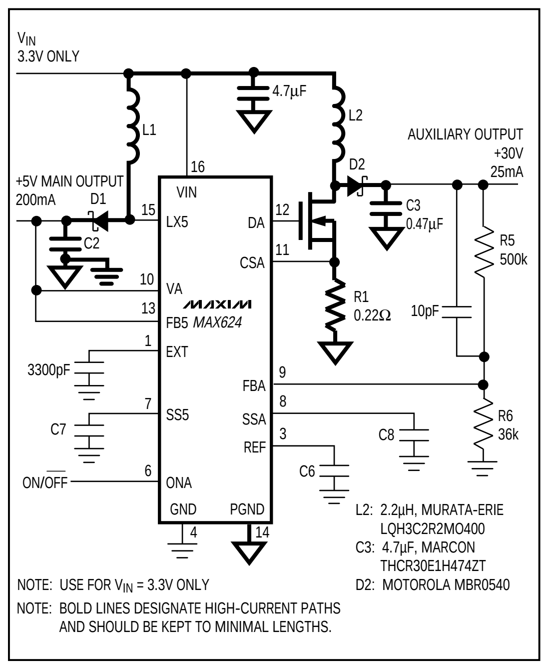


Figure 9. Positive 30V (25mA) Auxiliary Output Application Circuit

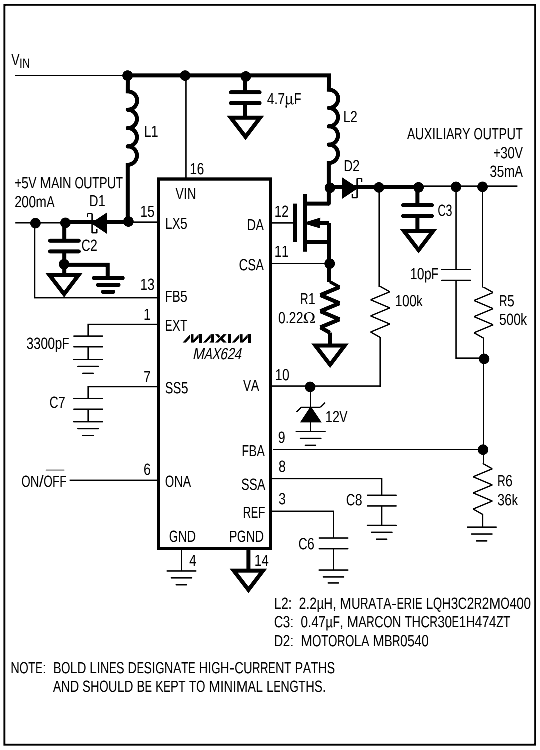


Figure 10. Positive 30V (35mA) Auxiliary Output Application Circuit

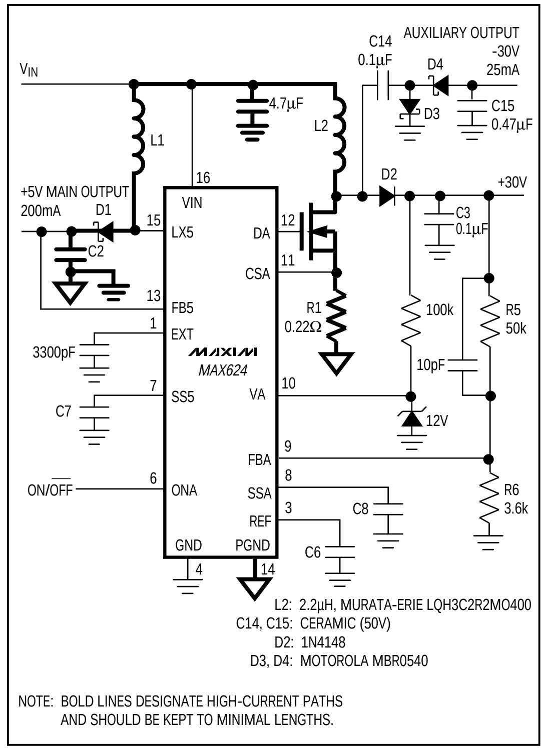
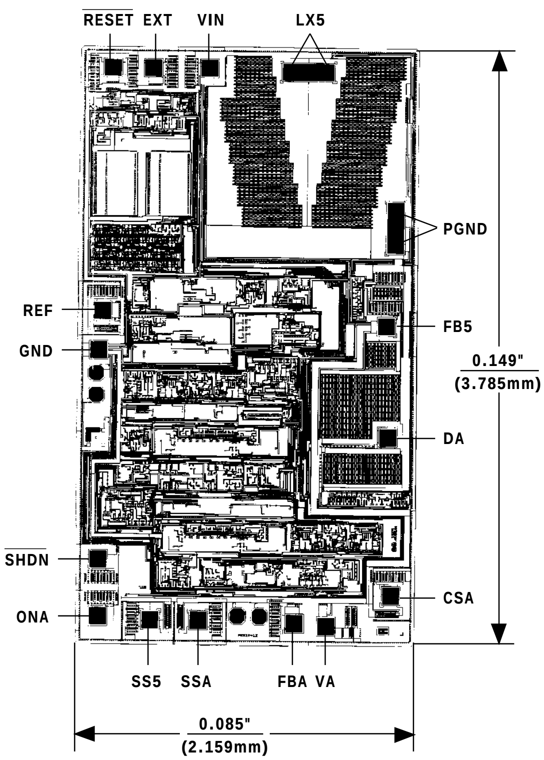


Figure 11. Negative 30V Auxiliary Output Application Circuit

Chip Topography



TRANSISTOR COUNT: 926
SUBSTRATE CONNECTED TO GND