19-1979; Rev 0a; 3/01

Quad-Output TFT LCD DC-DC Converters with Buffer

General Description

The MAX1778/MAX1880–MAX1885 multiple-output DC-DC converters provide the regulated voltages required by active matrix thin-film transistor (TFT) liquid crystal displays (LCD) in a low-profile TSSOP package. One high-power step-up converter and two low-power charge pumps convert the 2.7V to 5.5V input voltage into three independent output voltages. A built-in linear regulator and VCOM buffer complete the power-supply requirements.

The main step-up converter accurately generates an externally set output voltage up to 13V that can supply the display's row/column drivers. The converter's high switching frequency and current-mode PWM architecture provide fast transient response and allow the use of small low-profile inductors and ceramic capacitors. The low-power BiCMOS control circuitry and internal 14V switch (0.35Ω N-channel MOSFET) enable efficiencies up to 91%.

The dual low-power charge pumps (MAX1778/MAX1880/MAX1881/MAX1882 only) independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and -40V. A unique control scheme minimizes output ripple as well as capacitor sizes for both charge pumps.

A resistor-programmable, 40mA, low-dropout linear regulator (MAX1778/MAX1881/MAX1883/MAX1884 only) provides preregulation or postregulation for any of the supplies. For higher current applications, an external transistor can be added. Additionally, the VCOM buffer provides a high current output that is ideal for driving the capacitive backplane of TFT LCD panels. The VCOM buffer's output voltage is preset with an internal 50% resistive-divider or can be externally adjusted for other voltages.

The MAX1778/MAX1880–MAX1885 are protected against output undervoltage and thermal overload conditions by a latched fault detection circuit that shuts down the device. All devices are available in the ultra-thin TSSOP package (1.1mm max height).

Applications

TFT LCD Notebook Displays

TFT LCD Desktop Monitor Panels

Features

- **500kHz/1MHz Current-Mode PWM Step-Up Regulator**
  - **Up to +13V Main High-Power Output**
  - **±1% Accurate**
  - **High Efficiency (91%)**
- **Dual Regulated Charge-Pump Outputs (MAX1778/MAX1880/MAX1881/MAX1882 only)**
  - **Up to +40V Positive Charge-Pump Output**
  - **Up to -40V Negative Charge-Pump Output**
- **Low-Dropout 40mA Linear Regulator (MAX1778/MAX1881/MAX1883/MAX1884 only)**
  - **Up to +15V LDO Input**
- **Optional Higher Current with External Transistor**
- **2.7V to 5.5V Input Supply**
- **Internal Supply Sequencing and Soft-Start**
- **Power-Ready Output**
- **Adjustable Fault-Detection Latch**
- **Thermal Protection (+160°C)**
- **0.1µA Shutdown Current**
- **0.7mA IN Quiescent Current**
- **Ultra-Small External Components**
- **Thin TSSOP Package (1.1mm max height)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1778EUG	-40°C to +85°C	24 TSSOP
MAX1880EUG	-40°C to +85°C	24 TSSOP
MAX1881EUG	-40°C to +85°C	24 TSSOP
MAX1882EUG	-40°C to +85°C	24 TSSOP
MAX1883EUP	-40°C to +85°C	20 TSSOP
MAX1884EUP	-40°C to +85°C	20 TSSOP
MAX1885EUP	-40°C to +85°C	20 TSSOP

Typical Operating Circuit appears at end of data sheet.

Pin Configurations and Selector Guide appear at end of data sheet.

Quad-Output TFT LCD DC-DC Converters with Buffer

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, TGND, FLTSET to GND ....-0.3V to +6V
DRVN to GND ....-0.3V to (V_{SUPN} + 0.3V)
DRVP to GND ....-0.3V to (V_{SUPP} + 0.3V)
$\overline{PGND}$ to GND ....±0.3V
$\overline{RDY}$, SUPB to GND ....-0.3V to +14V
LX, SUPP, SUPN to PGND ....-0.3V to +14V
SUPL to GND...-0.3V to +18V
LDOOUT to GND ....-0.3V to (V_{SUPL} + 0.3V)
INTG, REF, FB, FBN, FBP to GND..............-0.3V to (V_{IN} + 0.3V)
FBL to GND ....-0.3V to the lower of (V_{SUPL} + 0.3V) or +6V
BUFOUT, BUF+, BUF- to GND ....-0.3V to (V_{SUPB} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
24-Pin TSSOP (derate 12.2mW/°C above +70°C) 975mW
Operating Temperature Range
MAX1778EUG, MAX1883EUP ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{IN}			2.7		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 40mV hysteresis (typ)		2.2	2.4	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V	MAX1778/MAX1880/ MAX1883 (f_{OSC} = 1MHz)		0.7	1	mA
			MAX1881/MAX1882/ MAX1884/MAX1885 (f_{OSC} = 500kHz)		0.6	1	
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.4	0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.3	0.5	
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.4	0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.3	0.5	
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V			0.1	10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			0.1	10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			0.1	10	µA
SUPL Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPL} = 13V MAX1778/MAX1881/MAX1883/MAX1884			0.1	10	µA
SUPB Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPB} = 13V			6	13	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN STEP-UP CONVERTER						
Main Output Voltage Range	V_{MAIN}		V_{IN}		13	V
FB Regulation Voltage	V_{FB}	Integrator enabled, C_{INTG} = 1000pF	1.234	1.247	1.260	V
		Integrator disabled (INTG = REF)	1.220		1.280	
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND	-50		+50	nA
Operating Frequency	f_{OSC}	MAX1778/MAX1880/MAX1883	0.85	1	1.15	MHz
		MAX1881/MAX1882/MAX1884/MAX1885	425	500	575	kHz
Oscillator Maximum Duty Cycle			80	85	91	%
Load Regulation		I_{LX} = 0 to 200mA, V_{MAIN} = 10V; Integrator enabled, C_{INTG} = 1000pF		0.01		%
		I_{LX} = 0 to 200mA, V_{MAIN} = 10V; Integrator disabled (INTG = REF)		0.2		
Line Regulation				0.1		%/V
Integrator Transconductance				317		µs
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA		0.35	0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V		0.01	20	µA
LX Current Limit	I_{LIM}	Phase I = soft-start (1024/f_{OSC})	0.275	0.38	0.5	A
		Phase II = soft-start (1024/f_{OSC})		0.75		
		Phase III = soft-start (1024/f_{OSC})		1.12		
		Phase IV = fully-on (after 3072/f_{OSC})	1.15	1.5	1.85	
Maximum RMS LX Current				1		A
Soft-Start Period	t_{SS}	Power-up to the end of Phase III		3072 / f_{OSC}		s
FB Fault Trip Level		Falling edge, FLTSET = GND	1.07	1.1	1.14	V
		Falling edge, FLTSET = 1V	0.955	0.99	1.025	
POSITIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 ONLY)						
SUPP Input Supply Range	V_{SUPP}		2.7		13	V
Operating Frequency	f_{CHP}			0.5 x f_{OSC}		Hz
FBP Regulation Voltage	V_{FBP}		1.2	1.25	1.3	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50		+50	nA
DRVP PCH On-Resistance	$R_{PCH(ON)}$			5	10	Ω
DRVP NCH On-Resistance	$R_{NCH(ON)}$	V_{FBP} = 1.2V		2	4	Ω
		V_{FBP} = 1.3V	20			kΩ
Maximum RMS DRVP Current				0.1		A
FBP Power-Ready Trip Level		Rising edge	1.09	1.125	1.16	V
FBP Fault Trip Level		Falling edge, FLTSET = GND	1.08	1.11	1.16	V
		Falling edge, FLTSET = 1V	0.955	0.99	1.025	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NEGATIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 ONLY)							
SUPN Input Supply Range	V_{SUPN}			2.7		13	V
Operating Frequency	f_{CHP}				0.5 x f_{OSC}		Hz
FBN Regulation Voltage	V_{FBN}			-50	0	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0		-50		+50	nA
DRVN PCH On-Resistance	$R_{PCH(ON)}$				5	10	Ω
DRVN NCH On-Resistance	$R_{NCH(ON)}$	V_{FBN} = +50mV			2	4	Ω
		V_{FBN} = -50mV		20			kΩ
Maximum RMS DRVN Current					0.1		A
FBN Power-Ready Trip Level		Falling edge		80	125	165	mV
FBN Fault Trip Level		Rising edge		80	140	190	mV
LOW-DROPOUT LINEAR REGULATOR (MAX1778/MAX1881/MAX1883/MAX1884 ONLY)							
SUPL Input Supply Range	V_{SUPL}			4.5		15	V
SUPL Undervoltage Lockout		Rising edge, 50mV hysteresis (typ)		3.8	4	4.3	V
SUPL Quiescent Current	I_{SUPL}	I_{LDO} = 100µA			120	220	µA
Dropout Voltage (Note 1)	V_{DROP}	LDO is set to regulate at 9V	I_{LDO} = 40mA		130	300	mV
			I_{LDO} = 5mA		70		
FBL Regulation Voltage	V_{FBL}	V_{SUPL} = 10V, LDO regulating at 9V, I_{LDO} = 15mA		1.235	1.25	1.265	V
LDO Load Regulation		V_{SUPL} = 10V, LDO regulating at 9V, I_{LDO} = 100µA to 40mA				1.2	%
LDO Line Regulation		V_{SUPL} = 4.5V to 15V, FBL = LDOOUT, I_{LDO} = 15mA				0.02	%/V
FBL Input Bias Current	I_{FBL}	V_{FBL} = 1.25V		-0.8		+0.8	µA
LDO Current Limit	I_{LDOLIM}	V_{SUPL} = 10V, V_{LDOOUT} = 9V, V_{FBL} = 1.2V		40	130	220	mA
VCOM BUFFER							
SUPB Input Supply Range	V_{SUPB}			4.5		13	V
SUPB Quiescent Current	I_{SUPB}	V_{SUPB} = 13V			420	850	µA
BUFOUT Leakage Current				-10		+10	µA
Power-Supply Rejection Ratio	PSRR	V_{SUPB} = 4.5V to 13V, V_{CM} = 2.25V		85	98		dB
Input Common-Mode Voltage Range	V_{CM}	$\lvert V_{OS} \rvert$ < 10mV		1.2		8.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.2V to 8.8V		75			dB
Input Bias Current	I_{BIAS}	V_{CM} = 5V		-100	-10	+100	nA
Input Offset Current	I_{OS}	V_{CM} = 5V		-100		+100	nA
Gain Bandwidth Product	GBW	C_{BUF} = 1µF			13		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{BUFOUT}	BUF+ = GND	I_{BUFOUT} = 0	4.99		5.01	V
			I_{BUFOUT} = ±5mA	4.97		5.03	
			I_{BUFOUT} = ±45mA	4.93		5.07	
Input Offset Voltage	V_{OS}	V_{SUPB} = 4.5V to 13V, V_{CM} = 1.2V to (V_{SUPB} –1.2V)	I_{BUFOUT} = ±5mA	-30		30	mV
			I_{BUFOUT} = ±45mA	-70		70	
Output Voltage Swing High	V_{OH}	I_{BUFOUT} = -45mA, ΔV_{OS} = 1V		9	9.6		V
Output Voltage Swing Low	V_{OL}	I_{BUFOUT} = +45mA, ΔV_{OS} = 1V			0.4	1	V
Peak Buffer Output Current					±150		mA
BUF+ Dual Mode™ Threshold Voltage		Falling edge, 20mV hysteresis (typ)		80	125	170	mV
REFERENCE							
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA		1.231	1.25	1.269	V
Reference Undervoltage Threshold				0.9	1.05	1.2	V
LOGIC SIGNALS							
$\overline{SHDN}$ Input Low Voltage						0.9	V
$\overline{SHDN}$ Input High Voltage				2.1			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$				0.01	1	µA
FLTSET Input Voltage Range				0.67 x V_{REF}		0.85 x V_{REF}	V
FLTSET Threshold Voltage		Rising edge, 25mV hysteresis (typ)		80	125	170	mV
FLTSET Input Current		V_{FLTSET} = 1V			0.1	50	nA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA			0.25	0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V			0.01	1	µA
Thermal Shutdown		Rising temperature			160		°C

Dual Mode is a registered trademark of Maxim Integrated Products, Inc.

Quad-Output TFT LCD DC-DC Converters with Buffer

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Input Supply Range	V_{IN}			2.7	5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} Rising, 40mV hysteresis (typ)		2.2	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V	MAX1778/MAX1880/ MAX1883 (f_{OSC} = 1MHz)		1	mA
			MAX1881/MAX1882/MAX1884/ MAX1885 (f_{OSC} = 500kHz)		1	
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.5	
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.5	
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V			10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			10	µA
SUPL Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPL} = 13V, MAX1778/MAX1881/MAX1883/MAX1884			10	µA
SUPB Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPB} = 13V			13	µA
MAIN STEP-UP CONVERTER						
Main Output Voltage Range	V_{MAIN}			V_{IN}	13	V
FB Regulation Voltage	V_{FB}	Integrator enabled, C_{INTG} = 1000pF		1.223	1.269	V
		Integrator disabled (INTG = REF)		1.21	1.29	
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND		-50	+50	nA
Operating Frequency	F_{OSC}	MAX1778/MAX1880/MAX1883		0.75	1.25	MHz
		MAX1881/MAX1882/MAX1884/MAX1885		375	625	kHz
Oscillator Maximum Duty Cycle				79	91	%
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA			0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V			20	µA
LX Current Limit	I_{LIM}	Phase I = soft-start (1024/f_{OSC})		0.275	0.525	A
		Phase IV = fully on (after 3072/f_{OSC})		1.1	2.05	
FB Fault Trip Level		Falling edge, FLTSET = GND		1.07	1.14	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
POSITIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 ONLY)					
SUPP Input Supply Range	V_{SUPP}		2.7	13	V
FBP Regulation Voltage	V_{FBP}		1.2	1.3	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50	+50	nA
DRVP PCH On-Resistance	$R_{PCH(ON)}$			10	Ω
DRVP NCH On-Resistance	$R_{NCH(ON)}$	V_{FBP} = 1.2V		4	Ω
		V_{FBP} = 1.3V	20		kΩ
FBP Power-Ready Trip Level		Rising edge	1.09	1.16	V
NEGATIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 ONLY)					
SUPN Input Supply Range	V_{SUPN}		2.7	13	V
FBN Regulation Voltage	V_{FBN}		-50	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0	-50	+50	nA
DRVN PCH On-Resistance	$R_{PCH(ON)}$			10	Ω
DRVN NCH On-Resistance	$R_{NCH(ON)}$	V_{FBN} = +50mV		4	Ω
		V_{FBN} = -50mV	20		kΩ
FBN Power-Ready Trip Level		Falling edge	80	165	mV
LOW DROPOUT LINEAR REGULATOR (MAX1778/MAX1881/MAX1883/MAX1884 ONLY)					
SUPL Input Supply Range	V_{SUPL}		4.5	15	V
SUPL Undervoltage Lockout		Rising edge, 50mV hysteresis (typ)	3.8	4.3	V
SUPL Quiescent Current	I_{SUPL}	I_{LDO} = 100µA		240	µA
Dropout Voltage (Note 1)	V_{DROP}	LDO regulating to 9V, I_{LDO} = 40mA		330	mV
FBL Regulation Voltage	V_{FBL}	V_{SUPL} = 10V, LDO regulating to 9V, I_{LDO} = 15mA	1.222	1.265	V
LDO Load Regulation		V_{SUPL} = 10V, LDO regulating to 9V, I_{LDO} = 100µA to 40mA		1.2	%
LDO Line Regulation		V_{SUPL} = 4.5V to 15V, FBL = LDOOUT, I_{LDO} = 15mA		0.02	%/V
FBL Input Bias Current	I_{FBL}	V_{FBL} = 1.25V	-1.2	+1.2	µA
LDO Current Limit	I_{LDOLIM}	V_{SUPL} = 10V, V_{LDOOUT} = 9V, V_{FBL} = 1.2V	40	260	mA
VCOM BUFFER					
SUPB Input Supply Range	V_{SUPB}		4.5	13	V
SUPB Quiescent Current	I_{SUPB}	V_{SUPB} = 13V		850	µA
BUFOUT Leakage Current			-10	+10	µA
Input Common-Mode Voltage	V_{CM}	$\|V_{OS}\|$ < 10mV	1.2	8.8	V

Quad-Output TFT LCD DC-DC Converters with Buffer

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

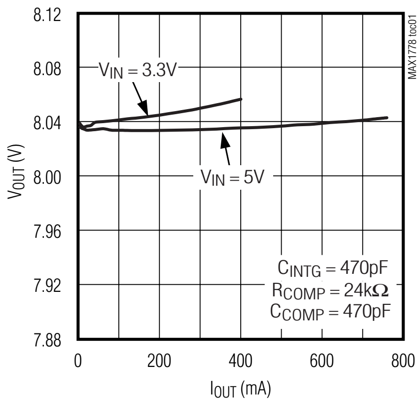
PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Input Bias Current	I_{BIAS}	V_{CM} = 5V		-500	+500	nA
Input Offset Current	I_{OS}	V_{CM} = 5V		-500	+500	nA
Output Voltage	V_{BUFOUT}	BUF+ = GND	I_{BUFOUT} = 0	4.988	5.012	V
			I_{BUFOUT} = ±5mA	4.97	5.03	
			I_{BUFOUT} = ±45mA	4.93	5.07	
Input Offset Voltage	V_{OS}	V_{SUPB} = 4.5V to 13V V_{CM} = 1.2V to (V_{SUPB} - 1.2V)	I_{BUFOUT} = ±5mA	-30	30	mV
			I_{BUFOUT} = ±45mA	-70	70	
Output Voltage Swing High	V_{OH}	I_{BUFOUT} = -45mA, ΔV_{OS} = 1V		9		V
Output Voltage Swing Low	V_{OL}	I_{BUFOUT} = +45mA, ΔV_{OS} = 1V			1	V
BUF+ Dual Mode Threshold Voltage		Falling edge, 20mV hysteresis (typ)		80	170	mV
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA		1.223	1.269	V
Reference Undervoltage Threshold				0.9	1.2	V
LOGIC SIGNALS						
$\overline{SHDN}$ Input Low Voltage					0.9	V
$\overline{SHDN}$ Input High Voltage				2.1		V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$				1	µA
FLTSET Input Voltage Range				0.74 x V_{REF}	0.85 x V_{REF}	V
FLTSET Threshold Voltage		Rising edge, 25mV hysteresis (typ)		80	170	mV
FLTSET Input Current		V_{FLTSET} = 1V			50	nA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA			0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V			1	µA

Note 1: Dropout Voltage is defined as the V_{SUPL} - V_{LDOOUT}, when V_{SUPL} is 100mV below the set value of V_{LDOOUT}.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

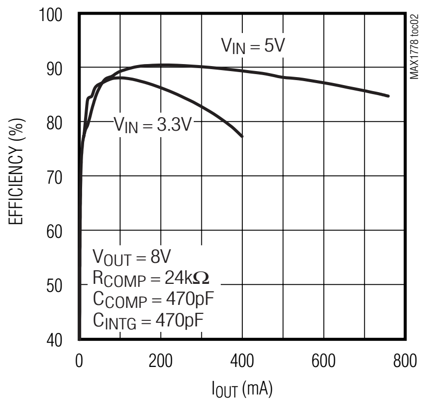
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

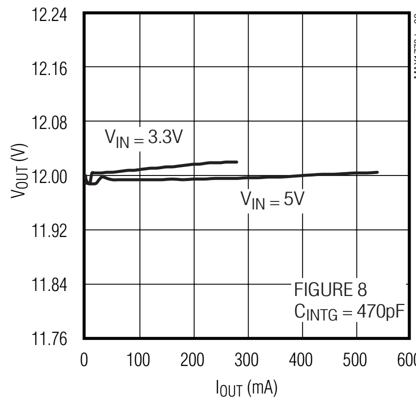
MAIN 8V OUTPUT VOLTAGE vs. LOAD CURRENT



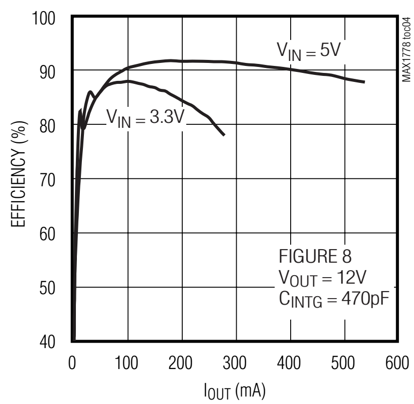
MAIN 8V OUTPUT EFFICIENCY vs. LOAD CURRENT



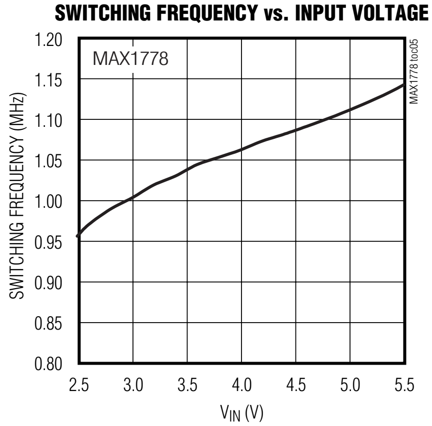
MAIN 12V OUTPUT VOLTAGE vs. LOAD CURRENT



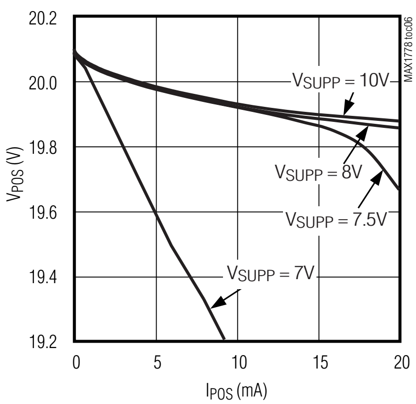
MAIN 12V OUTPUT EFFICIENCY vs. LOAD CURRENT



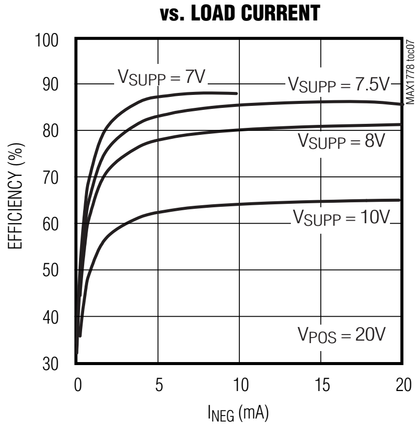
STEP UP CONVERTERS SWITCHING FREQUENCY vs. INPUT VOLTAGE



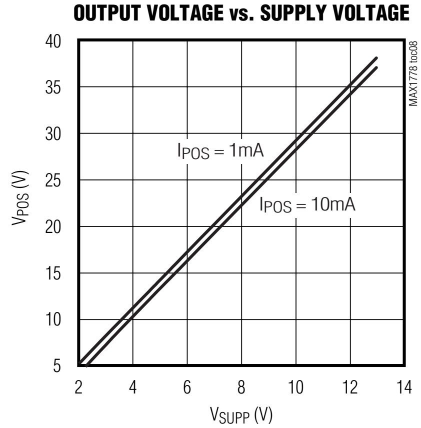
POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



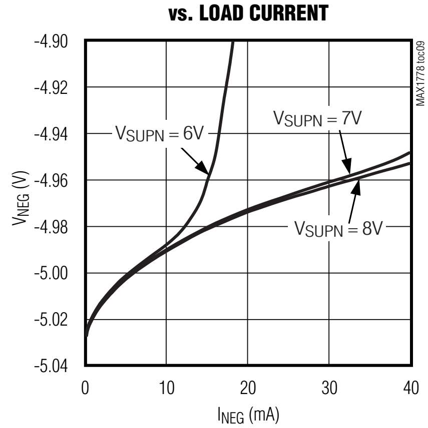
POSITIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



MAXIMUM POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT

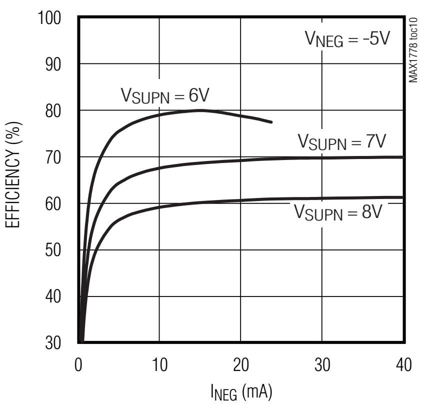


Quad-Output TFT LCD DC-DC Converters with Buffer

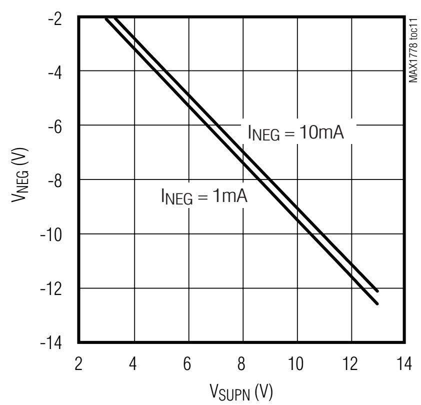
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

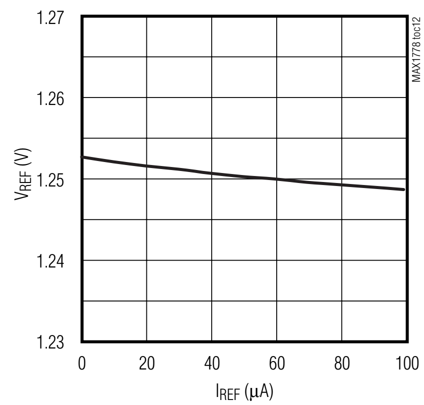
NEGATIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



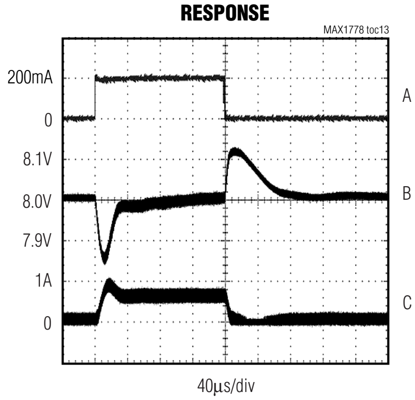
MAXIMUM NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT

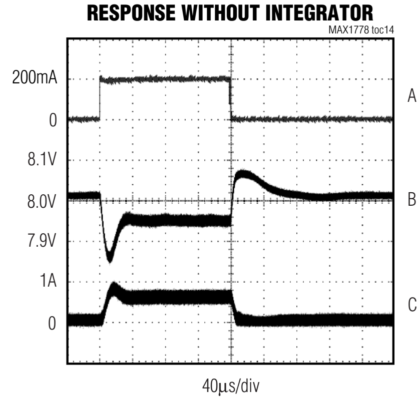


STEP-UP CONVERTER LOAD-TRANSIENT RESPONSE



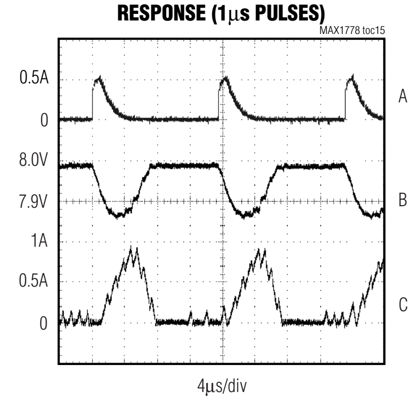
A. I_{MAIN} = 20mA to 200mA, 200mA/div
B. V_{MAIN} = 8V, 100mV/div
C. INDUCTOR CURRENT, 1A/div
C_{INTG} = 1000pF

STEP-UP CONVERTER LOAD-TRANSIENT RESPONSE WITHOUT INTEGRATOR



A. I_{MAIN} = 20mA to 200mA, 200mA/div
B. V_{MAIN} = 8V, 100mV/div
C. INDUCTOR CURRENT, 1A/div
INTG = REF

STEP-UP CONVERTER LOAD-TRANSIENT RESPONSE (1µs PULSES)

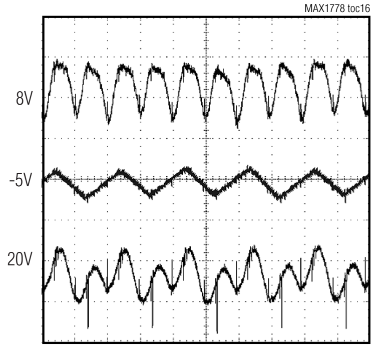


A. I_{MAIN} = 0 to 500mA, 500mA/div
B. V_{MAIN} = 8V, 100mV/div
C. INDUCTOR CURRENT, 500mA/div

Typical Operating Characteristics (continued)

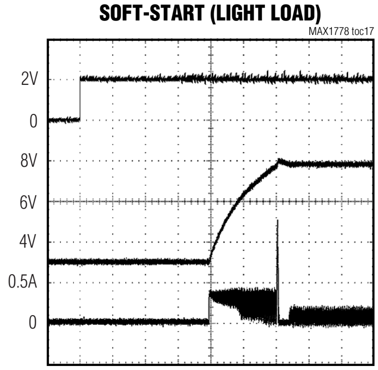
(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

RIPPLE VOLTAGE WAVEFORMS



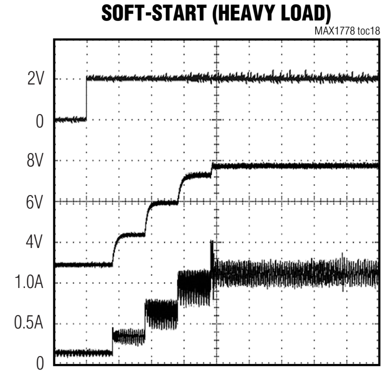
A. V_{MAIN} = 8V, I_{MAIN} = 200mA, 10mV/div
B. V_{NEG} = -5V, I_{NEG} = 10mA, 20mV/div
C. V_{POS} = 20V, I_{POS} = 5mA, 20mV/div

STEP-UP CONVERTER SOFT-START (LIGHT LOAD)



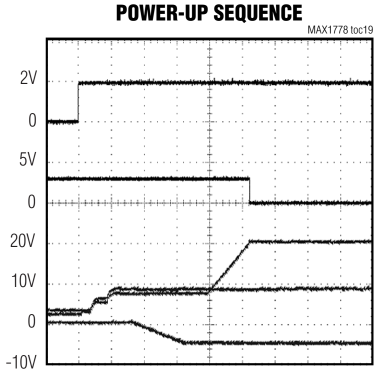
A. $V_{\overline{SHDN}}$ = 0 TO 2V, 2V/div
B. V_{MAIN} = 8V, 2V/div
C. INDUCTOR CURRENT, 500mA/div
R_{LOAD} = 400Ω

STEP-UP CONVERTER SOFT-START (HEAVY LOAD)



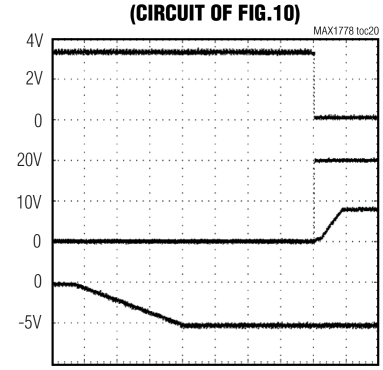
A. $V_{\overline{SHDN}}$ = 0 TO 2V, 2V/div
B. V_{MAIN} = 8V, 2V/div
C. INDUCTOR CURRENT, 500mA/div
R_{LOAD} = 20Ω

POWER-UP SEQUENCE



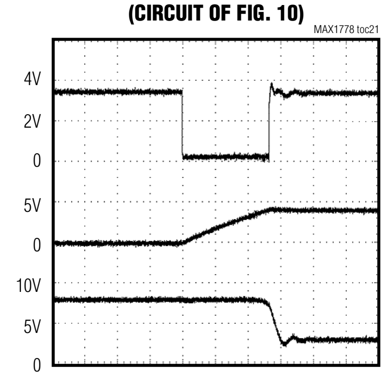
A. $V_{\overline{SHDN}}$ = 0 TO 2V, 2V/div
B. $\overline{RDY}$, 5V/div
C. POSITIVE CHARGE PUMP = V_{POS} = 20V, R_{LOAD} = 4kΩ, 10V/div
D. STEP-UP CONVERTER: V_{MAIN} = 8V, R_{LOAD} = 40Ω, 10V/div
E. NEGATIVE CHARGE PUMP: V_{NEG} = -5V, R_{LOAD} = 500Ω, 10V/div

POWER-UP SEQUENCE (CIRCUIT OF FIG.10)



A. $\overline{RDY}$, 2V/div
B. POSITIVE CHARGE PUMP, $V_{POS(SYS)}$ = 20V, 10V/div
C. STEP-UP CONVERTER: $V_{MAIN(SYS)}$ = 8V, 10V/div
D. NEGATIVE CHARGE PUMP, V_{NEG} = -5V, -5V/div

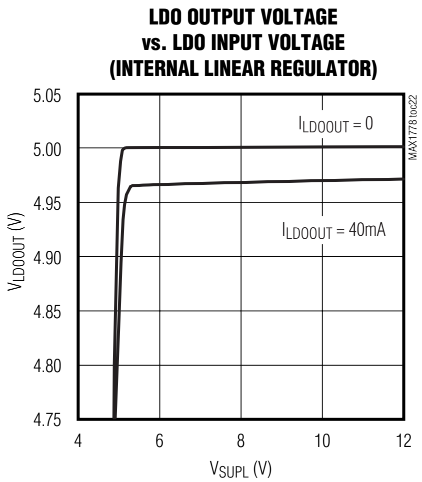
POWER-UP INTO SHORT-CIRCUIT (CIRCUIT OF FIG. 10)

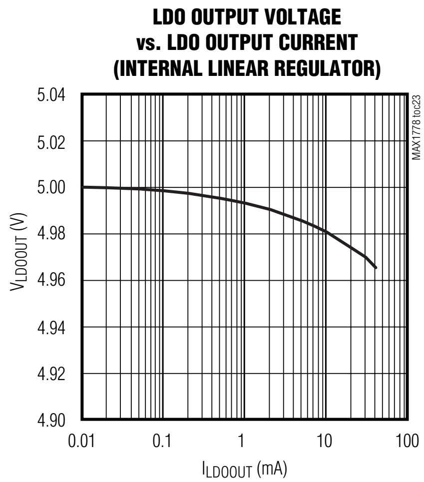


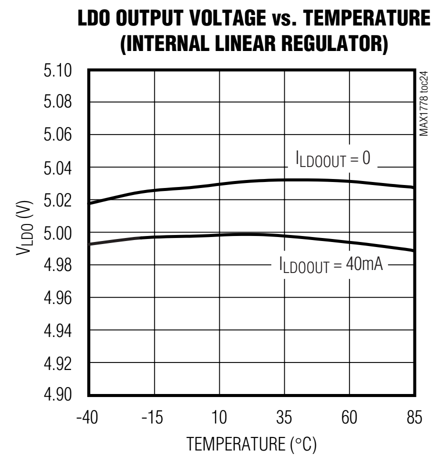
A. $\overline{RDY}$, 2V/div
B. GATE OF N-CH MOSFET, 5V/div
C. STEP-UP CONVERTER, $V_{MAIN(START)}$ = 8V, 5V/div
$V_{MAIN(SYS)}$ = GND

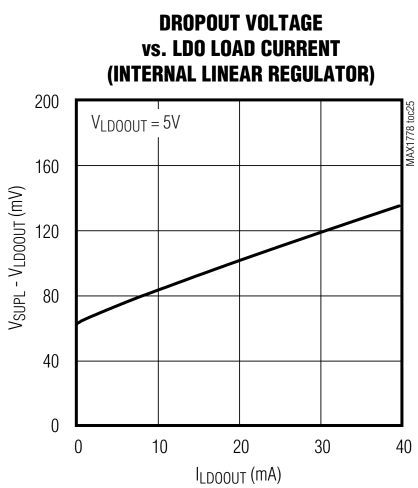
Typical Operating Characteristics (continued)

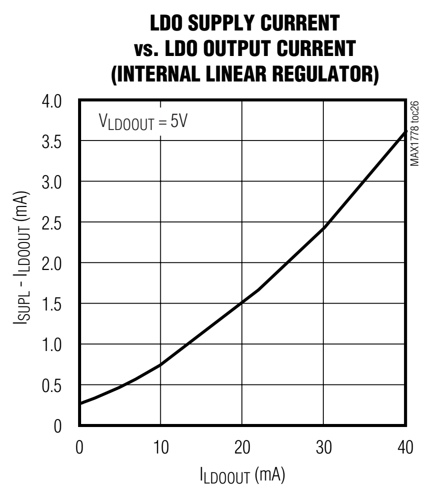
(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)







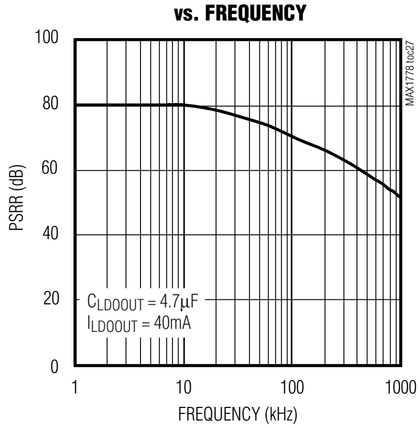




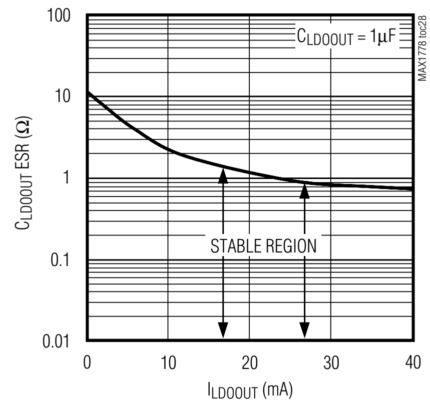
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

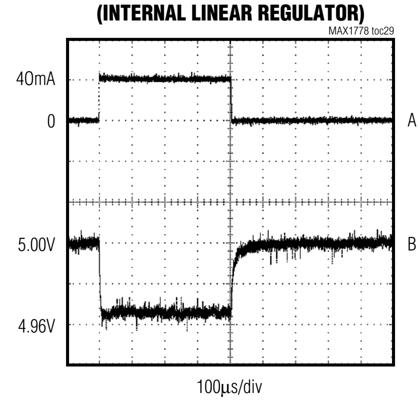
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



REGION OF STABLE C_{LDOOUT} ESR vs. LOAD CURRENT

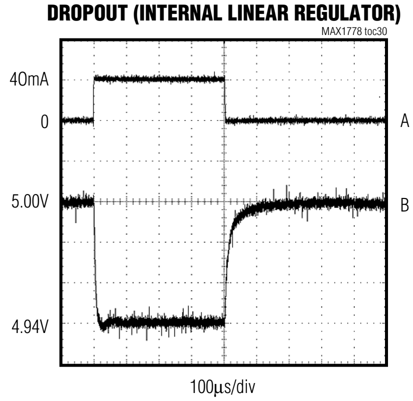


LOAD-TRANSIENT RESPONSE (INTERNAL LINEAR REGULATOR)



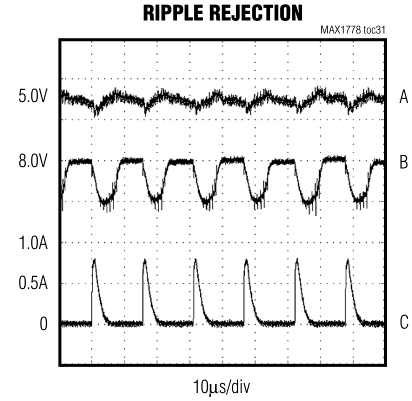
A. I_{LDO} = 100µA TO 40mA, 40mA/div
B. V_{LDO} = 5V, 20mV/div
V_{SUPL} = V_{LDO} + 500mV

LOAD-TRANSIENT RESPONSE NEAR DROPOUT (INTERNAL LINEAR REGULATOR)



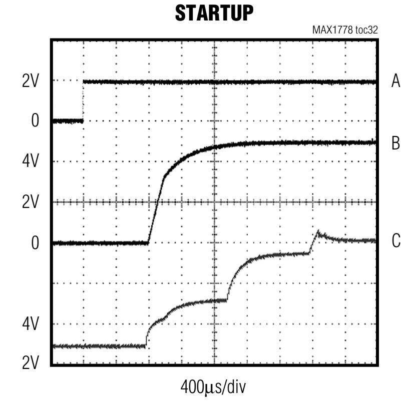
A. I_{LDO} = 100µA TO 40mA, 40mA/div
B. V_{LDO} = 5V, 20mV/div
V_{IN} = V_{LDO} + 100mV

INTERNAL LINEAR-REGULATOR RIPPLE REJECTION



A. V_{LDOOUT} = 5V, I_{LDOOUT} = 40mA, 10mV/div
B. V_{MAIN} = V_{SUPL} = 8V, 200mV/div
C. I_{MAIN} = 0 TO 750mA, 500mA/div

INTERNAL LINEAR-REGULATOR STARTUP



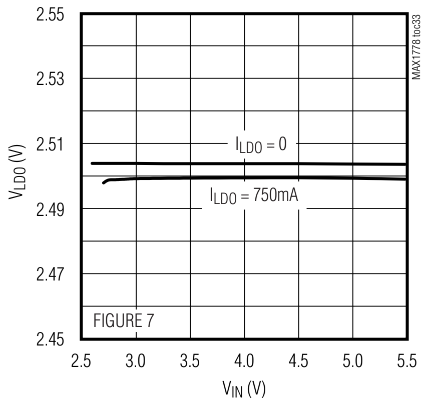
A. $V_{\overline{SHDN}}$ = 0 TO 2V, 2V/div
B. V_{LDOOUT} = 5V, R_{LDOOUT} = 125Ω, 2V/div
C. V_{MAIN} = 8V, R_{MAIN} = 40Ω, 2V/div

Quad-Output TFT LCD DC-DC Converters with Buffer

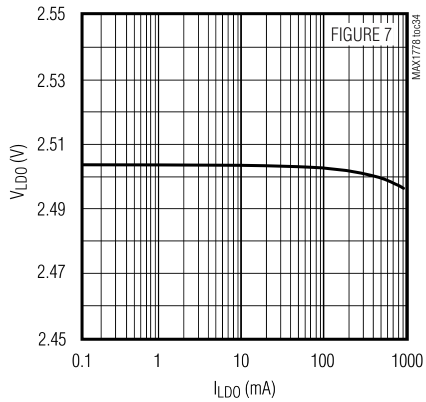
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

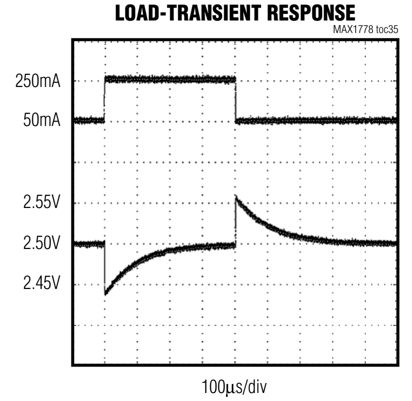
LINEAR-REGULATOR OUTPUT VOLTAGE vs. INPUT VOLTAGE (EXTERNAL LINEAR REGULATOR)



LINEAR-REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (EXTERNAL LINEAR REGULATOR)

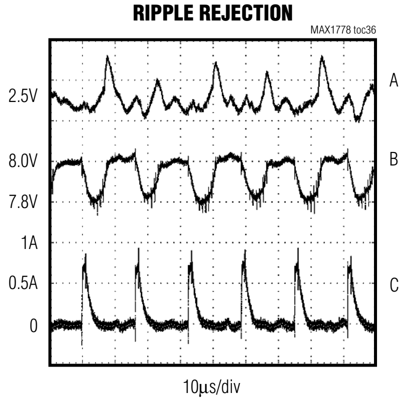


EXTERNAL LINEAR-REGULATOR LOAD-TRANSIENT RESPONSE



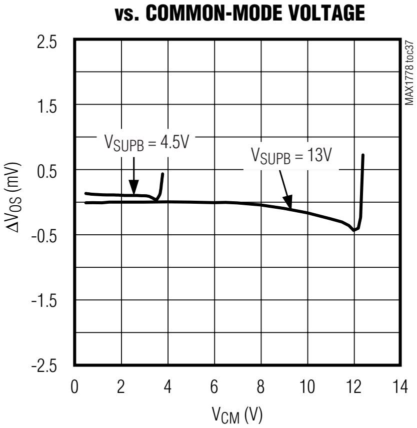
A. I_{LDO} = 50mA TO 250mA, 200mA/div
B. V_{LDO} = 2.5V, 50mV/div
FIGURE 7

EXTERNAL LINEAR-REGULATOR RIPPLE REJECTION

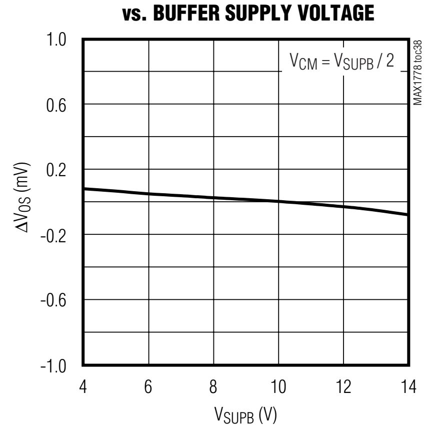


A. V_{LDO} = 2.5V, I_{LDO} = 200mA, 10mV/div
B. V_{MAIN} = V_{SUPL} = 8V, 200mV/div
C. I_{MAIN} = 0 TO 750mA, 500mA/div
FIGURE 7

INPUT OFFSET VOLTAGE DEVIATION vs. COMMON-MODE VOLTAGE



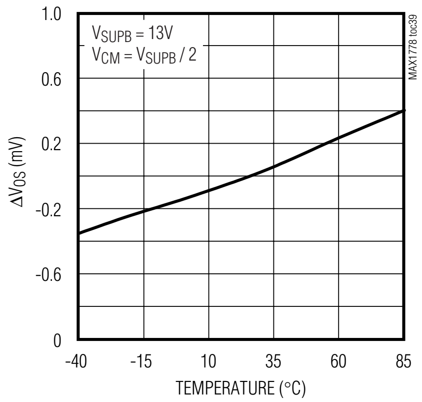
INPUT OFFSET VOLTAGE DEVIATION vs. BUFFER SUPPLY VOLTAGE



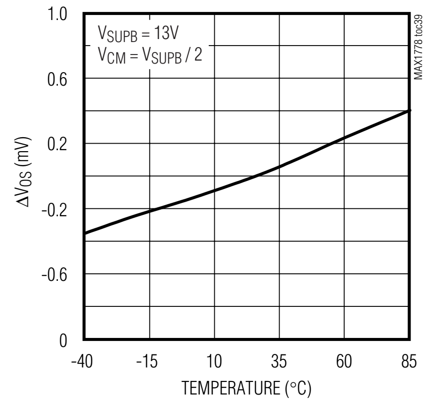
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

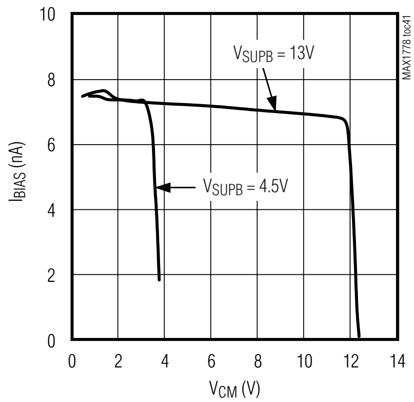
INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE



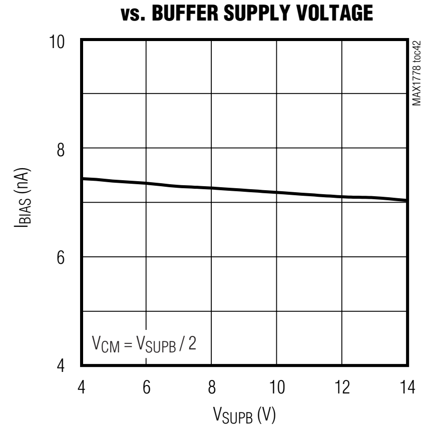
INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE



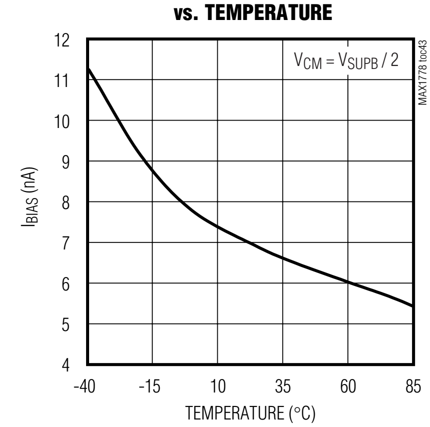
BUFFER INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



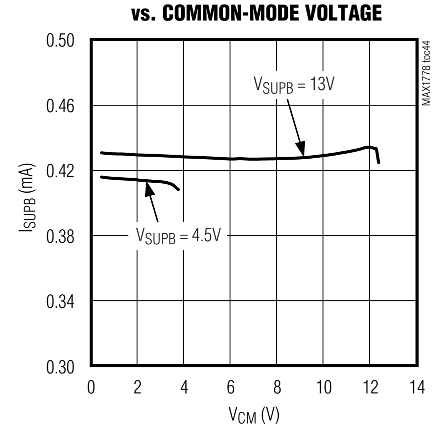
BUFFER INPUT BIAS CURRENT vs. BUFFER SUPPLY VOLTAGE



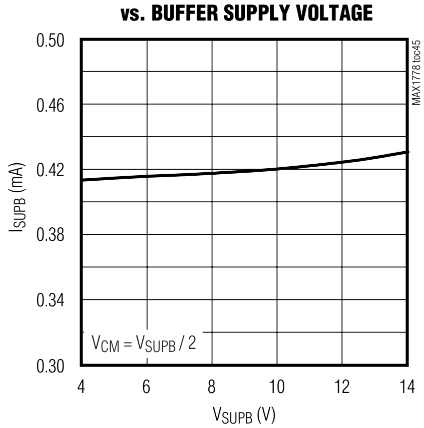
BUFFER INPUT BIAS CURRENT vs. TEMPERATURE



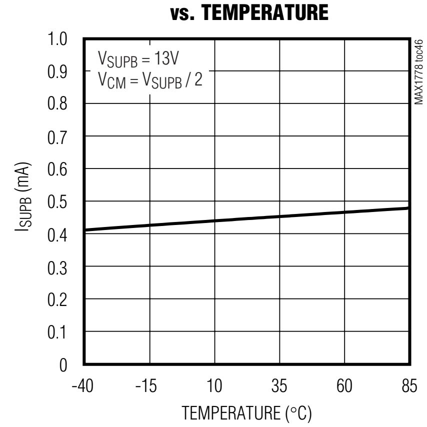
BUFFER SUPPLY CURRENT vs. COMMON-MODE VOLTAGE



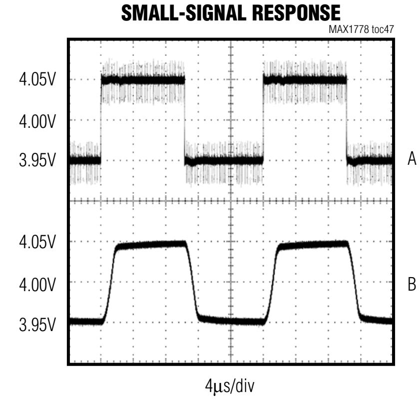
BUFFER SUPPLY CURRENT vs. BUFFER SUPPLY VOLTAGE



NO-LOAD BUFFER SUPPLY CURRENT vs. TEMPERATURE



VCOM BUFFER SMALL-SIGNAL RESPONSE



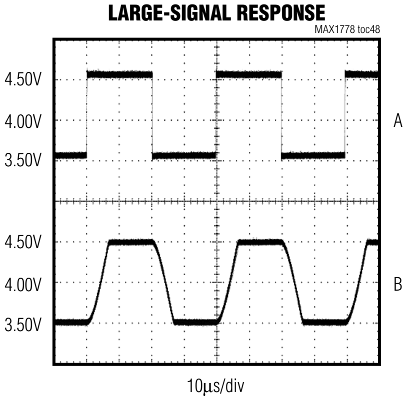
A. V_{BUF+} = 3.95V TO 4.05V, 50mV/div
B. BUFOUT = BUF-, 50mV/div
C_{BUF} = 1μF, V_{SUPB} = 8V

Quad-Output TFT LCD DC-DC Converters with Buffer

Typical Operating Characteristics (continued)

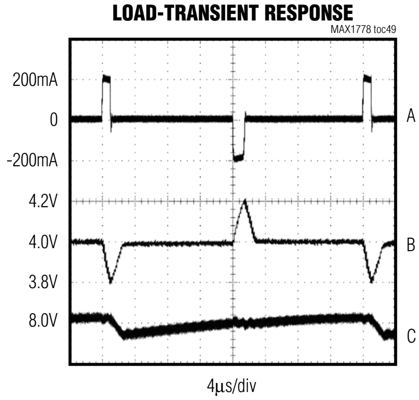
(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

VCOM BUFFER LARGE-SIGNAL RESPONSE



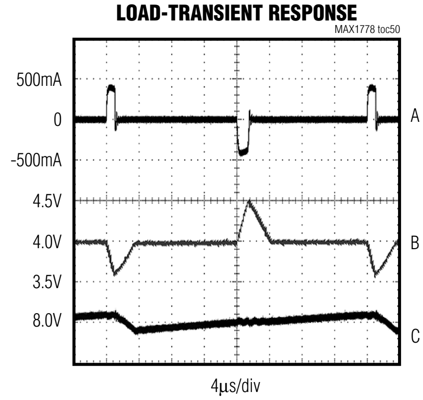
A. V_{BUF+} = 3.50V TO 4.50V, 0.5V/div
B. BUFOUT = BUF-, 0.5V/div
C_{BUF} = 1μF, V_{SUPB} = 8V

VCOM BUFFER LOAD-TRANSIENT RESPONSE



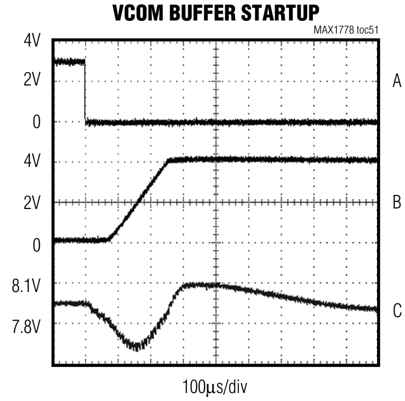
A. I_{BUFOUT} = 200mA PULSES, 200mA/div
B. BUFOUT = BUF-, 200mV/div
C. V_{MAIN} = 8V, 50mV/div
V_{SUPB} = V_{MAIN}, BUF+ = GND, C_{BUF} = 1μF

VCOM BUFFER LOAD-TRANSIENT RESPONSE



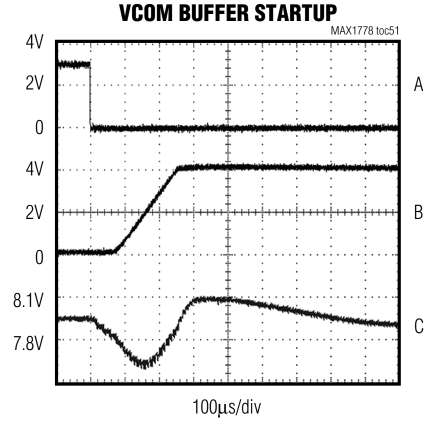
A. I_{BUFOUT} = 400mA PULSES, 500mA/div
B. BUFOUT = BUF-, 0.5V/div
C. V_{MAIN} = 8V, 100mV/div
V_{SUPB} = V_{MAIN}, BUF+ = GND, C_{BUF} = 1μF

VCOM BUFFER STARTUP



A. $\overline{RDY}$, 2V/div
B. BUFOUT = BUF-, C_{BUF} = 1μF, 2V/div
C. V_{SUPB} = V_{MAIN} = 8V, I_{MAIN} = 20mA, 200mV/div
BUF+ = GND

VCOM BUFFER STARTUP



A. $\overline{RDY}$, 2V/div
B. BUFOUT = BUF-, C_{BUF} = 1μF, 2V/div
C. V_{SUPB} = V_{MAIN} = 8V, I_{MAIN} = 20mA, 200mV/div
BUF+ = GND

Pin Description

PIN				NAME	FUNCTION
MAX1778 MAX1881	MAX1880 MAX1882	MAX1883 MAX1884	MAX1885		
1	1	1	1	FB	Main Step-Up Regulator Feedback Input. Regulates to 1.25V nominal. Connect a resistive divider from the output (V_{MAIN}) to FB to analog ground (GND).
2	2	2	2	INTG	Main Step-Up Integrator Output. When using the integrator, connect 1000pF to analog ground (GND). To disable the integrator, connect INTG to REF.
3	3	3	3	IN	Main Supply Voltage. The supply voltage powers the control circuitry for all of the regulators and may range from 2.7V to 5.5V. Bypass with a 0.1µF capacitor between IN and GND, as close to the pins as possible.
4	4	4	4	BUF+	VCOM Buffer (Operational Transconductance Amplifier) Positive Feedback Input. Connect to GND to select the internal resistive divider that sets the positive input to half the amplifier's supply voltage ($V_{BUF+} = V_{SUPB}/2$).
5	5	5	5	BUF-	VCOM Buffer (Operational Transconductance Amplifier) Negative Feedback Input
6	6	6	6	SUPB	VCOM Buffer (Operational Transconductance Amplifier) Supply Voltage
7	7	7	7	BUFOUT	VCOM Buffer (Operational Transconductance Amplifier) Output
8	8	8	8	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
9	9	9	9	REF	Internal Reference Bypass Terminal. Connect a 0.22µF ceramic capacitor from REF to analog ground (GND). External load capability up to 50µA.
10	10	–	–	FBP	Positive Charge-Pump Regulator Feedback Input. Regulates to 1.25V nominal. Connect a resistive divider from the positive charge-pump output (V_{POS}) to FBP to analog ground (GND).
11	11	–	–	FBN	Negative Charge-Pump Regulator Feedback Input. Regulates to 0V nominal. Connect a resistive divider from the negative charge-pump output (V_{NEG}) to FBN to the reference (REF).
12	12	10	10	$\overline{SHDN}$	Active-Low Shutdown Control Input. Pull $\overline{SHDN}$ low to force the controller into shutdown. If unused, connect $\overline{SHDN}$ to IN for normal operation. A rising edge on $\overline{SHDN}$ clears the fault latch.
13	–	11	–	SUPL	Low-Dropout Linear Regulator Input Voltage. Can range from 4.5V to 15V. Bypass with a 1µF capacitor to GND (see *Capacitor Selection and Regulator Stability*). Connect both input pins together externally.

Quad-Output TFT LCD DC-DC Converters with Buffer

Pin Description (continued)

PIN				NAME	FUNCTION
MAX1778 MAX1881	MAX1880 MAX1882	MAX1883 MAX1884	MAX1885		
14	–	12	–	LDOOUT	Linear Regulator Output. Sources up to 40mA. Bypass to GND with a ceramic capacitor determined by: $C_{LDOOUT} \geq 0.5ms \times \left(\frac{I_{LDOOUT(MAX)}}{V_{LDOOUT}}\right)$
15	–	13	–	FBL	Voltage Setting Input. Connect a resistive divider from the linear regulator output (V_{LDOOUT}) to FBL to analog ground (GND).
16	16	14	14	FLTSET	Fault Trip-Level Set Input. Connect to a resistive divider between REF and GND to set the main step-up converter's and positive charge pump's fault thresholds between 0.67 x V_{REF} and 0.85 x V_{REF}. Connect to GND for the preset fault threshold (0.9 x V_{REF}).
17	17	–	–	SUPN	Negative Charge-Pump Driver Supply Voltage. Bypass to power ground (PGND) with a 0.1µF capacitor.
18	18	–	–	DRVN	Negative Charge-Pump Driver Output. Output high level is V_{SUPN} and low level is PGND.
19	19	–	–	SUPP	Positive Charge-Pump Driver Supply Voltage. Bypass to power ground (PGND) with a 0.1µF capacitor.
20	20	–	–	DRVP	Positive Charge-Pump Driver Output. Output high level is V_{SUPP} and low level is PGND
21	21	17	17	PGND	Power Ground. Connect to analog ground (GND) underneath the IC.
22	22	18	18	LX	Main Step-Up Regulator Power MOSFET N-Channel Drain. Place output diode and output capacitor as close to PGND as possible.
23	23	19	19	TGND	Must be connected to ground.
24	24	20	20	$\overline{RDY}$	Active-Low, Open-Drain Output. Indicates all outputs are ready. On-resistance is 125Ω (typ).
–	13, 14, 15	15, 16	11, 12, 13, 15, 16	N.C.	No Connection. Not internally connected.

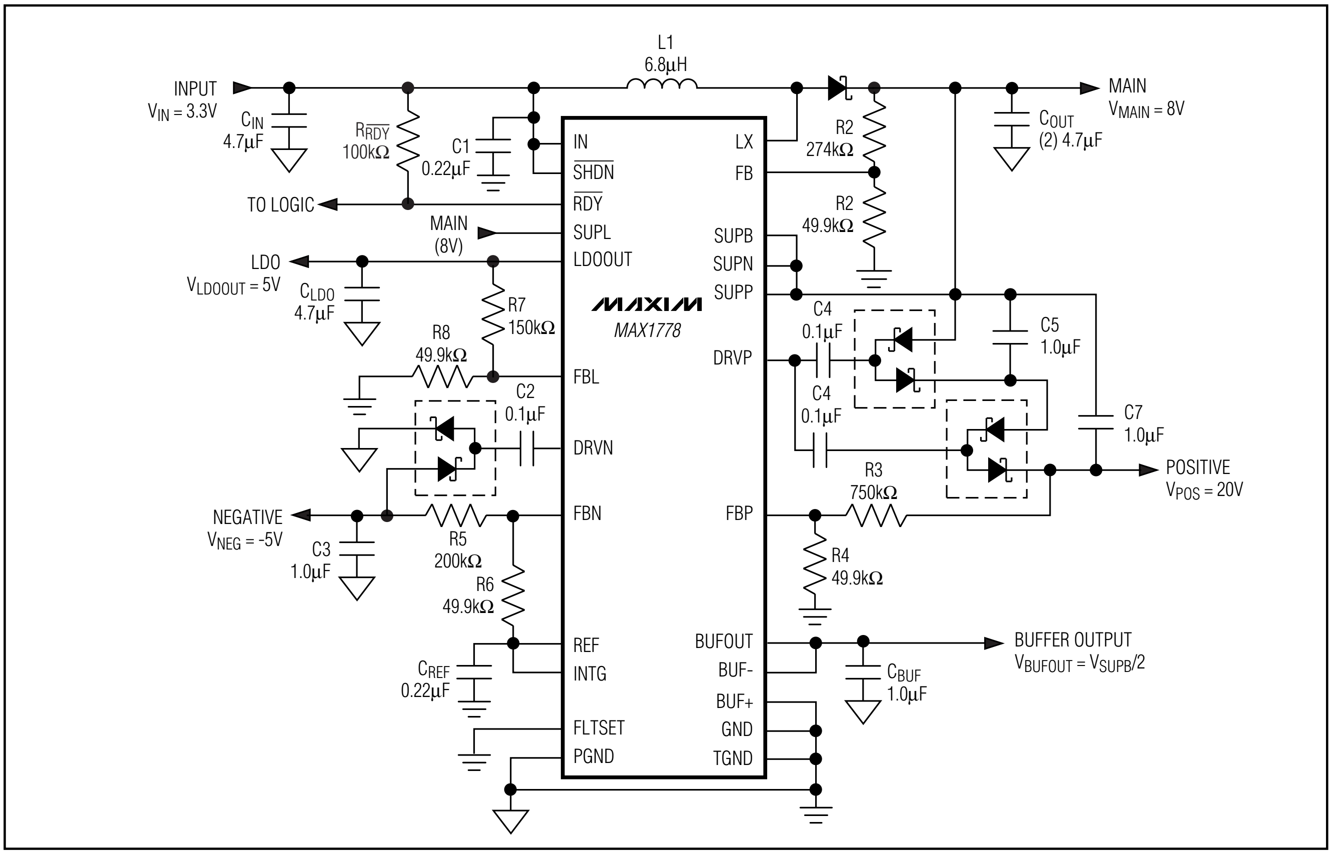


Figure 1. Typical Application Circuit

Detailed Description

The MAX1778/MAX1880–MAX1885 are highly efficient multiple-output power supplies for thin-film transistor (TFT) liquid crystal display (LCD) applications. The devices contain one high-power step-up converter, two low-power charge pumps, an operational transconductance amplifier (V_{COM} buffer), and a low-dropout linear regulator. The primary step-up converter uses an internal N-channel MOSFET to provide maximum efficiency and to minimize the number of external components. The output voltage of the main step-up converter (V_{MAIN}) can be set from V_{IN} to 13V with external resistors.

The dual charge pumps (MAX1778/MAX1880/MAX1881/MAX1882 only) independently regulate a positive output (V_{POS}) and a negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages from -40V to +40V. A unique control scheme minimizes output ripple as well as capacitor sizes for both charge pumps.

A resistor-programmable 40mA linear regulator (MAX1778/MAX1881/MAX1883/MAX1884 only) can provide preregulation or postregulation for any of the supplies. For higher current applications, an external transistor can be added.

Additionally, the V_{COM} buffer provides a high current output that is ideal for driving capacitive loads, such as the backplane of a TFT LCD panel. The positive feedback input features dual mode operation, allowing this input to be connected to an internal 50% resistive-divider between the buffer's supply voltage and ground, or externally adjusted for other voltages.

Also included in the MAX1778/MAX1880–MAX1885 is a precision 1.25V reference that sources up to 50µA, logic shutdown, soft-start, power-up sequencing, adjustable fault detection, thermal shutdown, and an active-low, open-drain ready output.

Main Step-up Controller

During normal pulse-width modulation (PWM) operation, the MAX1778/MAX1880–MAX1885 main step-up controllers switch at a constant frequency of 500kHz or 1MHz (see *Selector Guide*), allowing the use of low-profile inductors and output capacitors. Depending on the input-to-output voltage ratio, the controller regulates the output voltage and controls the power transfer by modulating the duty cycle (D) of each switching cycle:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

On the rising edge of the internal clock, the controller sets a flip-flop when the output voltage is too low, which turns on the N-channel MOSFET (Figure 2). The inductor current ramps up linearly, storing energy in a magnetic field. Once the sum of the feedback voltage error amplifier, slope-compensation, and current-feedback signals trip the multi-input comparator, the MOSFET turns off, the flip-flop resets, and the diode (D1) turns on. This forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and load. The MOSFET remains off for the rest of the clock cycle. Changes in the feedback voltage-error signal shift the switch-current trip level, consequently modulating the MOSFET duty cycle.

Under very light loads, an inherent switchover to pulse-skipping takes place (Figure 3). When this occurs, the controller skips most of the oscillator pulses in order to reduce the switching frequency and gate charge losses. When pulse-skipping, the step-up controller initiates a new switching cycle only when the output voltage drops too low. The N-channel MOSFET turns on, allowing the inductor current to ramp up until the multi-input comparator trips. Then, the MOSFET turns off and the diode turns on, forcing the inductor current to ramp down. When the inductor current reaches zero, the diode turns off, so the inductor stops conducting current. This forces the threshold between pulse-skipping and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation:

$$I_{LOAD(CROSSOVER)} \approx \frac{1}{2}\left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{f_{OSC} L}\right)$$

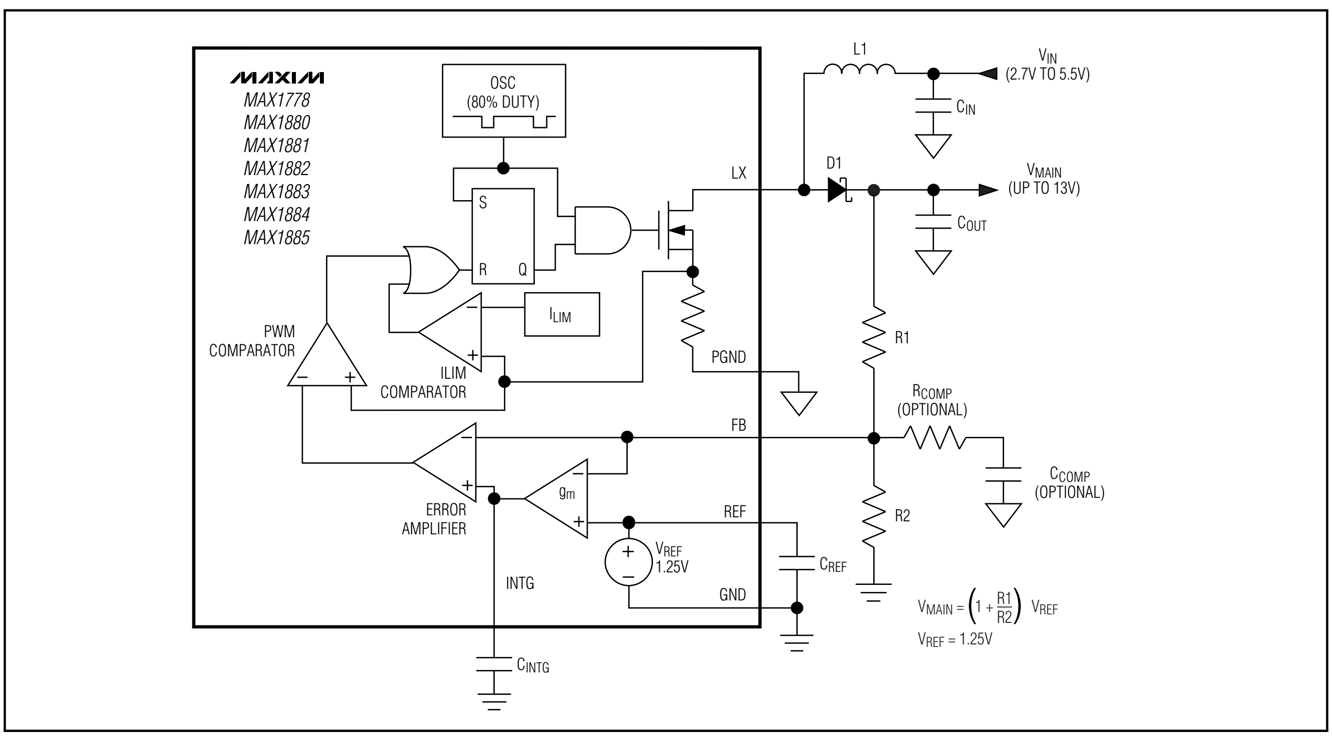


Figure 2. Main Step-Up Converter block Diagram

The switching waveforms will appear noisy and asynchronous when light loading causes pulse-skipping operation; this is a normal operating condition that improves light-load efficiency.

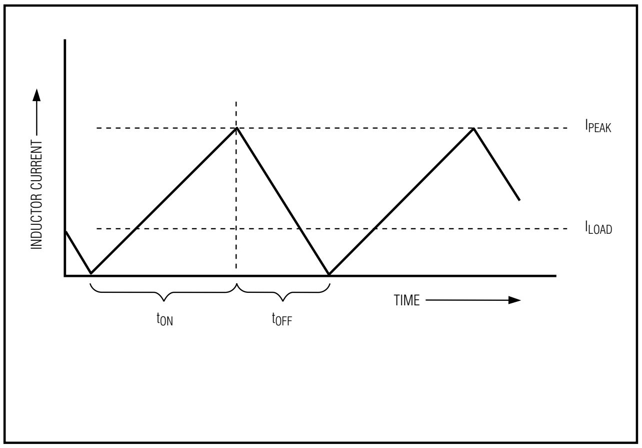


Figure 3. Discontinuous-to-Continuous Conduction Crossover Point

Dual Charge-Pump Regulator (MAX1778/ MAX1880/MAX1881/MAX1882 Only)

The MAX1778/MAX1880/MAX1881/MAX1882 controllers contain two independent low-power charge pumps (Figure 4). One charge pump inverts the input voltage and provides a regulated negative output voltage. The second charge pump doubles the input voltage and provides a regulated positive output voltage. The controllers contain internal P-channel and N-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant frequency (fCHP = fOSC/2).

Positive Charge Pump

During the first half-cycle, the N-channel MOSFET turns on and charges flying capacitor $C_{X(POS)}$ (Figure 4). This initial charge is controlled by the variable N-channel on-resistance. During the second half-cycle, the N-channel MOSFET turns off and the P-channel MOSFET turns on, level shifting $C_{X(POS)}$ by V_{SUPP} volts. This connects $C_{X(POS)}$ in parallel with the reservoir capacitor $C_{OUT(POS)}$. If the voltage across $C_{OUT(POS)}$ plus a diode drop (V_{POS} + V_{DIODE}) is smaller than the level-shifted flying capacitor voltage ($V_{CX(POS)}$ + V_{SUPP}), charge flows from $C_{X(POS)}$ to $C_{OUT(POS)}$ until the diode (D3) turns off.

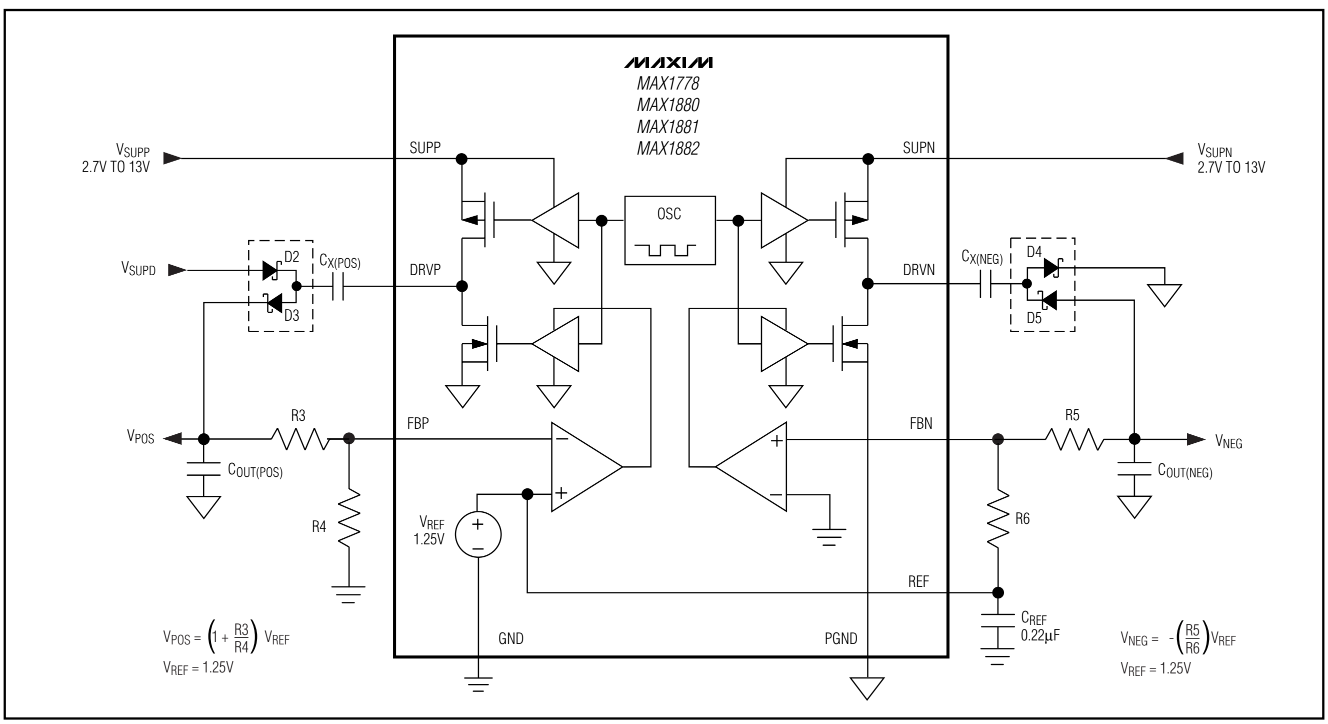


Figure 4. Low-Power Charge Pump Block Diagram

Quad-Output TFT LCD DC-DC Converters with Buffer

Negative Charge Pump

During the first half-cycle, the P-channel MOSFET turns on, and flying capacitor $C_{X(NEG)}$ charges to V_{SUPN} minus a diode drop (Figure 4). During the second half-cycle, the P-channel MOSFET turns off, and the N-channel MOSFET turns on, level shifting $C_{X(NEG)}$. This connects $C_{X(NEG)}$ in parallel with reservoir capacitor $C_{OUT(NEG)}$. If the voltage across $C_{OUT(NEG)}$ minus a diode drop is greater than the voltage across $C_{X(NEG)}$, charge flows from $C_{OUT(NEG)}$ to $C_{X(NEG)}$ until the diode (D5) turns off. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

Low-Dropout Linear Regulator (MAX1778/MAX1881/MAX1883/MAX1884 Only)

The MAX1778/MAX1881/MAX1883/MAX1884 contain a low-dropout linear regulator (Figure 5) that uses an internal PNP pass transistor (Q_P) to supply loads up to 40mA. As illustrated in Figure 5, the 1.25V reference is connected to the error amplifier, which compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is higher than the reference voltage, the controller lowers the base current of Q_P, which reduces the amount of current to the output. If the feedback voltage is too low, the device increases the pass transistor base current, which allows more current to pass to the output and increases the output voltage. However, the linear regulator also includes an output current limit to protect the internal pass transistor against short circuits.

The low-dropout linear regulator monitors and controls the pass transistor's base current, limiting the output current to 130mA (typ). In conjunction with the thermal overload protection, this current limit protects the output, allowing it to be shorted to ground for an indefinite period of time without damaging the part.

VCOM Buffer

The MAX1778/MAX1880–MAX1885 include a VCOM buffer, which uses an operational transconductance amplifier (OTA) to provide a current output that is ideal for driving capacitive loads, such as the backplane of a TFT LCD panel. The unity-gain bandwidth of this current-output buffer is:

$$GBW = gm/C_{OUT}$$

where gm is the amplifier's transconductance. The bandwidth is inversely proportional to the output capacitor, so large capacitive loads improve stability; however, lower bandwidth decreases the buffer's transient response time. To improve the transient response

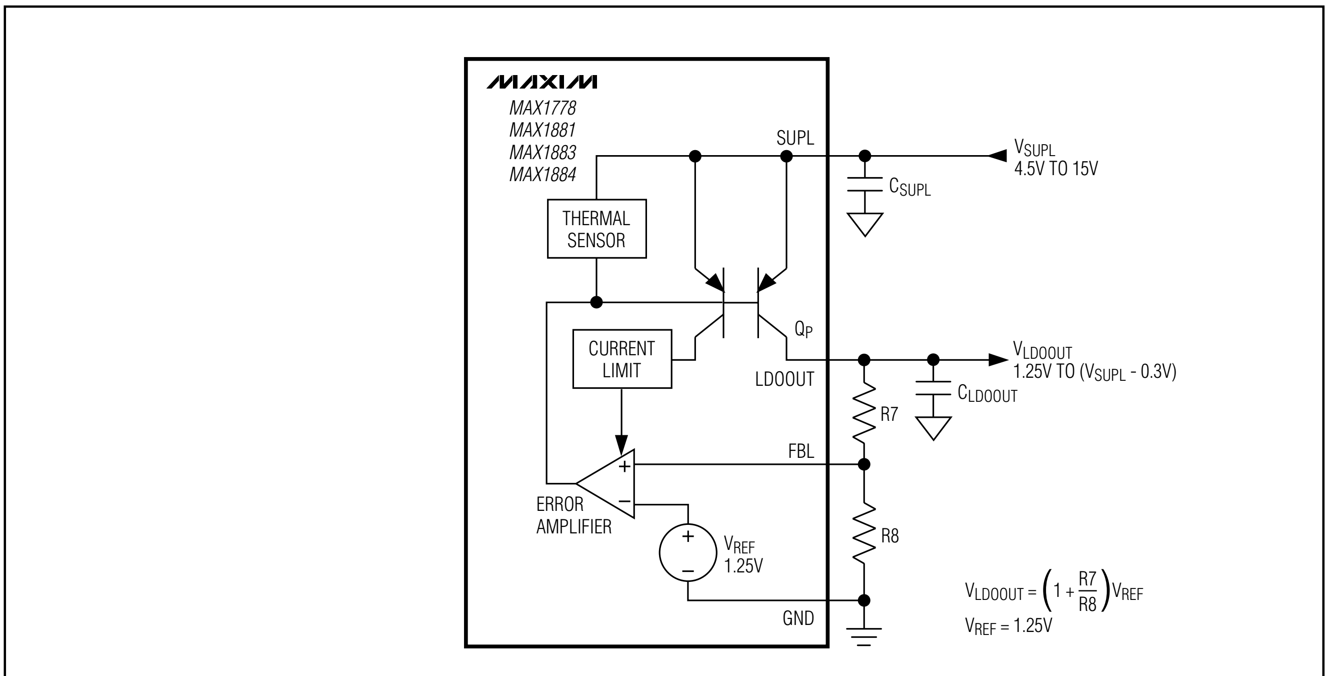


Figure 5. Low-Dropout Linear Regulator Block Diagram

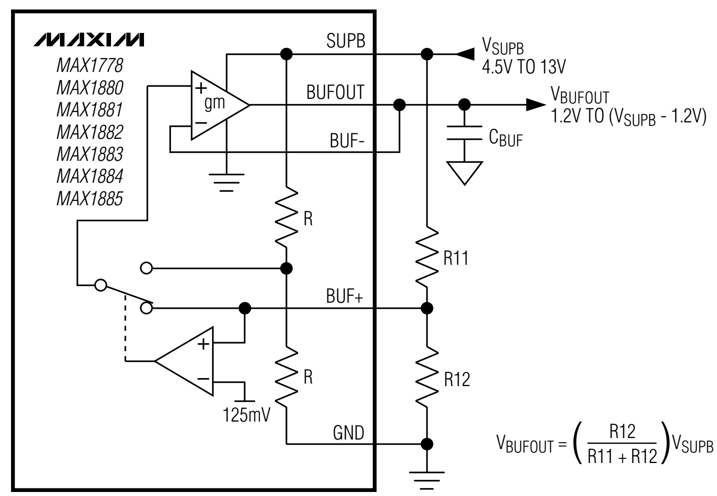


Figure 6. VCOM Buffer Block Diagram

times, the amplifier's transconductance increases as the output current increases (see *Typical Operating Characteristics*).

The VCOM buffer's positive feedback input features dual mode operation. The buffer's output voltage can be internally set by a 50% resistive divider connected to the buffer's supply voltage (SUPB), or the output voltage can be externally adjusted for other voltages.

Shutdown ($\overline{SHDN}$)

A logic-low level on $\overline{SHDN}$ shuts down all of the converters and the reference. When shut down, the supply current drops to 0.1µA to maximize battery life, and the reference is pulled to ground. The output capacitance, feedback resistors, and load current determine the rate at which each output voltage will decay. A logic-level high on $\overline{SHDN}$ power activates the MAX1778/MAX1880–MAX1885 (see Power-Up Sequencing). Do not leave $\overline{SHDN}$ floating. If unused, connect $\overline{SHDN}$ to IN. A logic-level transition on $\overline{SHDN}$ clears the fault latch.

Power-Up Sequencing

Upon power-up or exiting shutdown, the MAX1778/MAX1880–MAX1885 start a power-up sequence. First, the reference powers up. Then, the main DC-DC step-up converter powers up with soft-start enabled. The linear regulator powers up at the same time as the main step-up converter; however, the power sequence and ready output signal are not affected by the regulation of the linear regulator. While the main step-up converter powers up, the output of the PWM comparator remains low (Figure 2), and the step-up converter charges the output capacitors, limited only by the maximum duty cycle and current-limit comparator. When the step-up converter approaches its nominal regulation value and the PWM comparator's output changes states for the first time, the negative charge pump turns on. When the negative output voltage reaches approximately 90% of its nominal value (V_{FBN} < 110mV), the positive charge pump starts up. Finally, when the positive output voltage reaches 90% of its nominal value (V_{FBP} > 1.125V), the active-low ready signal ($\overline{RDY}$) goes low (see *Power Ready)*, and the VCOM buffer powers up. The MAX1883/MAX1884/MAX1885 do not contain the charge pumps, but the power-up sequence still contains the charge pumps' startup logic, which appears as a delay (2 × 4096/fOSC) between the step-up converter reaching regulation and when the ready signal and VCOM buffer are activated.

Soft-Start

For the main step-up regulator, soft-start allows a gradual increase of the current-limit level during startup to reduce input surge currents. The MAX1778/MAX1880–MAX1885 divide the soft-start period into four phases. During the first phase, the controller limits the current limit to only 0.38A (see *Electrical Characteristics*), approximately a quarter of the maximum current limit

($I_{LX(MAX)}$). If the output does not reach regulation within 1ms, soft-start enters phase II, and the current limit is increased by another 25%. This process is repeated for phase III. The maximum 1.5A (typ) current limit is reached within 3072 clock cycles or when the output reaches regulation, whichever occurs first (see the startup waveforms in the *Typical Operating Characteristics*).

For the charge pumps (MAX1778/MAX1880/MAX1881/MAX1882 only), soft-start is achieved by controlling the rate of rise of the output voltage. Both charge-pump output voltages are controlled to be in regulation within 4096 clock cycles, irregardless of output capacitance and load, limited only by the charge pump's output impedance. Although the MAX1883/MAX1884/MAX1885 controllers do not include the charge pumps, the soft-start logic still contains the 4096 clock cycle startup periods for both charge pumps.

Fault Trip Level (FLTSET)

The MAX1778/MAX1880–MAX1885 feature dual mode operation to allow operation with either a preset fault trip level or an adjustable trip level for the step-up converter and positive charge-pump outputs. Connect FLTSET to GND to select the preset $0.9 \times V_{REF}$ fault threshold. The fault trip level may also be adjusted by connecting a voltage divider from REF to FLTSET (Figure 8). For greatest accuracy, the total load on the reference (including current through the negative charge-pump feedback resistors) should not exceed 50µA so that VREF is guaranteed to be in regulation (see *Electrical Characteristics* Table). Therefore, select R10 in the 100kΩ to 1MΩ range, and calculate R9 with the following equation:

$$R9 = R10\,[(V_{REF} / V_{FLTSET}) - 1]$$

where V_{REF} = 1.25V, and V_{FLTSET} may range from 0.67 x V_{REF} to 0.85 x V_{REF}. FLTSET's input bias current has a maximum value of 50nA. For 1% error, the current through R10 should be at least 100 times the FLTSET input bias current (I_{FLTSET}).

Fault Condition

Once $\overline{RDY}$ is low, if the output of the main regulator or either low-power charge pump falls below its fault detection threshold, or if the input drops below its undervoltage threshold, then $\overline{RDY}$ goes high impedance and all outputs shut down; however, the reference remains active. After removing the fault condition, toggle shutdown (below 0.8V) or cycle the input voltage (below 0.2V) to clear the fault latch and reactivate the device.

The reference fault threshold is 1.05V. For the step-up converter and positive charge-pump, the fault trip level is set by FLTSET (see *Fault Trip Level*). For the negative charge pump, the fault threshold measured at the charge-pump's feedback input (FBN) is 140mV (typ).

Power Ready (RDY)

Power ready is an open-drain output. When the power-up sequence for the main step-up converter and low-power charge pumps has properly completed, the 14V MOSFET turns on and pulls $\overline{RDY}$ low with a 125Ω (typ) on-resistance. If a fault is detected on any of these three outputs, the internal open-drain MOSFET appears as a high impedance. Connect a 100kΩ pullup resistor between $\overline{RDY}$ and IN for a logic-level output.

Voltage Reference (REF)

The voltage at REF is nominally 1.25V. The reference can source up to 50µA with good load regulation (see Typical Operating Characteristics). Connect a 0.22µF ceramic bypass capacitor between REF and GND.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1778/MAX1880–MAX1885. When the junction temperature exceeds T_J = +160°C, a thermal sensor activates the fault protection, which shuts down the controller, allowing the IC to cool. Once the device cools down by 15°C, toggle shutdown (below 0.8V) or cycle the input voltage (below 0.2V) to clear the fault latch and reactivate the controller. Thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

The MAX1778/MAX1880–MAX1885s' maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of any airflow. The power dissipated in the device depends on the operating conditions of each regulator and the buffer.

The step-up controller dissipates power across the internal N-channel MOSFET as the controller ramps up the inductor current. In continuous conduction, the power dissipated internally can be approximated by:

$$P_{STEP-UP} \approx \left[\left(\frac{I_{MAIN} V_{MAIN}}{V_{IN}}\right)^2 + \frac{1}{12}\left(\frac{V_{IN} D}{f_{OSC} L}\right)^2\right] \times R_{DS(ON)} D$$

where I_{MAIN} includes the primary load current and the input supply currents for the charge pumps (see *Charge-Pump Input Power and Efficiency Considerations*), linear regulator, and VCOM buffer.

The linear regulator generates an output voltage by dissipating power across an internal pass transistor, so the power dissipation is simply the load current times the input-to-output voltage differential:

$$P_{LDO(INT)} = I_{LDO}(V_{SUPL} - V_{LDO})$$

When driving an external transistor, the internal linear regulator provides the base drive current. Depending on the external transistor's current gain (β) and the maximum load current, the power dissipated by the internal linear regulator may still be significant:

$$P_{LDO(INT)} = \frac{I_{LDO}}{\beta}\left[V_{SUPL} - \left(V_{LDO} + 0.7V\right)\right]$$
$$= I_{LDOOUT}(V_{SUPL} - V_{LDOOUT})$$

The charge pumps provide regulated output voltages by dissipating power in the low-side N-channel MOSFET, so they could be modeled as linear regulators followed by unregulated charge pumps. Therefore, their power dissipation is similar to a linear regulator:

$$P_{NEG} = I_{NEG}\left[(V_{SUPN} - 2V_{DIODE})N - V_{NEG}\right]$$
$$P_{POS} = I_{POS}\left[(V_{SUPP} - 2V_{DIODE})N + V_{SUPD} - V_{POS}\right]$$

where N is the number of charge-pump stages, V_{DIODE} is the diodes' forward voltage, and V_{SUPD} is the positive charge-pump diode supply (Figure 4).

The VCOM buffer's power dissipation depends on the capacitive load (C_{LOAD}) being driven, the peak-to-peak voltage change (V_{P-P}) across the load, and the load's switching rate:

$$P_{BUF} = V_{P-P}C_{LOAD}f_{LOAD}V_{SUPB}$$

To find the total power dissipated in the device, the power dissipated by each regulator and the buffer must be added together:

$$P_{TOTAL} = P_{STEP-UP} + P_{LDO(INT)}$$
$$+ P_{NEG} + P_{POS} + P_{BUF}$$

The maximum allowed power dissipation is 975mW (24-pin TSSOP) / 879mW (20-pin TSSOP) or:

$$P_{MAX} = (T_{J(MAX)} - T_A) / (\theta_{JB} + \theta_{BA})$$

where T_J - T_A is the temperature difference between the controller's junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package to the board, and θ_{BA} is the thermal resistance from the printed circuit board to the surrounding air.

Design Procedure

Main Step-Up Converter

Output Voltage Selection

Adjust the output voltage by connecting a voltage-divider from the output (VMAIN) to FB to GND (see Typical Operating Circuit). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equations:

$$R1 = R2\ [(V_{MAIN} / V_{REF}) - 1]$$

where V_{REF} = 1.25V. V_{MAIN} may range from V_{IN} to 13V.

Inductor Selection

Inductor selection depends upon the minimum required inductance value, saturation rating, series resistance, and size. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. For most applications, values between 4.7µH and 22µH work best with the controller's switching frequency (Tables 1 and 2).

The inductor value depends on the maximum output load the application must support, input voltage, output voltage, and switching frequency. With high inductor values, the MAX1778/MAX1880–MAX1885 source higher output currents, have less output ripple, and enter continuous conduction operation with lighter loads; however, the circuit's transient response time is slower. On the other hand, low-value inductors respond faster to transients, remain in discontinuous conduction operation, and typically offer smaller physical size for a given series resistance and current rating. The equations provided here include a constant LIR, which is the ratio of the peak-to-peak AC inductor current to the average DC inductor current. For a good compromise between the size of the inductor, power loss, and output voltage ripple, select an LIR of 0.3 to 0.5. The inductance value is then given by:

$$L_{MIN} = \left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right)^2\left(\frac{V_{MAIN} - V_{IN(MIN)}}{I_{MAIN(MAX)}f_{OSC}}\right)\left(\frac{1}{LIR}\right)\eta$$

where η is the efficiency, f_{OSC} is the oscillator frequency (see *Electrical Characteristics*), and I_{MAIN} includes the primary load current and the input supply currents for the charge pumps (see *Charge-Pump Input Power and Efficiency Considerations*), linear regulator, and VCOM buffer. Considering the typical application circuit, the maximum average DC load current ($I_{MAIN(MAX)}$) is 300mA with an 8V output. Based on the above equations and assuming 85% efficiency, the inductance value is then chosen to be 4.7µH.

The inductor's saturation current rating should exceed the peak inductor current throughout the normal operating range. The peak inductor current is then given by:

$$I_{PEAK} = \left(\frac{I_{MAIN(MAX)} V_{MAIN}}{V_{IN(MIN)}}\right)\left(1 + \frac{LIR}{2}\right)\left(\frac{1}{\eta}\right)$$

Under fault conditions, the inductor current may reach up to 1.85A ($I_{LIM(MAX)}$), see Electrical Characteristics). However, the controller's fast current-limit circuitry allows the use of soft-saturation inductors while still protecting the IC.

The inductor's DC resistance may significantly affect efficiency due to the power loss in the inductor. The power loss due to the inductor's series resistance (P_{LR}) may be approximated by the following equation:

$$P_{LR} \cong R_L\left(\frac{I_{MAIN} \times V_{MAIN}}{V_{IN}}\right)^2$$

where R_L is the inductor's series resistance. For best performance, select inductors with resistance less than the internal N-channel MOSFET on-resistance (0.35Ω typ).

Use inductors with a ferrite core or equivalent. To minimize radiated noise in sensitive applications, use a shielded inductor.

Output Capacitor

Output capacitor selection depends on circuit stability and output voltage ripple. A 10µF ceramic capacitor works well in most applications (Tables 1 and 2). Additional feedback compensation is required (see *Feedback Compensation*) to increase the margin for stability by reducing the bandwidth further. In cases where the output capacitance is sufficiently large, additional feedback compensation will not be necessary.

Output voltage ripple has two components: variations in the charge stored in the output capacitor with each LX pulse, and the voltage drop across the capacitor's equivalent series resistance (ESR) caused by the current into and out of the capacitor:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}, \text{ AND}$$

$$V_{RIPPLE(C)} \approx \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN}}\right)\left(\frac{I_{MAIN}}{C_{OUT} f_{OSC}}\right)$$

where I_{PEAK} is the peak inductor current (see Inductor Selection). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Feedback Compensation

For stability, add a pole-zero pair from FB to GND in the form of a compensation resistor (R_{COMP}) in series with a compensation capacitor (C_{COMP}) as shown in Figure 2. Select R_{COMP} to be half the value of R2, the low-side feedback resistor.

Integrator Capacitor

The MAX1778/MAX1880–MAX1885 contain an internal current integrator that improves the DC load regulation but increases the peak-to-peak transient voltage (see the load-transient waveforms in the *Typical Operating Characteristics*). For highly accurate DC load regulation, enable the current integrator by connecting a 470pF (f_{OSC} = 1MHz)/1000pF (f_{OSC} = 500kHz) capacitor to INTG. To minimize the peak-to-peak transient voltage at the expense of DC regulation, disable the integrator by connecting INTG to REF. When using the MAX1883/MAX1884/MAX1885, connect a 100kΩ resistor to GND when disabling the integrator.

Input Capacitor

The input capacitor (C_{IN}) in step-up designs reduces the current peaks drawn from the input supply and reduces noise injection. The value of C_{IN} is largely determined by the source impedance of the input supply. High source impedance requires high input capacitance, particularly as the input voltage falls. Since step-up DC-DC converters act as "constant-power" loads to their input supply, input current rises as input voltage falls. A good starting point is to use the same capacitance value for C_{IN} as for C_{OUT}.

Rectifier Diode

Use a Schottky diode with an average current rating equal to or greater than the peak inductor current, and a voltage rating at least 1.5 times the main output voltage (V_{MAIN}).

Charge Pumps (MAX1778/ MAX1880/ MAX1881/MAX1882 Only)

Selecting the Number of Charge-Pump Stages

The number of charge-pump stages required to regulate the output voltage depends on the supply voltage, output voltage, load current, switching frequency, the diode's forward voltage drop, and ceramic capacitor values.

For positive charge-pump outputs, the number of required stages may be determined by:

$$N_{POS} \geq \left(\frac{V_{POS} - V_{SUPD}}{V_{SUPP} - 1.1(2V_{DIODE} + R_{TX}I_{LOAD})} \right)$$

where V_{SUPD} is the positive charge-pump diode supply (Figure 4), V_{DIODE} is the diode's forward voltage drop, and R_{TX} is the charge pump's output impedance. The charge pump's output impedance may be approximated using the following equation:

$$R_{TX} = 2(R_{PCH(ON)} + R_{NCH(ON)}) + \left(\frac{1}{C_X f_{CHP}} \right) + \left(\frac{1}{C_{OUT} f_{CHP}} \right)$$

where the charge pump's switching frequency (f_{CHP}) is equal to 0.5 x f_{OSC}, the P-channel MOSFET's on-resistance ($R_{PCH(ON)}$) is 10Ω, and the N-channel MOSFET's on-resistance ($R_{NCH(ON)}$) is 4Ω (see *Electrical Characteristics*).

For negative charge pump outputs, the number of required stages may be determined by:

$$N_{NEG} \geq \left(\frac{V_{NEG}}{V_{SUPN} - 1.1(2V_{DROP} + R_{TX}I_{LOAD})} \right)$$

where N_{NEG} is rounded up to the nearest integer.

Table 1. MAX1778/MAX1880/MAX1883 Component Values (f_{OSC} = 1MHz)

	CIRCUIT #1	CIRCUIT #2	CIRCUIT #3	CIRCUIT #4	CIRCUIT #5
V_{IN}	3.3V	3.3V	3.3V	5V	5V
V_{MAIN}	9V	9V	9V	12V	12V
$I_{MAIN(MAX)}$	100mA	200mA	200mA	220mA	220mA
V_{NEG}	-5V	-5V	-5V	-5V	-5V
I_{NEG}	2mA	5mA	5mA	5mA	5mA
V_{POS}	24V	24V	24V	24V	24V
I_{POS}	2mA	5mA	5mA	5mA	5mA
L	2.2µH	4.7µH	4.7µH	6.8µH	6.8µH
I_{PEAK}	>1A	>1A	>1A	>1A	>1A
C_{OUT}	4.7µF	10µF	20µF	10µF	20µF
R1	309kΩ	309kΩ	309kΩ	429kΩ	429kΩ
R2	49.9kΩ	49.9kΩ	49.9kΩ	49.9kΩ	49.9kΩ
R_{COMP}	None	None	39kΩ*	None	20kΩ*
C_{COMP}	None	None	100pF*	None	200pF*

**R_{COMP} and C_{COMP} are connected between the step-up converter's output (V_{MAIN}) and FB.*

Table 2. MAX1881/MAX1882/MAX1884/MAX1885 Component Values (f_{OSC} = 500kHz)

	CIRCUIT #6	CIRCUIT #7	CIRCUIT #8	CIRCUIT #9
V_{IN}	3.3V	3.3V	3.3V	3.3V
V_{MAIN}	9V	9V	9V	9V
$I_{MAIN(MAX)}$	100mA	100mA	200mA	200mA
V_{NEG}	-5V	-5V	-5V	-5V
I_{NEG}	2mA	2mA	5mA	5mA
V_{POS}	24V	24V	24V	24V
I_{POS}	2mA	2mA	5mA	5mA
L	4.7µH	10µH	10µH	10µH
I_{PEAK}	>1A	>1A	>1A	>1A
C_{OUT}	4.7µF	10µF	10µF	20µF
R1	309kΩ	309kΩ	309kΩ	309kΩ
R2	49.9kΩ	49.9kΩ	49.9kΩ	49.9kΩ
R_{COMP}	None	None	None	20kΩ*
C_{COMP}	None	None	None	200pF*

**R_{COMP} and C_{COMP} are connected between the step-up converter's output (V_{MAIN}) and FB.*

Table 3. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coilcraft	847-639-6400	847-639-1469
Coiltronics	561-241-7876	561-241-9339
Sumida USA	847-956-0666	847-956-0702
Toko	847-297-0070	847-699-1194
CAPACITORS		
AVX	803-946-0690	803-626-3123
Kemet	408-986-0424	408-986-1442
Sanyo	619-661-6835	619-661-1055
Taiyo Yuden	408-573-4150	408-573-4159
DIODES		
Central Semiconductor	516-435-1110	516-435-1824
International Rectifier	310-322-3331	310-322-3332
Motorola	602-303-5454	602-994-6430
Nihon	847-843-7500	847-843-2798
Zetex	516-543-7100	516-864-7630

Charge-Pump Input Power and Efficiency Considerations

The charge pumps in the MAX1778/MAX1880/MAX1881/MAX1882 provide regulated output voltages by controlling the voltage drop across the low-side N-channel MOSFET, so they can be modeled as linear regulators followed by an unregulated charge pump when determining the input power requirements and efficiency.

The charge pump only provides charge to the output capacitor during half the period (50% duty cycle), so the input current is a function of the number of stages and the load current:

$$I_{SUPP} = I_{POS}(N+1)$$

for the positive charge pump, and:

$$I_{SUPP} = I_{POS}(N+1)$$

for the negative charge pump, where N is the number of charge pump stages.

The efficiency characteristics of the MAX1778/MAX1880/MAX1881/MAX1882 regulated charge pumps are similar to a linear regulator. It is dominated by quiescent current at low output currents and by the input voltage at higher output currents (see *Typical Operating Characteristics*). So the maximum efficiency may be approximated by:

$$\eta_{POS} \cong \frac{V_{POS}}{V_{SUPD} + V_{SUPP}N}$$

for the positive charge pump, and:

$$\eta_{NEG} \cong \frac{V_{NEG}}{V_{SUPN}N}$$

for the negative charge pump, where V_{SUPD} is the positive charge pump's diode supply (Figure 4).

Output Voltage Selection

Adjust the positive output voltage by connecting a voltage divider from the output (V_{POS}) to FBP to GND (see *Typical Operating Circuit*). Adjust the negative output voltage by connecting a voltage-divider from the output (V_{NEG}) to FBN to REF. Select R4 and R6 in the 50kΩ to 100kΩ range. Higher resistor values improve efficiency at low output current but increase output voltage error due to the feedback input bias current. For the negative charge pump, higher resistor values also reduce the load on the reference, which should not exceed 50µA for greatest accuracy (including current through the FLTSET resistors) to guarantee that V_{REF} remains in regulation (see Electrical Characteristics Table). Calculate the remaining resistors with the following equations:

$$R3 = R4\ [(V_{POS} / V_{REF}) - 1]$$

$$R5 = R6\ |V_{NEG} / V_{REF}|$$

where V_{REF} = 1.25V. V_{POS} may range from V_{SUPP} to 40V, and V_{NEG} may range from 0V to -40V.

Flying Capacitor

Increasing the flying capacitor (CX) value increases the output current capability. Above a certain point, increasing the capacitance has a negligible effect because the output current capability becomes dominated by the internal switch resistance and the diode impedance. The flying capacitor's voltage rating must exceed the following:

$$V_{CXN(POS)} > 1.5\left[V_{SUPD} + V_{SUPP}\ (N-1)\right]$$

for the positive charge pump, and:

$$V_{CXN(NEG)} > 1.5(V_{SUPN}N)$$

for the negative charge pump, where N is the stage number in which the flying capacitor appears, and V_{SUPD} is the positive charge pump's diode supply (Figure 4). For example, the two-stage positive charge pump in the typical application circuit (Figure 1) where V_{SUPP} = V_{SUPD} = 8V contains two flying capacitors. The flying capacitor in the first stage (C4) requires a voltage rating over 12V. The flying capacitor in the second stage (C6) requires a voltage rating over 24V.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq \frac{I_{LOAD}}{f_{CHP}V_{RIPPLE}}$$

where f_{CHP} is typically $f_{OSC}/2$ (see *Electrical Characteristics*).

Charge-Pump Input Capacitor

Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect directly to power ground (PGND).

Charge-Pump Rectifier Diodes

Use Schottky diodes with a current rating equal to or greater than two times the average charge-pump input current, and a voltage rating at least 1.5 times V_{SUPP} for the positive charge pump and V_{SUPN} for the negative charge pump.

Low-Dropout Linear Regulator (MAX1778/MAX1881/MAX1883/MAX1884 Only)

Output Voltage Selection

Adjust the linear-regulator output voltage by connecting a voltage-divider from LDOOUT to FBL to GND (Figure 5). Select R8 in the 5kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8\ [(V_{LDOOUT} / V_{FBL}) - 1]$$

where V_{FBL} = 1.25V, and V_{LDOOUT} may range from 1.25V to (V_{SUPL} - 300mV). FBL's input bias current is

Quad-Output TFT LCD DC-DC Converters with Buffer

0.8µA (max). For less than 0.5% error due to FBL input bias current (I_{FBL}), R8 must be less than 8kΩ.

Capacitor Selection and Regulator Stability

Capacitors are required at the input and output of the MAX1778/MAX1881/MAX1883/MAX1884 for stable operation over the full temperature range and with load currents up to 40mA. Connect a 1µF input bypass capacitor (C_{SUPL}) between SUPL and ground to lower the source impedance of the input supply. Connect a ceramic capacitor between LDOOUT and ground, using the following equation to determine the lowest value required for stable operation:

$$C_{LDOOUT} \geq 0.5ms \times \left(\frac{I_{LDOOUT(MAX)}}{V_{LDOOUT}}\right)$$

For example, with a 5V linear regulator output voltage and a maximum 40mA load, use at least 4µF of output capacitance. Applications that experience high-current load pulses may require more output capacitance.

The ESR of the linear regulator's output capacitor (C_{LDOOUT}) affects stability and output noise. Use output capacitors with an ESR of 0.1Ω or less to ensure stability and optimum transient response. Surface-mount ceramic capacitors are good for this purpose. Place C_{SUPL} and C_{LDOOUT} as close to the linear regulator as possible to minimize the impact of PC board trace inductance.

External Pass Transistor

For applications where the linear regulator currents exceed 40mA or where the power dissipation in the IC needs to be reduced, an external NPN transistor can be used. In this case, the internal LDO only provides the necessary base drive while the external NPN transistor supports the load, so most of the power dissipation occurs across the external transistor's collector and emitter.

Selection of the external NPN transistor is based on three factors: the package's power dissipation, the current gain (β), and the collector-to-emitter saturation voltage ($V_{CE(SAT)}$). First, the maximum power dissipation should not exceed the transistor's package rating:

$$P = (V_{COLLECTOR} - V_{LDO}) \times I_{LOAD(MAX)}$$

Once the appropriate package type is selected, consider the NPN transistor's current gain. Since the internal LDO cannot source more than 40mA (min), the transistor's current gain must be high enough at the lowest collector-to-emitter voltage to support the maximum output load:

$$\beta_{MIN} \geq \frac{I_{LOAD(MAX)} - 40mA}{40mA}$$

For stable operation, place a capacitor (C_{LDOOUT}) and a minimum load resistor (R5) at the output of the internal linear regulator (the base of the external transistor) to set the dominant pole:

$$C_{LDOOUT} \geq 0.5ms\left(\frac{1}{V_{LDO}}\right) \times \left(\frac{V_{LDO} + 0.7V}{R5} + \frac{I_{LOAD(MAX)}}{\beta_{MIN}}\right)$$

Since the LDO cannot sink current, a minimum pull-down resistor (R5) is required at the base of the NPN transistor to sink leakage currents and improve the high-to-low load-transient response. Under no-load conditions, leakage currents from the internal pass transistor supply the output capacitor (C_{LDOOUT}), even when the transistor is off. As the leakage currents increase over temperature, charge may build up on C_{LDOOUT}, making the linear regulator's output rise above its set point. Therefore, R5 must sink at least 100µA to guarantee proper regulation. Additionally, the minimum load current provided by R5 improves the high-to-low load transients by lowering the impedance seen by C_{LDOOUT} after the transient occurs. Therefore, if large load transients are expected, select R5 so that the minimum load current is 10% of the transistor's maximum base current:

$$R5 = \frac{V_{LDO} + 0.7V}{I_{LDOOUT(MIN)}} = 0.1\left[\frac{(V_{LDO} + 0.7V)\beta_{MIN}}{I_{LOAD(MAX)}}\right]$$

Alternatively, output capacitance placed on the external linear regulator's output (the emitter) adds a second pole that could destabilize the regulator. A capacitive-divider from the transistor's base to the feedback input (C2 and C3, Figure 7) circumvents this second pole by adding a pole-zero pair. Furthermore, to minimize excessive overshoot, the capacitive-divider's ratio must be the same as the resistive-divider's ratio. Once the output capacitor is selected, using the following equations to determine the required capacitive-divider values:

$$C2 + C3 \geq \frac{C_{LDO}}{100}\left(1 + \frac{R4}{R3}\right)$$

$$\frac{C2}{C2 + C3} = \frac{R4}{R3 + R4} = \frac{V_{REF}}{V_{LDO}}$$

Input-Output (Dropout) Voltage and Startup

A linear regulator's minimum input-to-output voltage differential (dropout voltage) determines the lowest useable supply voltage. Because the MAX1778/MAX1881/MAX1883/MAX1884 use an internal PNP transistor (or external NPN transistor), their dropout voltage is a function of the transistor's collector-to-emitter saturation voltage (see *Typical Operating Characteristics*). The linear regulator's quiescent current increases when in dropout.

The internal linear regulator will try to start up once its supply voltage (V_{SUPL}) exceeds 4V. When the linear regulator powers up, the linear regulator may be in dropout if the linear regulator's output set voltage is higher than its input supply voltage. Therefore, during this brief period, the linear regulator draws additional supply current until the input supply voltage exceeds the output set voltage plus the pass transistor's saturation voltage ($V_{LDO(SET)} + V_{CE(SAT)}$).

VCOM Buffer (Operational Transconductance Amplifier)

Buffer Output Voltage and Capacitor Selection

The positive input (BUF+) features dual mode operation. Connect BUF+ to GND for the preset VSUPB/2 output voltage, set by an internal 50% resistive-divider. Adjust the amplifier's output voltage by connecting a voltage-divider from SUPB to BUF+ to GND (Figure 6). Select R12 in the 10kΩ to 100kΩ range. Calculate R11 with the following equation:

$$R11 = R12\left[\left(\frac{V_{SUPB}}{V_{BUF+}}\right) - 1\right]$$

where V_{SUPB} may range from 4.5V to 13V, and V_{BUF+} may range from 1.2V to (V_{SUPB} - 1.2V). Connect a minimum 1µF ceramic capacitor from BUFOUT to ground.

PC Board Layout and Grounding

Careful PC board layout is extremely important for proper operation. Follow the following guidelines for good PC board layout:

1) Place the main step-up converter output diode and output capacitor less than 0.2in (5mm) from the LX and PGND pins with wide traces and no vias.
2) Separate analog ground and power ground. The ground connections for the step-up converter's and charge pump's input and output capacitors should be connected to the power ground plane. The linear regulator's and VCOM buffer's input and output capacitors should be connected to a separate power-ground path, star-connected to the PGND pin to minimize voltage drops. When using multilayer boards, the top layer should contain the boost

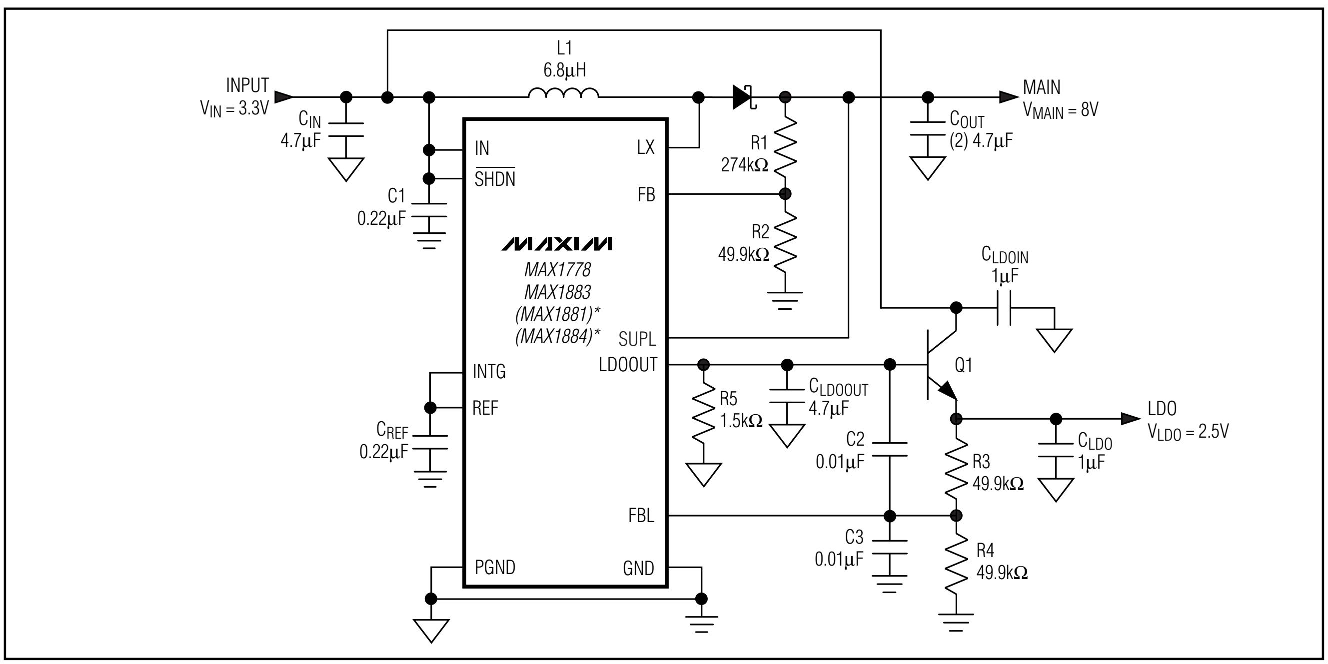


Figure 7. External Linear Regulator

regulator and charge-pump power ground plane, and the inner layer should contain the analog ground plane and power-ground plane/path for the V_{COM} buffer and LDO. Connect all three ground planes together at one place near the PGND pin.

3) Locate all feedback resistive-dividers as close to their respective feedback pins as possible. The voltage-divider's center trace should be kept short. Avoid running any feedback trace near the LX switching node or the charge-pump drivers. The resistive-dividers' ground connections should be to analog ground (GND).

4) When using multilayer boards, separate the top signal layer and bottom signal layer with a ground plane between to eliminate capacitive coupling between fast-charging nodes on the top layer and high-impedance nodes on the bottom layer. The fast-charging nodes, such as the LX and charge-pump driver nodes, should not have any other traces or ground planes near by.

5) Keep the charge-pump circuitry as close to the IC as possible, using wide traces and avoiding vias when possible. Place 0.1µF ceramic bypass capacitors near the charge-pump input pins (SUPP and SUPN) to the PGND pin.

6) To maximize output power and efficiency and minimize output ripple voltage, use extra wide, power ground traces, and solder the IC's power ground pin directly to it.

Refer to the MAX1778/MAX1880-MAX1885 evaluation kit for an example of proper board layout.

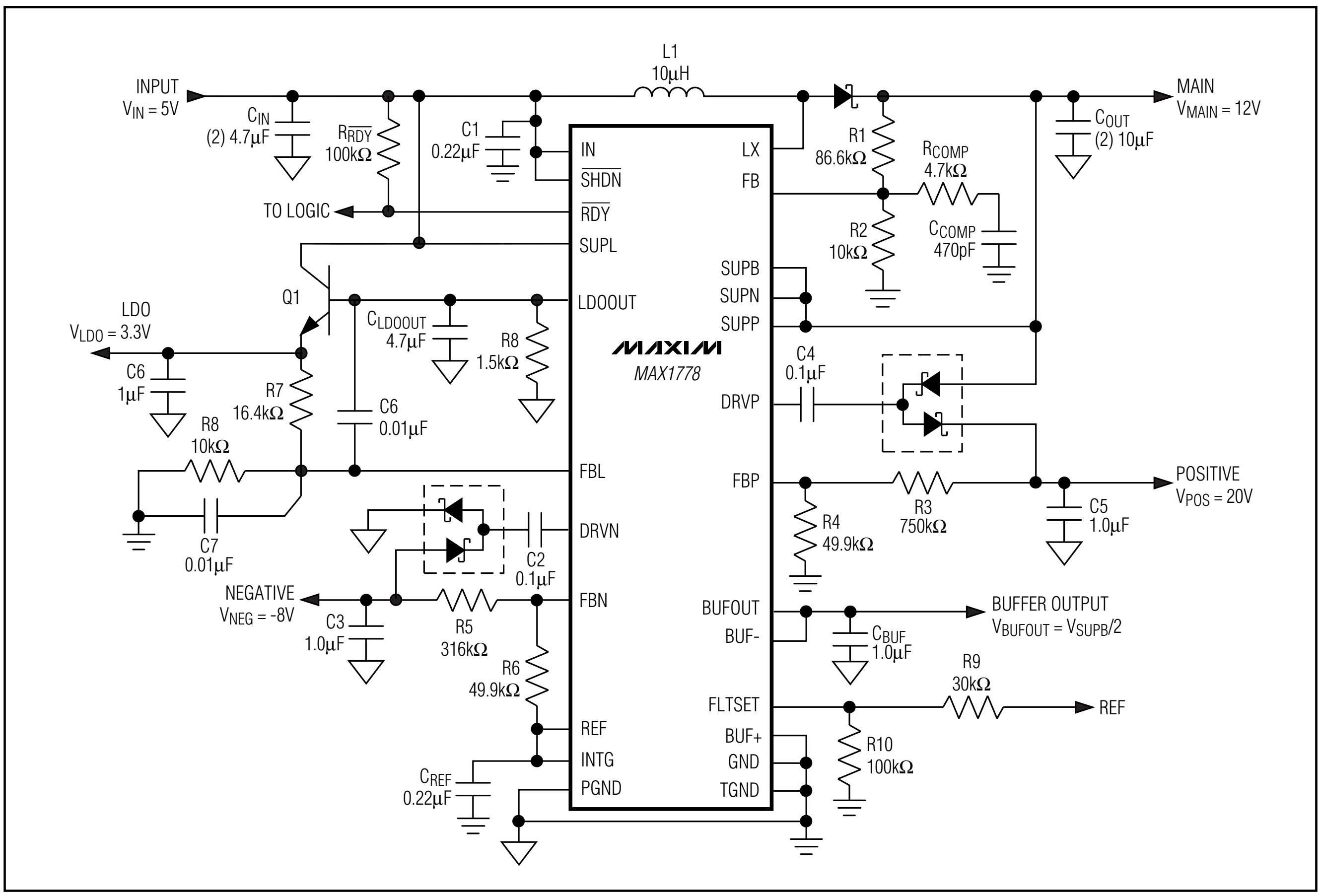


Figure 8. 5V Input Monitor Application

Applications Information

Low-Profile Components

Notebook applications generally require low-profile components, potentially limiting the circuit's performance. For example, low-profile inductors typically have lower saturation ratings and more series resistance, limiting output current and efficiency. Low-profile capacitors have lower voltage ratings for a given capacitance value, so 3.3µF low-profile capacitors with voltage ratings greater than 10V were not available at the time of publication.

Desktop Monitors

Monitor applications do not have the same component height restrictions associated with laptops, allowing more flexibility in component selection (Figure 8). Larger output capacitors with higher voltage ratings allow configurations with output voltages above 10V. Additionally, physically larger inductors with less series resistance and higher saturation ratings provide more output current and higher efficiency.

Input Voltage Above and Below the Output Voltage

Combining the step-up converter and linear regulator as shown in Figure 9 provides output voltage regulation above and below the input voltage. Supplied by the step-up converter, the linear regulator output provides a constant output voltage (V_{LDO}). When the input voltage exceeds the main step-up converter's nominal output voltage, the controller stops switching but the linear regulator maintains the output voltage. When the input voltage drops below the output voltage, the step-up

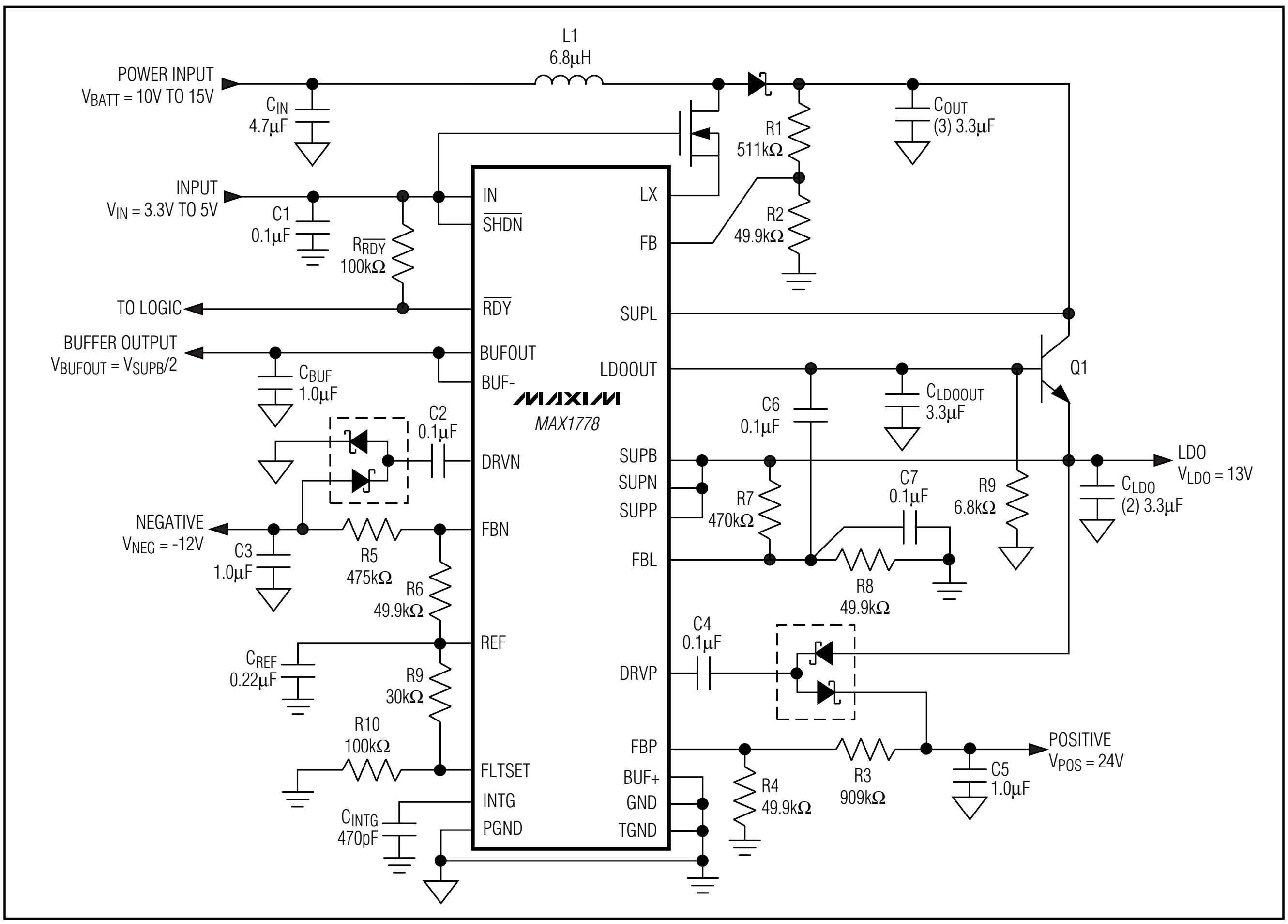


Figure 9. Input Voltage Above and Below the Output Voltage

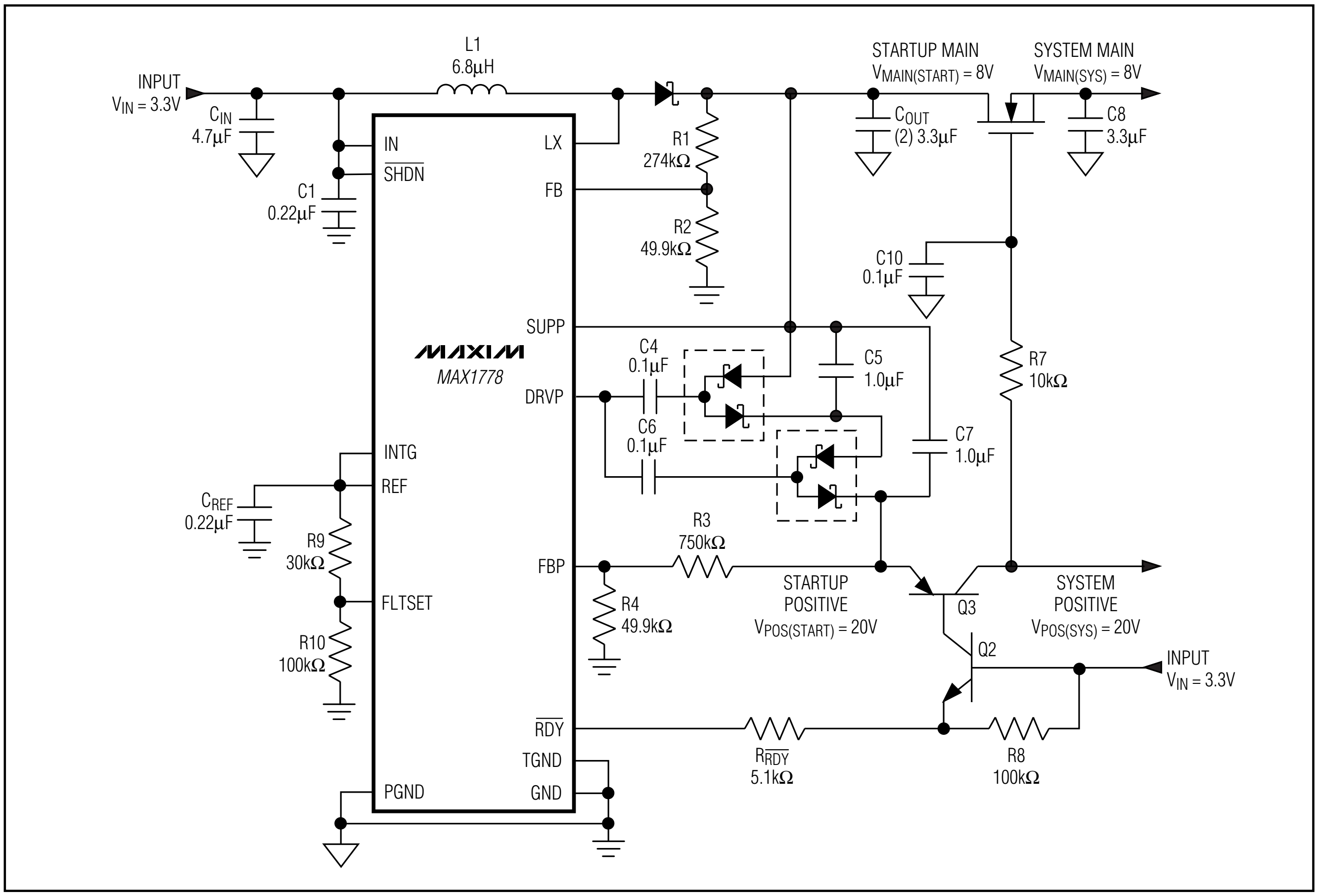


Figure 10. Power-Up Sequencing and Fault Protection;

converter steps up the input voltage so that the linear regulator will not drop out. Therefore, to guarantee that the external pass transistor does not saturate, the step-up converter's output voltage must be set above the linear regulator's output voltage plus the transistor's saturation rating ($V_{MAIN} \geq V_{LDO} + V_{SAT}$).

Power-Up Sequencing and Fault Protection

The MAX1778/MAX1880–MAX1885's fault protection cannot be activated until the power-up sequence is successfully completed and the power ready output goes low. Therefore, faults on the main output or positive charge-pump output could damage the controller or external components. Additional fault protection may be added as shown in Figure 10. The external MOSFET and PNP transistor isolate the positive outputs during startup. When the controller finishes the power-up sequence, the power-ready output goes low, turning on the PNP transistor. Any fault on the positive charge-pump output will pull down the charge pump's output voltage and trigger the fault protection; otherwise, the MOSFET's gate slow charges. Once the MOSFET turns on, any faults on the main step-up converter's output will pull down the main output voltage and trigger the fault protection.

VCOM Buffer Startup

The VCOM buffer does not include soft-start. Therefore, once the VCOM buffer turns on, it draws high surge currents while charging the output capacitance. In some applications, the buffer's high startup surge current could potentially trip the fault detection circuit, forcing the controller to shut down. In these cases, adding a soft-start resistive divider between SUPB and BUFOUT reduces the startup surge current and voltage drops associated with this load (Figure 11), as shown in

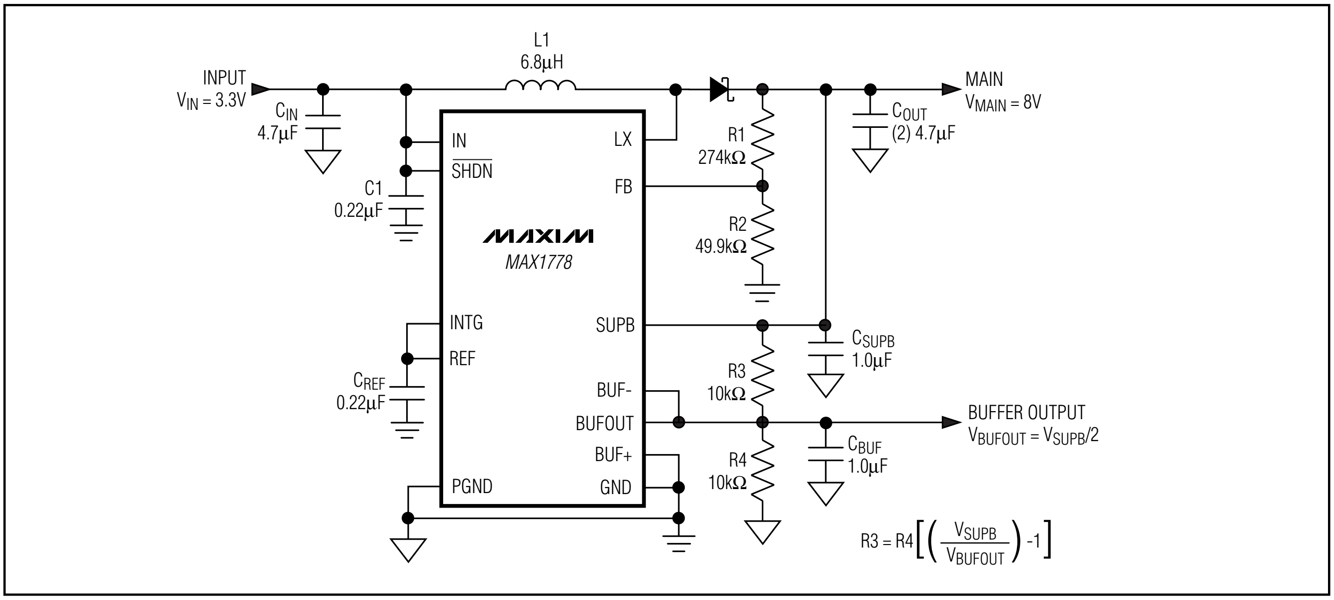


Figure 11. VCOM Buffer Soft-Start;

the *Typical Operating Characteristics*. Set the resistive divider to precharge BUFOUT, matching the buffer's output set voltage:

$$R3 = R4\left[\left(\frac{V_{SUPB}}{V_{BUFOUT}}\right) - 1\right]$$

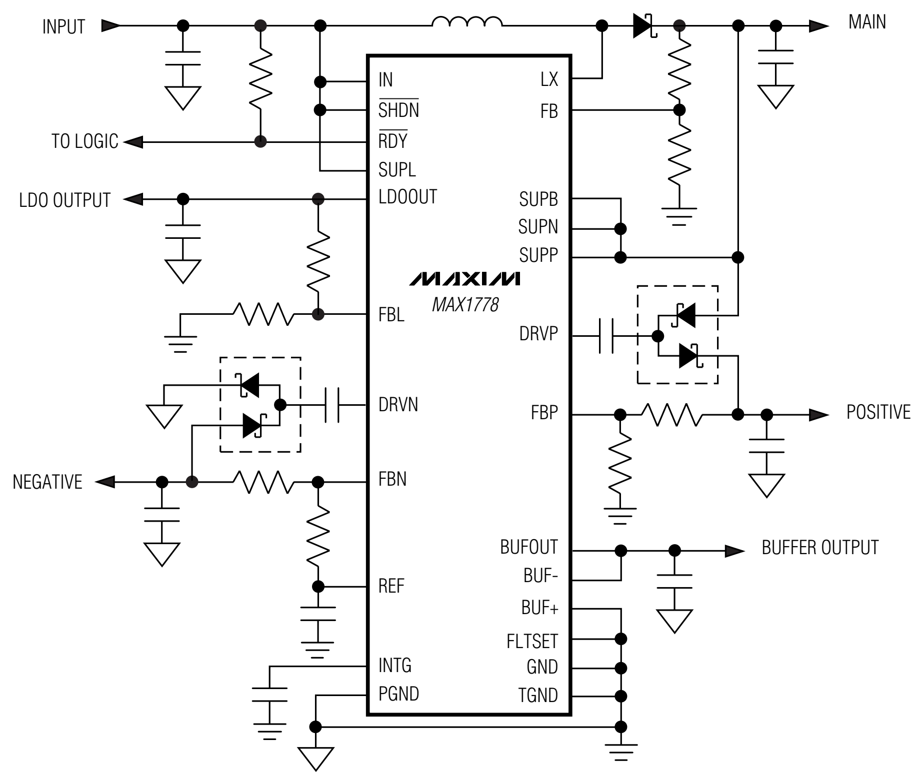
These resistor values are selected to charge the output capacitor close to the output set voltage before the buffer starts up:

$$C_{BUFOUT}(R3 \| R4) \approx \frac{5000}{f_{OSC}}$$

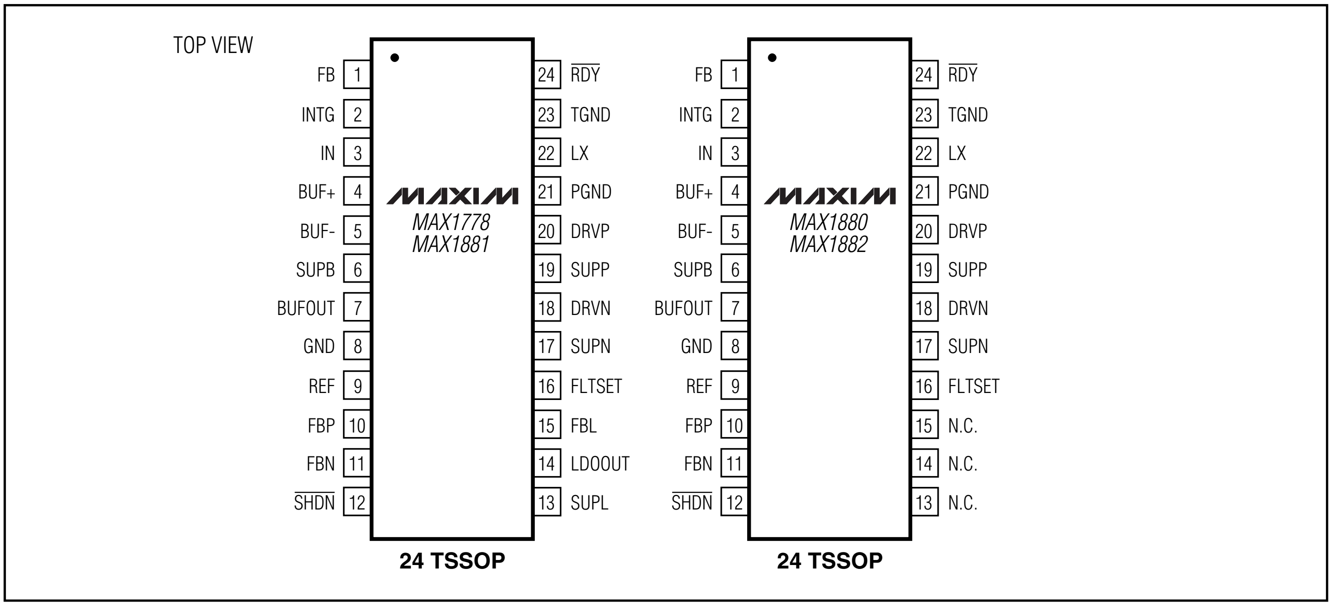
Selector Guide

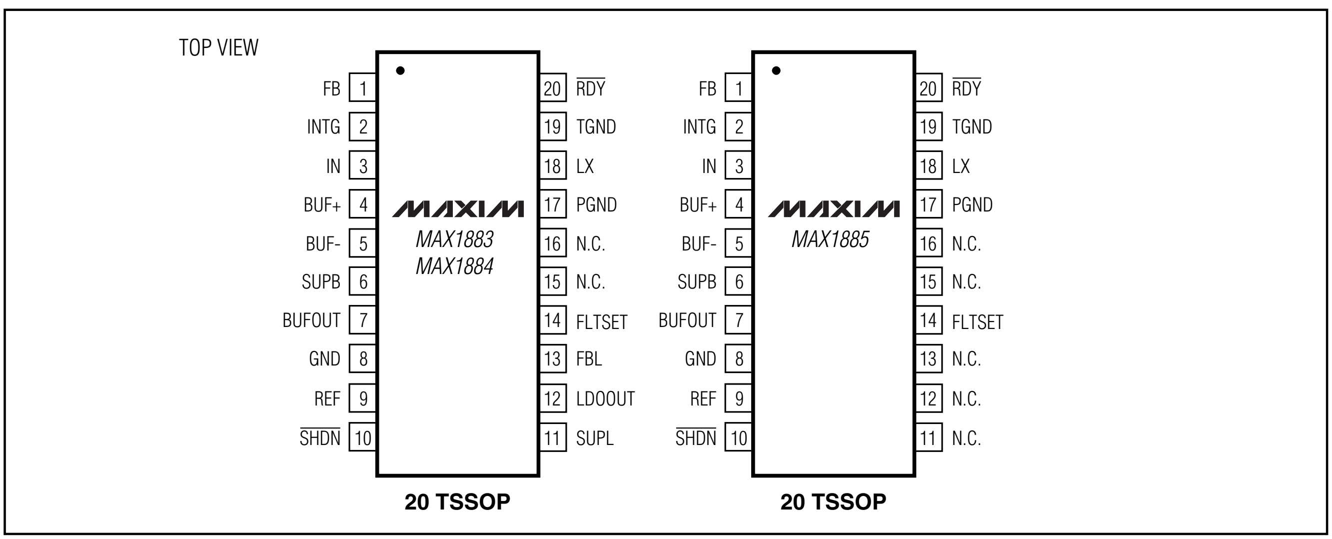
PART	STEP-UP SWITCHING FREQUENCY (Hz)	DUAL CHARGE PUMPS	LINEAR REGULATOR
MAX1778	1M	Yes	Yes
MAX1880	1M	Yes	No
MAX1881	500k	Yes	Yes
MAX1882	500k	Yes	No
MAX1883	1M	No	Yes
MAX1884	500k	No	Yes
MAX1885	500k	No	No

Typical Operating Circuit



Pin Configurations



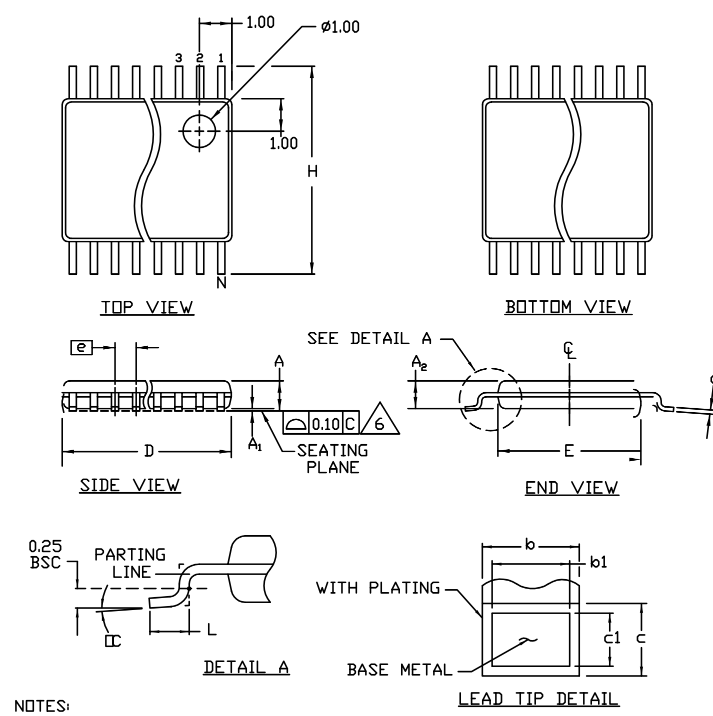


Chip Information

TRANSISTOR COUNT: 3739

Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV E | 1/1