High-Speed 12-Bit A/D Converters With External Reference Input

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V to V_{DD}+0.3V
AIN1, AIN2 to AGND ..... -15V to +15V
VREF to AGND ..... V_{SS}-0.3V to V_{DD}+0.3V
Digital Input Voltage to DGND
(CLKIN, CS, RD) ..... -0.3V to V_{DD}+0.3V
Digital Output Voltage to DGND
(D11-D0, BUSY, CLKOUT) ..... -0.3V to V_{DD}+0.3V

Power Dissipation to +75 C (any package) 1000mW
Derate above +75 C by ..... 10mW/ C
Operating Temperature Ranges:
MAX18_AC/BC ..... 0 C to +70 C
MAX18_AE/BE ..... -40 C to +85 C
MAX18_AM/BM ..... -55 C to +125 C
Storage Temperature ..... -65 C to +150 C
Lead Temperature (Soldering, 10 sec.) ..... +300 C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -10.8V to -16.5V; VREF = -5V; Slow Memory Mode; f_{CLK} = 4MHz for MAX183, f_{CLK} = 2.5MHz for MAX184, f_{CLK} = 1.25MHz for MAX185; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 2)							
Resolution	N			12			Bits
Integral Nonlinearity	INL	Tested range ±5V	MAX18_AC/AE			+1/2	LSB
			MAX18_AM T_A = +25 C			+1/2	
			MAX18_AM			+3/4	
			MAX18_B			+1	
Differential Nonlinearity	DNL	12-Bits, no missing codes over temp.				+0.9	LSB
Unipolar/Bipolar Offset Error			T_A = +25 C			+3	LSB
			T_A = T_{MIN} to T_{MAX}			+4	
					+2		ppm/ C
Unipolar/Bipolar Gain Error			T_A = +25 C			+4	LSB
			T_A = T_{MIN} to T_{MAX}			+6	
					±2		ppm/ C
Conversion Time	tCONV	Synchronous Clk (12.5 Clks)	MAX183			3.125	µs
			MAX184			5	
			MAX185			10	
		Asynchronous Clk (12 to 13 Clks)	MAX183	3.0		3.25	
			MAX184	4.8		5.2	
			MAX185	9.6		10.4	
ANALOG AND REFERENCE INPUTS							
Analog Input Current, AIN1 or AIN2		Unipolar input ranges 0V to +5V, 0V to +10V				3.5	mA
		Bipolar range ±5V				+1.75	
VREF Input Range (Note 3)				-5.1		-4.9	V
VREF Input Current						±3	µA
LOGIC INPUTS							
Input Low Voltage	V_{INL}	CS, RD, CLKIN				0.8	V
Input High Voltage	V_{INH}	CS, RD, CLKIN		2.4			V
Input Current	I_{IN}	CS, RD; V_{IN} = 0 to V_{DD}				+10	µA
		CLKIN; V_{IN} = 0 to V_{DD}				+20	
Input Capacitance (Note 3)	C_{IN}					10	pF

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V to V_{DD}+0.3V
AIN1, AIN2 to AGND ..... -15V to +15V
VREF to AGND ..... V_{SS}-0.3V to V_{DD}+0.3V
Digital Input Voltage to DGND
(CLKIN, CS, RD) ..... -0.3V to V_{DD}+0.3V
Digital Output Voltage to DGND
(D11-D0, BUSY, CLKOUT) ..... -0.3V to V_{DD}+0.3V

Power Dissipation to +75 C (any package) 1000mW
Derate above +75 C by ..... 10mW/ C
Operating Temperature Ranges:
MAX18 AC/BC ..... 0 C to +70 C
MAX18 AE/BE ..... -40 C to +85 C
MAX18 AM/BM ..... -55 C to +125 C
Storage Temperature ..... -65 C to +150 C
Lead Temperature (Soldering, 10 sec.) ..... +300 C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -10.8V to -16.5V; VREF = -5V; Slow Memory Mode; f_{CLK} = 4MHz for MAX183, f_{CLK} = 2.5MHz for MAX184, f_{CLK} = 1.25MHz for MAX185; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 2)							
Resolution	N			12			Bits
Integral Nonlinearity	INL	Tested range ±5V	MAX18 AC/AE			+1/2	LSB
			MAX18 AM T_A = +25 C			+1/2	
			MAX18 AM			+3/4	
			MAX18 B			+1	
Differential Nonlinearity	DNL	12-Bits, no missing codes over temp.				+0.9	LSB
Unipolar/Bipolar Offset Error			T_A = +25 C			+3	LSB
			T_A = T_{MIN} to T_{MAX}			+4	
					+2		ppm/ C
Unipolar/Bipolar Gain Error			T_A = +25 C			+4	LSB
			T_A = T_{MIN} to T_{MAX}			+6	
					±2		ppm/ C
Conversion Time	tCONV	Synchronous Clk (12.5 Clks)	MAX183			3.125	µs
			MAX184			5	
			MAX185			10	
		Asynchronous Clk (12 to 13 Clks)	MAX183	3.0		3.25	
			MAX184	4.8		5.2	
			MAX185	9.6		10.4	
ANALOG AND REFERENCE INPUTS							
Analog Input Current, AIN1 or AIN2		Unipolar input ranges 0V to +5V, 0V to +10V				3.5	mA
		Bipolar range ±5V				+1.75	
VREF Input Range (Note 3)				-5.1		-4.9	V
VREF Input Current						±3	µA
LOGIC INPUTS							
Input Low Voltage	V_{INL}	CS, RD, CLKIN				0.8	V
Input High Voltage	V_{INH}	CS, RD, CLKIN		2.4			V
Input Current	I_{IN}	CS, RD; V_{IN} = 0 to V_{DD}				+10	µA
		CLKIN; V_{IN} = 0 to V_{DD}				+20	
Input Capacitance (Note 3)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -10.8V to -16.5V; VREF = -5V, Slow Memory Mode: f_{CLK} = 4MHz for MAX183, f_{CLK} = 2.5MHz for MAX184, f_{CLK} = 1.25MHz for MAX185; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0, BUSY, CLK OUT; I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0, BUSY, CLK OUT; I_{SOURCE} = 200µA	4.0			V
Floating State Leakage Current	I_{LKG}	D11-D0; V_{OUT} = 0V to V_{DD}			±10	µA
Floating State Output Capacitance (Note 3)	C_{OUT}				15	pF
POWER REQUIREMENTS						
Supply Voltage (Note 1)	V_{DD}		4.75	5	5.25	V
	V_{SS}		-16.5	-12	-10.8	
Supply Current	I_{DD}	$\overline{CS}$ = RD = V_{DD}, AIN1 = AIN2 = 5V, BUSY = HIGH			7	mA
	I_{SS}				10	
Power Dissipation	PD	V_{DD} = +5V, V_{SS} = -12V		90	155	mW
Power-Supply Rejection, V_{DD} Only		FS Change, V_{SS} = -12V, V_{DD} = 4.75V to 5.25V		+1/4	±1	LSB
Power-Supply Rejection, V_{SS} Only		FS Change, V_{DD} = +5V, V_{SS} = -10.8V to -16.5V		+1/2	+1	LSB

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -10.8V to -16.5V; 100% production tested, T_A = T_{MIN} to T_{MAX}, unless otherwise indicated.) (Note 4, Figures 7, 9, 10)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX18 C/E			MAX18 M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CS to RD Setup Time (Note 3)	t1		0			0			0			ns
RD to BUSY Delay	t2	CL = 50pF		70	120			150			180	ns
Data Access Time (Note 5)	t3	CL = 100pF		50	100			130			150	ns
RD Pulse Width (Note 3)	t4		t3			t3			t3			ns
CS to RD Hold Time (Note 3)	t5		0			0			0			ns
Data Setup Time After BUSY (Note 5)	t6	CL = 100pF		40	70			90			100	ns
Bus Relinquish Time (Note 6)	t7			30	60			75			90	ns
Delay Between Read Operations	t8		200			200			200			ns
CLKIN to BUSY Delay (Note 3)	t9				120			150			180	ns
RD to CLKIN Setup/Hold Time (Notes 3, 7)	t10		25		100	25		100	25		100	ns

Note 1: Performance guaranteed over supply range by testing end-point errors (power-supply rejection) at the supply extremes.
Note 2: V_{DD} = +5V, V_{SS} = -12V, V_{REF} = -5V
Note 3: Guaranteed by design.
Note 4: All inputs are 0V to +5V swing with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 5: t3 and t6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross +0.8V or +2.4V.
Note 6: t7 is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 2.
Note 7: For predictable conversion times, RD to CLKIN falling edge must be outside this window.

High-Speed 12-Bit A/D Converters With External Reference Input

Pin Description

PIN	NAME	FUNCTION
1	AIN1	Analog Input
2	VREF	Voltage-Reference Input
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs. They are active when $\overline{CS}$ and $\overline{RD}$ are low. DB11 is the most significant bit.
12	DGND	Digital Ground
13-16	D3-D0	Three-State Data Outputs
17	CLKIN	Clock Input. Connect an external TTL-compatible clock to CLKIN. Alternatively, insert a crystal or ceramic resonator between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. When using an external clock, an inverted CLKIN signal appears on CLKOUT. See CLKIN description.
19	RD	READ Input. Along with $\overline{CS}$, this active low signal enables the three-state drivers and starts a conversion.
20	CS	CHIP SELECT. Along with $\overline{RD}$, this active low signal enables the three-state drivers and starts a conversion.
21	BUSY	$\overline{BUSY}$. Low while a conversion is in progress. $\overline{BUSY}$ indicates converter status.
22	V_{SS}	Negative Supply, -12V to -15V
23	V_{DD}	Positive Supply, +5V
24	AIN2	Analog Input

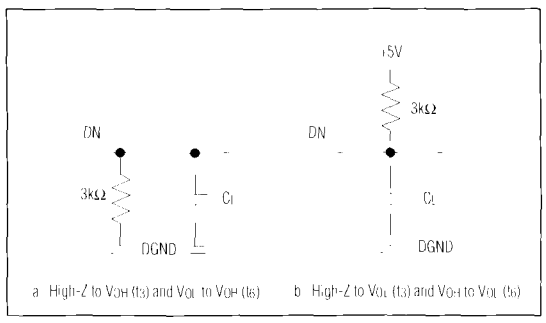


Figure 1. Load Circuits for Access Time

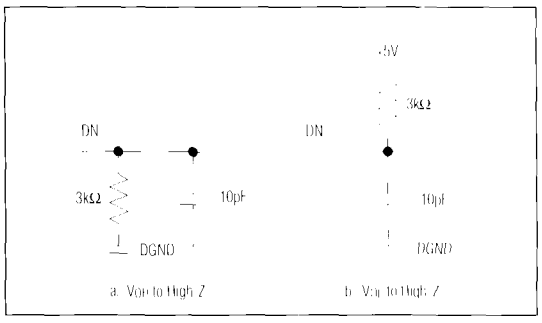
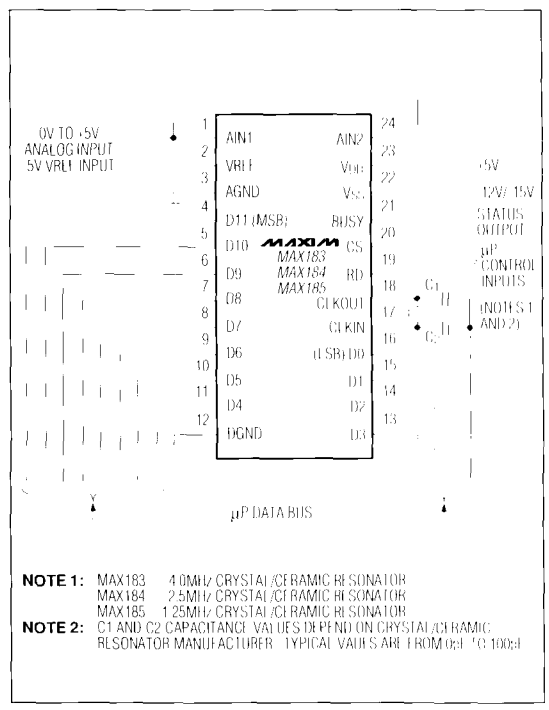


Figure 2. Load Circuits for Bus-Relinquish Time



NOTE 1: MAX183 4.0MHz CRYSTAL/CERAMIC RESONATOR
MAX184 2.5MHz CRYSTAL/CERAMIC RESONATOR
MAX185 1.25MHz CRYSTAL/CERAMIC RESONATOR

NOTE 2: C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 0pF TO 100pF.

Figure 3. MAX183/184/185 Operational Diagram

High-Speed 12-Bit A/D Converters With External Reference Input

Detailed Description

Converter Operation

The MAX183/184/185 use a successive approximation technique to convert an analog input to a 12-bit digital output code. The control logic provides easy interface to most µPs (Figure 3).

Figure 4 shows the MAX183/184/185 analog-equivalent circuit. The internal D/A converter (DAC) is controlled by a successive approximation register (SAR), has an output impedance of 2.5kΩ, and connects directly to the comparator input. The analog inputs AIN1 and AIN2 connect to the same comparator input through 5kΩ resistors.

A conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ and cannot be restarted after initiation. The $\overline{BUSY}$ output goes low when the conversion starts and can be used to control an external sample-and-hold when measuring wide bandwidth input signals.

The SAR is set, asynchronously with the clock input, to half scale when $\overline{CS}$ and $\overline{RD}$ go low. At the second falling edge of CLKIN (or rising edge of CLKOUT) following a conversion start, the output of the comparator is latched into the SAR most significant bit (MSB/D11) (Figure 5). The MSB is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (D10) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. At conversion end, following a falling CLKIN signal, $\overline{BUSY}$ goes high and the SAR result is latched into three-state output buffers.

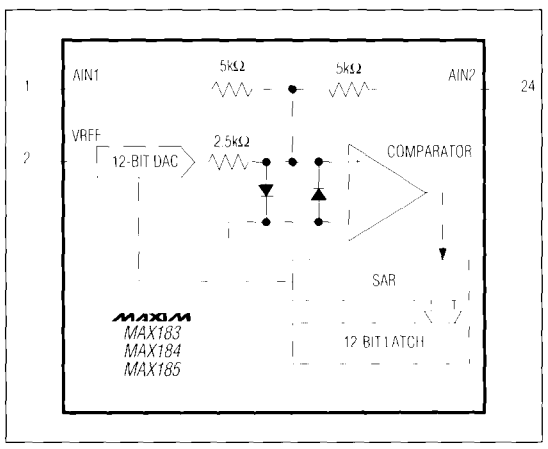


Figure 4. MAX183/184/185 AIN Inputs

Clock

Internal Clock Oscillator

Figure 6 shows the MAX183/184/185 clock circuitry. Minimize the capacitive load on the CLKOUT pin for low power dissipation and to avoid digital coupling of the CLKOUT buffer current to the comparator. CLKOUT should be left open if an external clock source is used to drive CLKIN. Connect a crystal/ceramic resonator between CLKOUT and CLKIN if the internal oscillator is used.

Control Inputs Synchronization

When RD is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). Use the following guidelines to ensure a fixed conversion time:

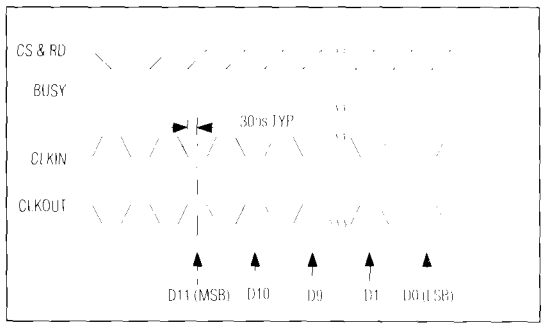


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN

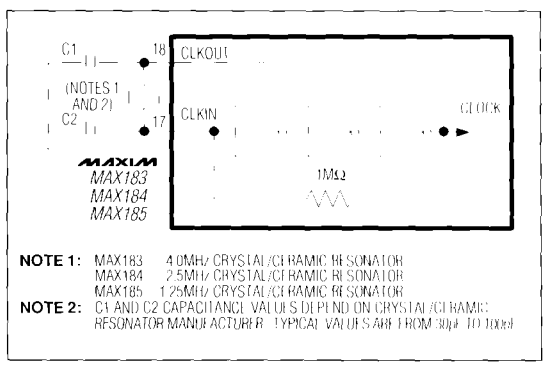


Figure 6. MAX183/184/185 Internal Clock Circuit

The MAX183/184/185 $\overline{RD}$ input should go low at the rising edge of CLKIN. In this case, the conversion lasts 12.5 clock cycles, and the conversion time is 3.125µs when f_{CLK} = 4MHz, 5µs when f_{CLK} = 2.5MHz, and 10µs when f_{CLK} = 1.25MHz. The delay from the falling edge of RD to the falling edge of CLKIN must not be less than 100ns to ensure the 12.5 clock cycle conversion time (Figure 7). This gives the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional 1/2 clock cycle of settling can be allowed for the sample-and-hold by having $\overline{RD}$ go low at the falling edge of CLKIN. This results in a 13 cycle conversion time (3.25µs, 5.2µs and 10.4µs).

Digital Interface

Timing and Control

CS and $\overline{RD}$ control conversion start and data-read operations. Figure 8 shows the logic equivalent for the conversion and the data-output control circuitry. A logic low at both inputs starts a conversion. Once a conversion is in progress, it cannot be restarted. The $\overline{BUSY}$ output remains low during the entire conversion cycle.

Figures 9 and 10 outline the two interface modes (slow memory and ROM). Slow memory mode is for µPs that can be forced into a wait state for periods as long as the MAX183/184/185 conversion time. ROM mode is for µPs that cannot be forced into a wait state. In both interface modes, a processor read operation to the ADC address starts the conversion. In the ROM mode, a second read operation accesses the conversion result.

Slow Memory Mode

The timing diagram in Figure 9 illustrates slow memory mode, which is designed for µPs with a wait state. CS and RD go low, triggering a conversion, and are kept low until the conversion is complete. BUSY responds by going low, and data from the previous conversion remains on the three-state data outputs. At conversion end, $\overline{BUSY}$ returns high, and the output latches transfer the new conversion results to the three-state data outputs. The µP completes the read operation by taking CS and RD high.

ROM Mode

The ROM mode avoids placing the µP into a wait state. A conversion begins with a read operation. While CS and $\overline{RD}$ are low, data from the last conversion is available on the data outputs. A second read operation reads the new data and begins the conversion process again. A delay at least as long as the MAX183/184/185 conversion times must be allowed between read operations. The data on the output bus is in a parallel format in either mode.

Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, coupling from the data pins to the ADC comparator may cause LSBs of error. Using slow memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, if the data bus is active during the conversion, use three-state drivers to isolate the bus from the ADC.

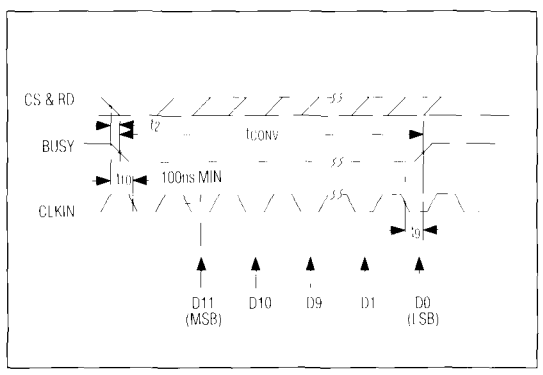


Figure 7. MAX183/184/185 $\overline{RD}$ and CLKIN for Synchronous Operation and Conversion Time of 12.5 Clock Cycles

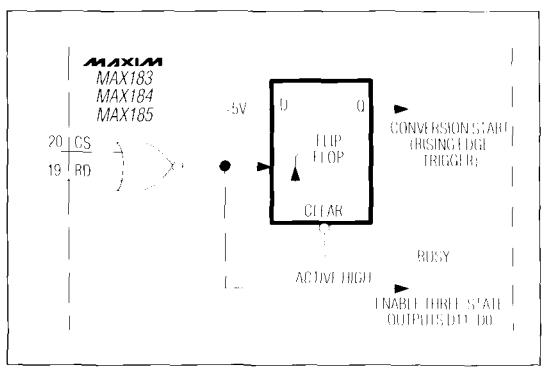


Figure 8. Logic for Control Inputs CS and RD Internal

ROM Mode

Digital noise is generated in the ADC when $\overline{RD}$ or CS go high, and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a bit decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than 1 clock cycle. In other words, the $\overline{RD}$ and $\overline{CS}$ low pulse should be less than 250ns for the MAX183, 400ns for the MAX184, and 1µs for the MAX185. If this cannot be done, the RD or CS signal must go high at a rising edge of CLKIN since the comparator output is always latched at falling edges of CLKIN.

Physical Layout

For best system performance, printed circuit boards should be used for the MAX183/184/185; wire-wrap boards are not recommended. Separate the digital- and analog-signal lines as much as possible in the board layout. Do not run analog and digital lines parallel to each other or digital lines underneath the MAX183/184/185 package.

Grounding

Figure 11 shows the recommended system ground connections. Establish a single-point analog ground (star ground), separate from the logic ground, at AGND of the MAX183/184/185. Connect all other analog grounds and DGND of the MAX183/184/185 to this star ground (no other digital grounds should be connected to this point). For noise-free operation of the ADC, use a low-impedance ground return to the power supply from this star ground.

Power-Supply Bypassing

The ADC's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog star ground with 0.1µF and 10µF bypass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10Ω-20Ω) resistor can be connected (Figure 11) to filter external noise.

Driving The Analog Input

The input signal leads to AIN and the input return leads to AGND should be as short as possible to minimize input noise coupling. Use shielded cables if the leads must be long. The input impedance at each AIN is typically 5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is needed since the analog input current is modulated at the clock rate during a conversion (up to 4MHz for MAX183, 2.5MHz for MAX184, or 1.25MHz for the MAX185). The output impedance of the driving amplifier is equal to its open-loop output impedance divided by the loop gain at the frequency of interest.

MAX184/185 The MAX184/185 maximum clock rate of 2.5MHz makes it possible to drive AIN with amplifiers like the OP42, AD711 or a Maxim OP27. A MAX400 or a Maxim OP07 can also be used up to 1.25MHz clock rate.

MAX183 – The MAX183, with a maximum 4MHz clock rate, might exhibit settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a Maxim OP27, an OP42, or an AD711 improves high-frequency output impedance.

Reference Input

VREF connects to an external -5V source. This may be either a precision negative reference, a positive reference (such as the MX584) connected as a two-terminal device to provide -5V (Figure 16), or an existing system reference. The allowed input range at REFIN is -5.1V to -4.9V. VREF (and AIN2 in bipolar input configuration) should be bypassed to ground with a 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.

If the external reference is biased from a power supply other than V_{SS}, then care must be taken to ensure that V_{SS} is applied to the ADC before VREF. If supply sequencing is in doubt, then connect a diode between V_{SS} and VREF, as shown in Figure 12. If the reference source is powered from the same supply as V_{SS}, then no diode is needed.

MAX183/184/185 to Sample-and-Hold Interface

The analog input to the ADC must be stable to within 1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input-signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX183. A sample-and-hold should be used for higher bandwidth signals.

The BUSY output from the MAX183/184/185 may be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. However, since the ADC's DAC is switched at approximately the same time as the BUSY signal goes low, sample-and-hold transients caused by DAC switching may result in code-dependent errors due to sample-and-hold aperture delay. Adding a NAND (inverted AND) gate ensures that the sample-and-hold is switched to the hold mode BEFORE any disturbances (Figures 13 and 14). The NAND gate solution works only if the width of the RD pulse is wider than the RD to BUSY delay in the MAX183/184/185. If this is not the case, use a flip-flop, which is set by the falling edge of RD and reset by the rising edge of BUSY.

High-Speed 12-Bit A/D Converters With External Reference Input

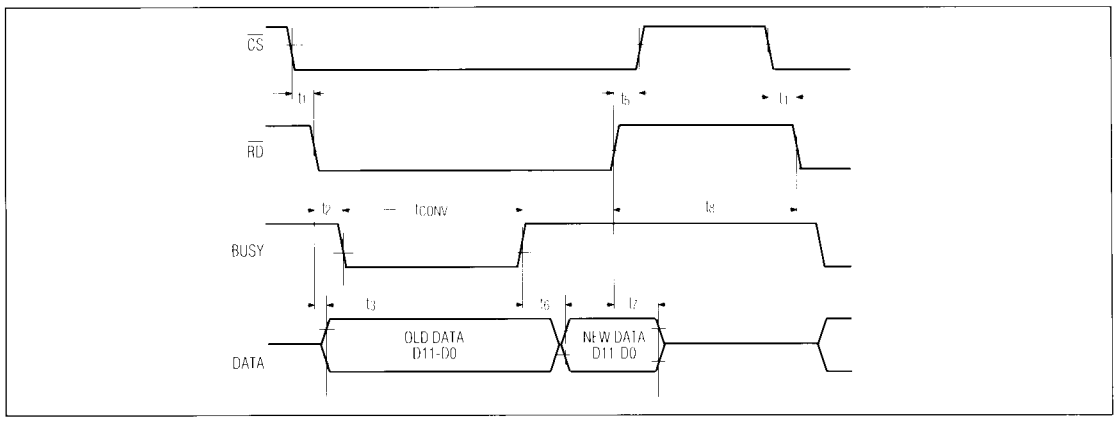


Figure 9. Slow Memory Mode Timing Diagram

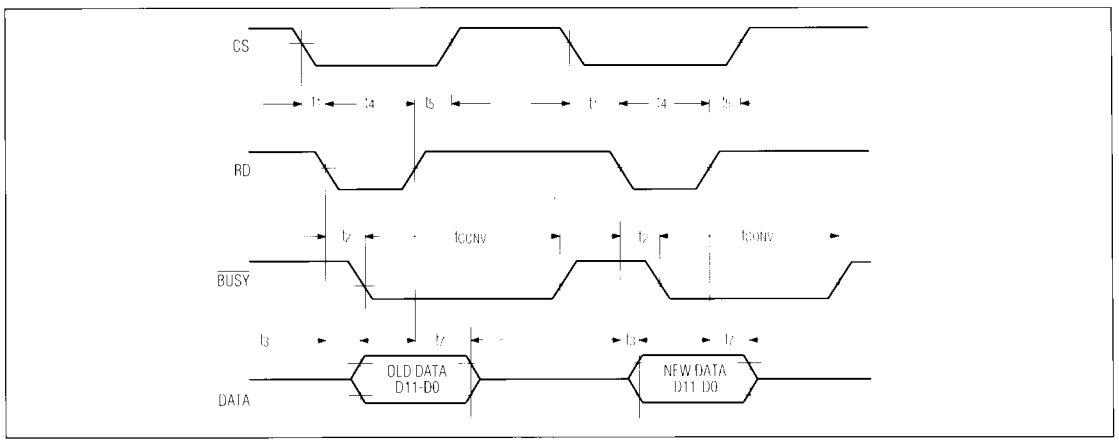


Figure 10. ROM Mode Timing Diagram

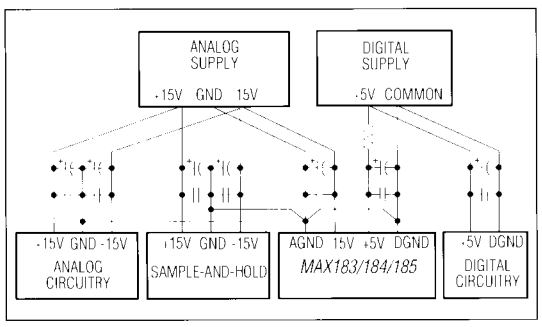


Figure 11. Power-Supply Grounding Practice

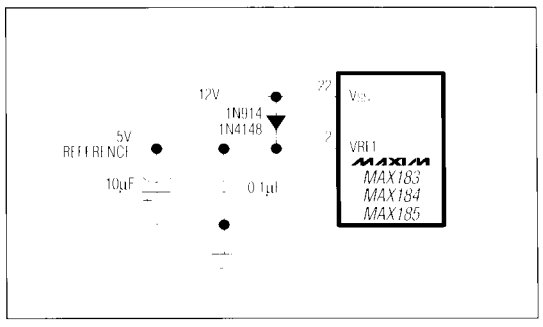


Figure 12. VREF/VSS Diode Clamp (See "Reference Input" Text).

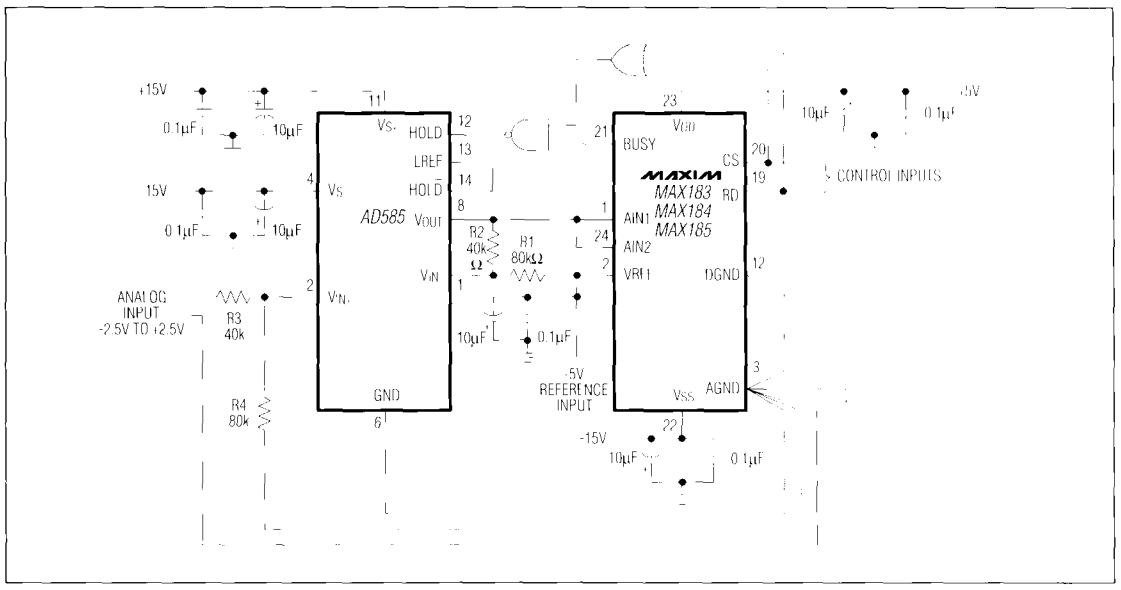


Figure 13. MAX183/184/185 –AD585 Sample-and-Hold Interface

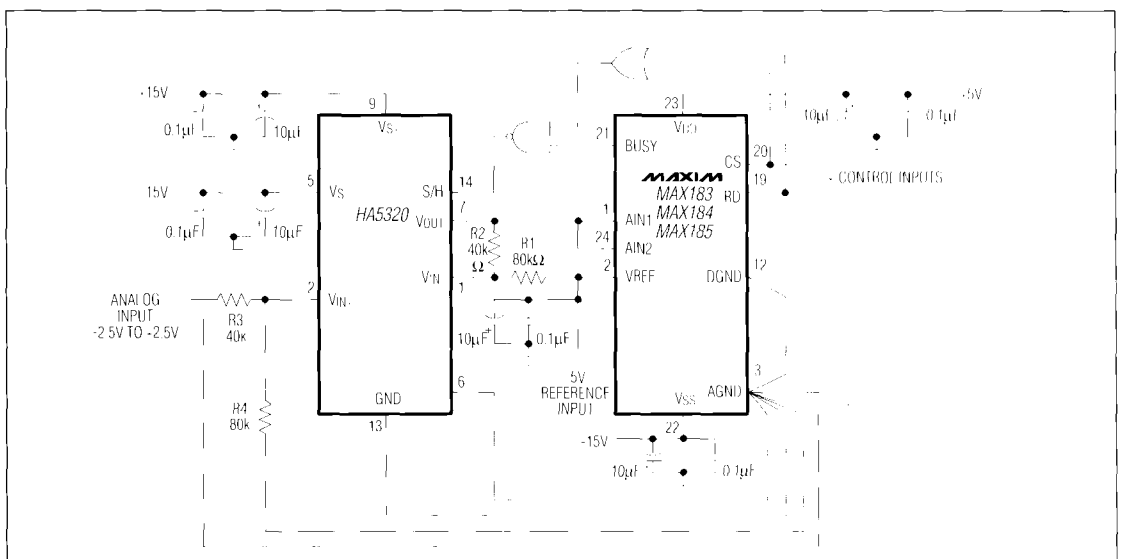


Figure 14. MAX183/184/185– HA5320 Sample-and-Hold Interface

For synchronous RD and CLKIN, the hold settling time allowed for the sample-and-hold is 375ns (MAX183), 600ns (MAX184), and 1.5µs (MAX185).

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock, allowing for a 3µs sample-and-hold acquisition time.

Although this circuit works well for the 1MHz clock rate, a faster sample-and-hold amplifier, such as the HA5320, is recommended at a 2.5MHz clock rate.

MAX183 – Figure 14 is the MAX183 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock, which allows a 1.5µs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Analog Input Ranges

The MAX183/184/185 provides three selectable analog input ranges: 0V to +5V, 0V to +10V, and ±5V. Figure 15 shows the configuration for the two analog inputs (AIN1 and AIN2) for these ranges.

Unipolar Operation

Figure 16 shows unipolar operation using a MX584 voltage reference configured for -5V.

Figure 17 shows the nominal input/output transfer function of the MAX183/184/185. Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = Full Scale (FS)/4096. FS is either +5V or +10V, based on the analog input configurations.

Offset and Full-Scale Adjustment

In applications requiring offset and FS range adjustment, use the circuit in Figure 19. Note: The amplifier shown could also be a sample-and-hold. Offset should be adjusted first. Apply 1/2LSB (0.61mV) at the analog input (AIN1 or AIN2) and adjust the offset of the amplifier until

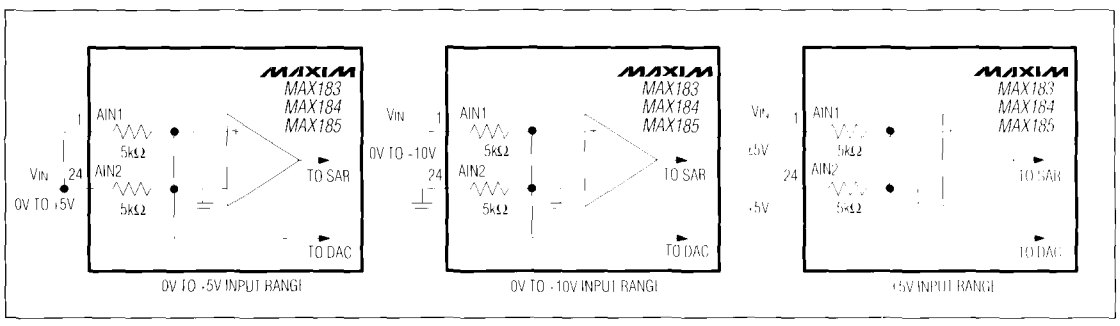


Figure 15. Analog Input Range Configurations

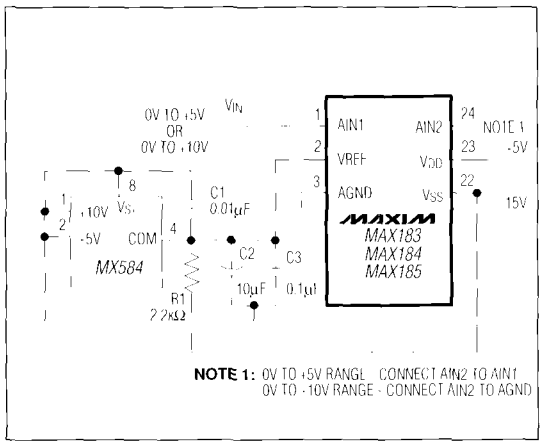


Figure 16. Unipolar Operation Using a MX584 Reference

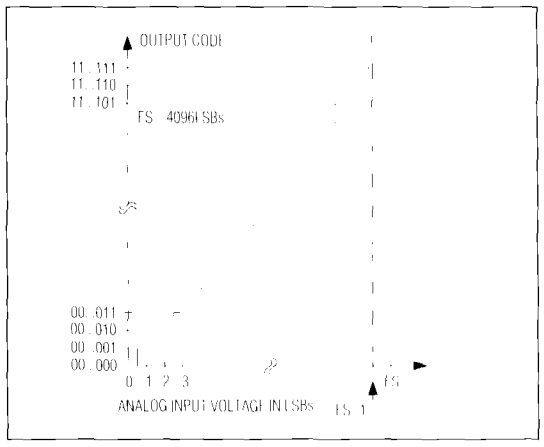


Figure 17. MAX183/184/185 Ideal Unipolar Transfer Function

the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

0V to +5V range: 1/2LSB = 0.61mV
0V to +10V range: 1/2LSB = 1.22mV

To adjust the full-scale range, apply FS-3/2LSB (last code transition) at the analog input and adjust R1 until the output code switches between 1111 1111 1110 and 1111 1111 1111.

0V to +5V range: FS-3/2LSB = 4.99817V
0V to +10V range: FS-3/2LSB = 9.99634V

Bipolar Operation

The bipolar input range is ±5V. V_{IN} is applied to AIN1, +5V to AIN2, and -5V to VREF. This requires two reference voltages: -5V for the VREF input and +5V for the AIN2 input. Figure 19 shows these reference voltages are produced from a MAX675 reference and a MAX400 op amp configured as an inverting amplifier.

The ideal input/output transfer characteristic after offset and gain adjustment is shown in Figure 20. The LSB is 2.44mV (10V/4096).

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full-scale adjustments must be made in bipolar circuits. If low tolerances are used, larger value potentiometers must be used, which results in poor trim resolution and higher temperature drift.

Offset and Gain Adjustment

In bipolar operation, the offset is trimmed at negative full scale and should always be adjusted first. For offset, apply -FS/2 + 1/2LSB (-4.99878V) at V_{IN} and adjust the 10kΩ potentiometer (Figure 18) until the output code switches between 0000 0000 0000 and 0000 0000 0001.

Gain is adjusted at full scale or bipolar zero. For full scale adjustment, apply FS/2 - 3/2LSBs (4.99634V) to V_{IN} and adjust the 200Ω potentiometer until the output code switches between 1111 1111 1110 and 1111 1111 1111.

Alternatively, to adjust gain at bipolar zero, apply -1.22mV at V_{IN} and adjust the 200Ω potentiometer until the output code switches between 0111 1111 1111 and 1000 0000 0000.

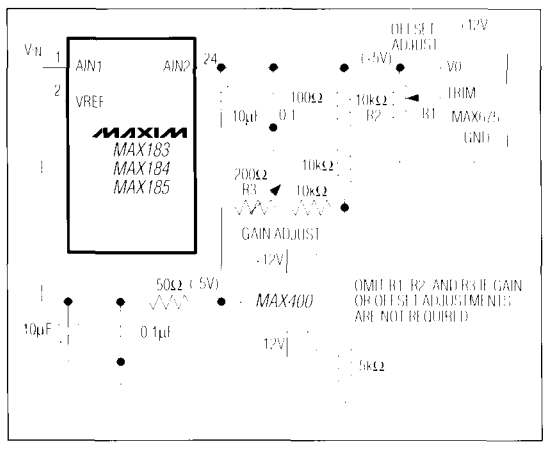


Figure 19. Bipolar Operation with Offset and Gain Error Adjust

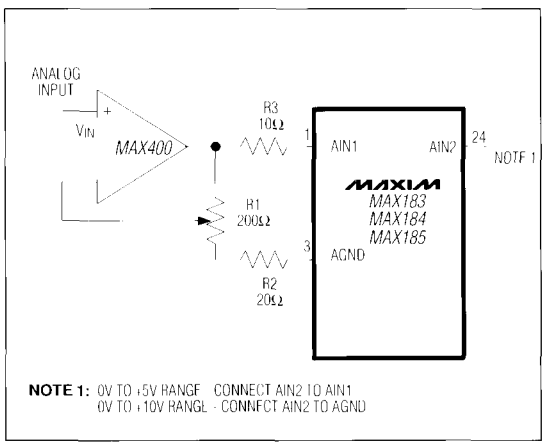


Figure 18. Unipolar Operation with Gain Adjust

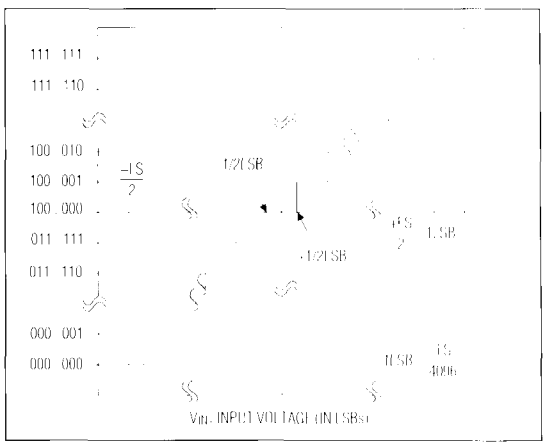


Figure 20. Ideal Input/Output Transfer Characteristic for Bipolar Operation

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSBs)
MAX183AENG	-40 C to +85 C	24 Plastic DIP	±1/2
MAX183BENG	-40 C to +85 C	24 Plastic DIP	±1
MAX183AEWG	-40 C to +85 C	24 Wide SO	±1/2
MAX183BEWG	-40 C to +85 C	24 Wide SO	±1
5µs Maximum Conversion Time			
MAX184ACNG	0 C to +70 C	24 Plastic DIP	±1/2
MAX184BCNG	0 C to +70 C	24 Plastic DIP	±1
MAX184ACWG	0 C to +70 C	24 Wide SO	±1/2
MAX184BCWG	0 C to +70 C	24 Wide SO	±1
MAX184BC/D	0 C to +70 C	Dice*	±1
MAX184AENG	-40 C to +85 C	24 Plastic DIP	±1/2
MAX184BENG	-40 C to +85 C	24 Plastic DIP	±1
MAX184AEWG	-40 C to +85 C	24 Wide SO	±1/2
MAX184BEWG	-40 C to +85 C	24 Wide SO	±1
MAX184AMRG	-55 C to +125 C	24 CERDIP**	±3/4
MAX184BMRG	-55 C to +125 C	24 CERDIP**	±1
10µs Maximum Conversion Time			
MAX185ACNG	0 C to +70 C	24 Plastic DIP	±1/2
MAX185BCNG	0 C to +70 C	24 Plastic DIP	±1
MAX185ACWG	0 C to +70 C	24 Wide SO	±1/2
MAX185BCWG	0 C to +70 C	24 Wide SO	±1
MAX185BC/D	0 C to +70 C	Dice*	±1
MAX185AENG	-40 C to +85 C	24 Plastic DIP	±1/2
MAX185BENG	-40 C to +85 C	24 Plastic DIP	±1
MAX185AEWG	-40 C to +85 C	24 Wide SO	±1/2
MAX185BEWG	-40 C to +85 C	24 Wide SO	±1
MAX185AMRG	-55 C to +125 C	24 CERDIP**	±3/4
MAX185BMRG	-55 C to +125 C	24 CERDIP**	±1

* *Consult factory for dice specifications.*

** *Contact factory for processing to Mil -STD-883.*